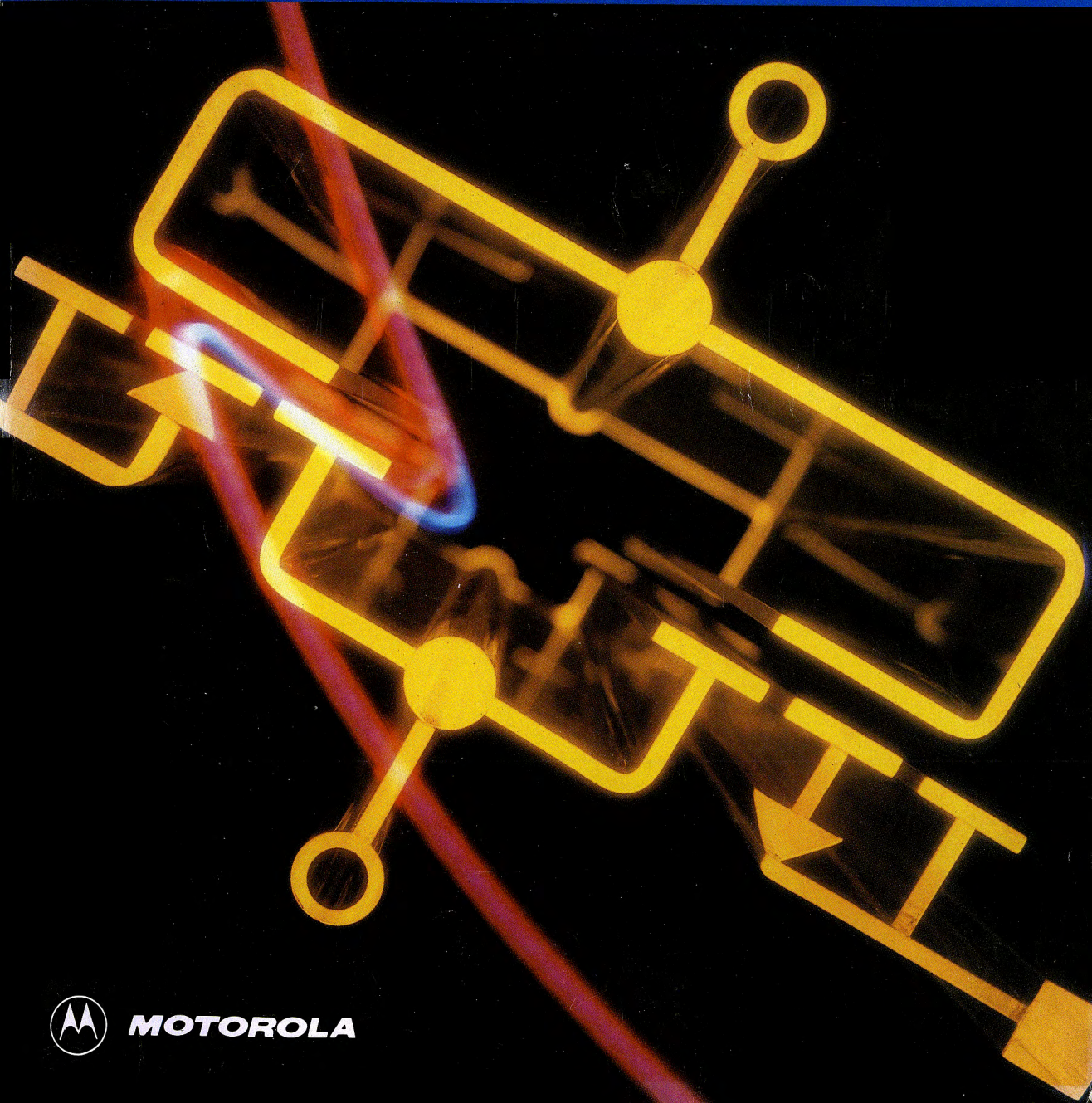


DL131
REV 3

CMOS Logic

Data



MOTOROLA

Master Index **1**

Product Selection Guide **2**

The “Better” Program **3**

B and UB Series Family Data **4**

CMOS Handling and Design Guidelines **5**

Data Sheets **6**

CMOS Reliability **7**

Equivalent Gate Count **8**

**Packaging Information
Including Surface Mounts** **9**

DATA CLASSIFICATION

Product Preview

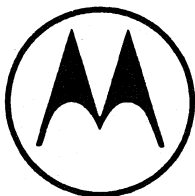
This heading on a data sheet indicates that the device is in the formative stages or in design (under development). The disclaimer at the bottom of the first page reads: "This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice."

Advance Information

This heading on a data sheet indicates that the device is in sampling, pre-production, or first production stages. The disclaimer at the bottom of the first page reads: "This document contains information on a new product. Specifications and information herein are subject to change without notice."

Fully Released

A fully released data sheet contains neither a classification heading nor a disclaimer at the bottom of the first page. This document contains information on a product in full production. Guaranteed limits will not be changed without written notice to your local Motorola Semiconductor Sales Office.




MOTOROLA

CMOS LOGIC DATA

Prepared by
Technical Information Center

This book presents technical data for the broad line of CMOS logic integrated circuits and demonstrates Motorola's continued commitment to Metal-Gate CMOS. Complete specifications are provided in the form of data sheets. In addition, a Product Selector Guide and a Handling and Design Guidelines chapter have been included to familiarize the user with these circuits.

Motorola reserves the right to make changes without further notice to any products herein to improve reliability, function or design. Motorola does not assume any liability arising out of the application or use of any product or circuit described herein; neither does it convey any license under its patent rights nor the rights of others. Motorola products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Motorola product could create a situation where personal injury or death may occur. Should Buyer purchase or use Motorola products for any such unintended or unauthorized application, Buyer shall indemnify and hold Motorola and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Motorola was negligent regarding the design or manufacture of the part. Motorola and  are registered trademarks of Motorola, Inc. Motorola, Inc. is an Equal Employment Opportunity/Affirmative Action Employer.

Master Index

1

MASTER INDEX

This index includes Motorola's entire MC14000 series CMOS products, although this book contains data sheets for Logic Devices only. Data sheets for devices in the CMOS/NMOS Special Functions Data book (DL130) are designated in the page number column as SF.

Products which have been cancelled are designated in the page number column as —.

Device	Function	Page
MC14000UB	Dual 3-Input NOR Gate Plus Inverter	6-2
MC14001B	Quad 2-Input NOR Gate	6-5
MC14001UB	Quad 2-Input NOR Gate	6-14
MC14002B	Dual 4-Input NOR Gate	6-5
MC14002UB	Dual 4-Input NOR Gate	6-14
MC14006B	18-Bit Static Shift Register	6-19
MC14007UB	Dual Complementary Pair Plus Inverter	6-23
MC14008B	4-Bit Full Adder	6-27
MC14011B	Quad 2-Input NAND Gate	6-5
MC14011UB	Quad 2-Input NAND Gate	6-14
MC14012B	Dual 4-Input NAND Gate	6-5
MC14012UB	Dual 4-Input NAND Gate	6-14
MC14013B	Dual D Flip-Flop	6-33
MC14014B	8-Bit Static Shift Register	6-37
MC14015B	Dual 4-Bit Static Shift Register	6-41
MC14016B	Quad Analog Switch/Multiplexer	6-47
MC14017B	Decade Counter	6-54
MC14018B	Presetable Divide-by-N Counter	6-59
MC14020B	14-Bit Binary Counter	6-63
MC14021B	8-Bit Static Shift Register	6-37
MC14022B	Octal Counter	6-67
MC14023B	Triple 3-Input NAND Gate	6-5
MC14023UB	Triple 3-Input NAND Gate	6-14
MC14024B	7-Stage Ripple Counter	6-72
MC14025B	Triple 3-Input NOR Gate	6-5
MC14025UB	Triple 3-Input NOR Gate	6-14
MC14027B	Dual J-K Flip-Flop	6-77
MC14028B	BCD-to-Decimal/Binary-to-Octal Decoder	6-81
MC14029B	Presetable Binary/BCD Up/Down Counter	6-86
MC14032B	Triple Serial Adder (Positive Logic)	6-92
MC14034B	8-Bit Universal Bus Register	6-97
MC14035B	4-Bit Shift Register	6-104
MC14038B	Triple Serial Adder (Negative Logic)	6-92
MC14040B	12-Bit Binary Counter	6-108
MC14042B	Quad Transparent Latch	6-112
MC14043B	Quad NOR R-S Latch	6-116
MC14044B	Quad NAND R-S Latch	6-116
MC14046B	Phase-Locked Loop	6-120

Device	Function	Page
MC14049B	Hex Inverting Buffer	6-125
MC14049UB	Hex Inverting Buffer	6-129
MC14050B	Hex Noninverting Buffer	6-125
MC14051B	8-Channel Analog Multiplexer/Demultiplexer	6-133
MC14052B	Dual 4-Channel Analog Multiplexer/Demultiplexer	6-133
MC14053B	Triple 2-Channel Analog Multiplexer/Demultiplexer	6-133
MC14060B	14-Bit Binary Counter and Oscillator	6-140
MC14066B	Quad Analog Switch/Multiplexer	6-144
MC14067B	16-Channel Analog Multiplexer/Demultiplexer	6-150
MC14068B	8-Input NAND Gate	6-5
MC14069UB	Hex Inverter	6-158
MC14070B	Quad Exclusive OR Gate	6-160
MC14071B	Quad 2-Input OR Gate	6-5
MC14072B	Dual 4-Input OR Gate	6-5
MC14073B	Triple 3-Input AND Gate	6-5
MC14075B	Triple 3-Input OR Gate	6-5
MC14076B	Quad D-Type Register with Tri-State Outputs	6-162
MC14077B	Quad Exclusive NOR Gate	6-160
MC14078B	8-Input NOR Gate	6-5
MC14081B	Quad 2-Input AND Gate	6-5
MC14082B	Dual 4-Input AND Gate	6-5
MC14093B	Quad 2-Input NAND Schmitt Trigger	6-166
MC14094B	8-Stage Shift/Store Register with Tri-State Outputs	6-170
MC14097B	Dual 8-Channel Analog Multiplexer/Demultiplexer	6-150
MC14099B	8-Bit Addressable Latch	6-174
MC14106B	Hex Schmitt Trigger	6-180
MC14160B	Synchronous Presettable BCD Counter	6-184
MC14161B	Synchronous Presettable 4-Bit Binary Counter	6-184
MC14162B	Synchronous Presettable BCD Counter	6-184
MC14163B	Synchronous Presettable 4-Bit Binary Counter	6-184
MC14174B	Hex D Flip-Flop	6-193
MC14175B	Quad D Flip-Flop	6-197
MC14194B	4-Bit Universal Shift Register	6-201
MC14415	Quad Precision Timer/Driver	6-205
MC14433	3½ Digit A/D Converter	SF
MC14442	Microprocessor-Compatible A/D Converter	SF
MC14443	6-Channel A/D Converter Subsystem	SF

Device	Function	Page
MC14444	Microprocessor-Compatible A/D Converter	SF
MC14447	6-Channel A/D Converter Subsystem.	SF
MC14457	Remote Control Transmitter	SF
MC14458	Remote Control Receiver.	SF
MC14460	Automotive Speed Control Processor.	SF
MC14466	Low Cost Smoke Detector	SF
MC14467-1	Low Cost Smoke Detector	SF
MC14468	Interconnectable Smoke Detector	SF
MC14469	Addressable Asynchronous Receiver/Transmitter	SF
MC14490	Hex Contact Bounce Eliminator.	6-210
MC14495-1	Hexadecimal-to-7 Segment Latch/Decoder ROM/Driver.	SF
MC14497	PCM Remote Control Transmitter	SF
MC14499	7-Segment LED Display Decoder/Driver with Serial Interface	SF
MC14500B	Industrial Control Unit	6-217
MC14501UB	Triple Gate	6-223
MC14502B	Strobed Hex Inverter/Buffer	6-227
MC14503B	Hex 3-State Buffer	6-231
MC14504B	TTL or CMOS to CMOS Hex Level Shifter	6-235
MC14506UB	Dual Expandable AOI Gate	6-238
MC14508B	Dual 4-Bit Latch.	6-243
MC14510B	Presettable BCD Up/Down Counter	6-248
MC14511B	BCD-to-7-Segment Latch/Decoder/Driver	6-256
MC14512B	8-Channel Data Selector	6-262
MC14513B	BCD-to-7-Segment Latch/Decoder/Driver with Ripple Blanking	6-266
MC14514B	4-Bit Transparent Latch/4-to-16 Line Decoder (High).	6-274
MC14515B	4-Bit Transparent Latch/4-to-16 Line Decoder (Low)	6-274
MC14516B	Presettable Binary Up/Down Counter.	6-280
MC14517B	Dual 64-Bit Static Shift Register	6-288
MC14518B	Dual BCD Up Counter.	6-292
MC14519B	4-Bit AND/OR Selector	6-297
MC14520B	Dual Binary Up Counter	6-292
MC14521B	24-Stage Frequency Divider.	6-301
MC14522B	Presettable BCD Down Counter	6-307

Device	Function	Page
MC14526B	Presetable 4-Bit Binary Down Counter	6-307
MC14527B	BCD Rate Multiplier	6-315
MC14528B	Dual Monostable Multivibrator	6-321
MC14529B	Dual 4-Channel Analog Data Selector	6-327
MC14530B	Dual 5-Input Majority Logic Gate	6-333
MC14531B	12-Bit Parity Tree	6-338
MC14532B	8-Bit Priority Encoder	6-341
MC14534B	5 Cascaded BCD Counters	6-347
MC14536B	Programmable Timer	6-354
MC14538B	Dual Precision Monostable Multivibrator	6-365
MC14539B	Dual 4-Channel Data Selector/Multiplexer	6-373
MC14541B	Programmable Oscillator/Timer	6-377
MC14543B	BCD-to-7-Segment Latch/Decoder/Driver for Liquid Crystals	6-382
MC14544B	BCD-to-7-Segment Latch/Decoder/Driver with Ripple Blanking	6-387
MC14547B	High-Current BCD-to-7-Segment Decoder/Driver	6-393
MC14549B	Successive Approximation Registers	6-398
MC14551B	Quad 2-Channel Analog Multiplexer/Demultiplexer	6-405
MC14553B	3-Digit BCD Counter	6-412
MC14554B	2 x 2-Bit Parallel Binary Multiplier	6-418
MC14555B	Dual Binary to 1-of-4 Decoder (Active High Outputs)	6-422
MC14556B	Dual Binary to 1-of-4 Decoder (Active Low Outputs)	6-422
MC14557B	1-to-64 Bit Variable Length Shift Register	6-425
MC14558B	BCD-to-7-Segment Decoder	6-429
MC14559B	Successive Approximation Registers	6-398
MC14560B	NBCD Adder	6-434
MC14561B	9's Complementer	6-445
MC14562B	128-Bit Static Shift Register	6-451
MC14566B	Industrial Time Base Generator	6-455
MC14568B	Phase Comparator and Programmable Counters	6-461
MC14569B	Programmable Dual 4-Bit Binary/BCD Down Counter	6-471
MC14572UB	Hex Gate	6-481
MC14573	Quad Programmable Op Amp	SF
MC14574	Quad Programmable Comparator	SF
MC14575	Programmable Dual Op Amp/Dual Comparator	SF
MC14580B	4 x 4 Multiport Register	6-484
MC14581B	4-Bit Arithmetic Logic Unit	6-489
MC14582B	Look-Ahead Carry Block	6-494

Device	Function	Page
MC14583B	Dual Schmitt Trigger	6-498
MC14584B	Hex Schmitt Trigger	6-504
MC14585B	4-Bit Magnitude Comparator.	6-507
MC14597B	8-Bit Bus-Compatible Counter Latch	6-511
MC14598B	8-Bit Bus-Compatible Addressable Latch	6-511
MC14599B	8-Bit Addressable Latch.	6-174
MC144110	Hex D/A Converter with Serial Interface	SF
MC144111	Quad D/A Converter with Serial Interface	SF
MC145000	48-Segment Multiplexed LCD Driver (Master)	SF
MC145001	44-Segment Multiplexed LCD Driver (Slave)	SF
MC145026	Remote Control Encoder	SF
MC145027	Remote Control Decoder	SF
MC145028	Remote Control Decoder	SF
MC145029	Remote Control Decoder	SF
MC145040	Analog-to-Digital Converter with Serial Interface.	SF
MC145041	Analog-to-Digital Converter with Serial Interface.	SF
MC145104	PLL Frequency Synthesizer (Not Recommended for New Designs)	SF
MC145106	PLL Frequency Synthesizer	SF
MC145107	PLL Frequency Synthesizer (Not Recommended for New Designs)	SF
MC145109	PLL Frequency Synthesizer (Not Recommended for New Designs)	SF
MC145112	PLL Frequency Synthesizer (Not Recommended for New Designs)	SF
MC145143	PLL Frequency Synthesizer (Not Recommended for New Designs)	SF
MC145144	4-Bit Data Bus Input PLL Frequency Synthesizer (Not Recommended for New Designs)	SF
MC145145-1	4-Bit Data Bus Input PLL Frequency Synthesizer	SF
MC145146-1	4-Bit Data Bus Input PLL Frequency Synthesizer	SF
MC145151-1	Parallel Input PLL Frequency Synthesizer	SF
MC145152-1	Parallel Input PLL Frequency Synthesizer	SF
MC145155-1	Serial Input PLL Frequency Synthesizer	SF
MC145156-1	Serial Input PLL Frequency Synthesizer	SF
MC145157-1	Serial Input PLL Frequency Synthesizer	SF
MC145158-1	Serial Input PLL Frequency Synthesizer	SF
MC145159-1	Serial Input PLL Frequency Synthesizer with Analog Phase Detector.	SF
MC145453	33-Segment LCD Driver with Serial Interface.	SF

Product Selection Guide

2

CMOS Selection Guide by Function

2

Device	Function	Page
NAND Gates		
MC14011B	Quad 2-Input NAND Gate	6-5
MC14011UB	Quad 2-Input NAND Gate	6-14
MC14093B	Quad 2-Input NAND Schmitt Trigger	6-166
MC14023B	Triple 3-Input NAND Gate	6-5
MC14023UB	Triple 3-Input NAND Gate	6-14
MC14012B	Dual 4-Input NAND Gate	6-5
MC14012UB	Dual 4-Input NAND Gate	6-14
MC14068B	8-Input NAND Gate	6-5
NOR Gates		
MC14001B	Quad 2-Input NOR Gate	6-5
MC14001UB	Quad 2-Input NOR Gate	6-14
MC14025B	Triple 3-Input NOR Gate	6-5
MC14025UB	Triple 3-Input NOR Gate	6-14
MC14000UB	Dual 3-Input NOR Gate Plus Inverter	6-2
MC14002B	Dual 4-Input NOR Gate	6-5
MC14002UB	Dual 4-Input NOR Gate	6-14
MC14078B	8-Input NOR Gate	6-5
AND Gates		
MC14081B	Quad 2-Input AND Gate	6-5
MC14073B	Triple 3-Input AND Gate	6-5
MC14082B	Dual 4-Input AND Gate	6-5
OR Gates		
MC14071B	Quad 2-Input OR Gate	6-5
MC14075B	Triple 3-Input OR Gate	6-5
MC14072B	Dual 4-Input OR Gate	6-5
Complex Gates		
MC14070B	Quad Exclusive OR Gate	6-160
MC14077B	Quad Exclusive NOR Gate	6-160
MC14501UB	Triple Gate	6-223
MC14506UB	Dual Expandable AOI Gate	6-238
MC14530B	Dual 5-Input Majority Logic Gate	6-333
MC14519B	4-Bit AND/OR Selector	6-297
MC14572UB	Hex Gate	6-481
Inverters/Buffers/Level Translator		
MC14007UB	Dual Complementary Pair Plus Inverter	6-23
MC14049B	Hex Inverting Buffer	6-125
MC14049UB	Hex Inverting Buffer	6-129
MC14050B	Hex Noninverting Buffer	6-125
MC14069UB	Hex Inverter	6-158
MC14502B	Strobed Hex Inverter/Buffer	6-227
MC14503B	Hex 3-State Buffer	6-231
MC14504B	TTL or CMOS to CMOS Hex Level Shifter	6-235
MC14584B	Hex Schmitt Trigger	6-504

Device	Function	Page
Decoders/Encoders		
MC14028B	BCD-to-Decimal/Binary-to-Octal Decoder	6-81
MC14511B	BCD-to-7-Segment Latch/Decoder/Driver	6-256
MC14513B	BCD-to-7-Segment Latch/Decoder/Driver with Ripple Blanking.	6-266
MC14543B	BCD-to-7-Segment Latch/Decoder/Driver for Liquid Crystals	6-382
MC14544B	BCD-to-7-Segment Latch/Decoder/Driver with Ripple Blanking.	6-387
MC14547B	High-Current BCD-to-7-Segment Decoder/Driver	6-393
MC14558B	BCD-to-7-Segment Decoder	6-429
MC14514B	4-Bit Transparent Latch/4-to-16 Line Decoder (High)	6-274
MC14515B	4-Bit Transparent Latch/4-to-16 Line Decoder (Low)	6-274
MC14532B	8-Bit Priority Encoder	6-341
MC14555B	Dual Binary to 1-of-4 Decoder (Active High Outputs)	6-422
MC14556B	Dual Binary to 1-of-4 Decoder (Active Low Outputs)	6-422
Multiplexers/Demultiplexers/Bilateral Switches		
MC14016B	Quad Analog Switch/Multiplexer	6-47
MC14066B	Quad Analog Switch/Multiplexer	6-144
MC14551B	Quad 2-Channel Analog Multiplexer/Demultiplexer.	6-405
MC14053B	Triple 2-Channel Analog Multiplexer/Demultiplexer	6-133
MC14052B	Dual 4-Channel Analog Multiplexer/Demultiplexer	6-133
MC14097B	Dual 8-Channel Analog Multiplexer/Demultiplexer	6-150
MC14529B	Dual 4-Channel Analog Data Selector	6-327
MC14539B	Dual 4-Channel Data Selector/Multiplexer	6-373
MC14067B	16-Channel Analog Multiplexer/Demultiplexer	6-150
MC14051B	8-Channel Analog Multiplexer/Demultiplexer.	6-133
MC14512B	8-Channel Data Selector.	6-262
MC14519B	4-Bit AND/OR Selector.	6-297
Schmitt Triggers		
MC14093B	Quad 2-Input NAND Schmitt Trigger	6-166
MC14583B	Dual Schmitt Trigger	6-498
MC14106B	Hex Schmitt Trigger	6-180
MC14584B	Hex Schmitt Trigger	6-504
Flip-Flops/Latches		
MC14042B	Quad Transparent Latch	6-112
MC14043B	Quad NOR R-S Latch	6-116
MC14044B	Quad NAND R-S Latch	6-116
MC14076B	Quad D-Type Register with Tri-State Outputs	6-162
MC14175B	Quad D Flip-Flop.	6-197
MC14013B	Dual D Flip-Flop	6-33
MC14027B	Dual J-K Flip-Flop	6-77
MC14508B	Dual 4-Bit Latch	6-243
MC14174B	Hex D Flip-Flop.	6-193
MC14099B	8-Bit Addressable Latch	6-174
MC14597B	8-Bit Bus-Compatible Counter Latch	6-511
MC14598B	8-Bit Bus-Compatible Addressable Latch	6-511
MC14599B	8-Bit Addressable Latch	6-174

Device	Function	Page
Shift Registers		
MC14015B	Dual 4-Bit Static Shift Register	6-41
MC14517B	Dual 64-Bit Static Shift Register	6-288
MC14562B	128-Bit Shift Register	6-451
MC14557B	1-to-64 Bit Variable Length Shift Register	6-425
MC14006B	18-Bit Static Shift Register	6-19
MC14014B	8-Bit Static Shift Register	6-37
MC14021B	8-Bit Static Shift Register	6-37
MC14034B	8-Bit Universal Bus Register	6-97
MC14094B	8-Stage Shift/Store Register with Tri-State Outputs	6-170
MC14035B	4-Bit Shift Register	6-104
MC14194B	4-Bit Universal Shift Register	6-201
MC14549B	Successive Approximation Registers	6-398
MC14559B	Successive Approximation Registers	6-398
Counters		
MC14017B	Decade Counter	6-54
MC14018B	Presetable Divide-by-N Counter	6-59
MC14020B	14-Bit Binary Counter	6-63
MC14022B	Octal Counter	6-67
MC14024B	7-Stage Ripple Counter	6-72
MC14029B	Presetable Binary/BCD Up/Down Counter	6-86
MC14040B	12-Bit Binary Counter	6-108
MC14060B	14-Bit Binary Counter and Oscillator	6-140
MC14160B	Synchronous Presetable BCD Counter	6-184
MC14161B	Synchronous Presetable 4-Bit Binary Counter	6-184
MC14162B	Synchronous Presetable BCD Counter	6-184
MC14163B	Synchronous Presetable 4-Bit Binary Counter	6-184
MC14510B	Presetable BCD Up/Down Counter	6-248
MC14516B	Presetable Binary Up/Down Counter	6-280
MC14518B	Dual BCD Up Counter	6-292
MC14520B	Dual Binary Up Counter	6-292
MC14522B	Presetable BCD Down Counter	6-307
MC14526B	Presetable 4-Bit Binary Down Counter	6-307
MC14534B	5 Cascaded BCD Counters	6-347
MC14553B	3-Digit BCD Counter	6-412
MC14566B	Industrial Time Base Generator	6-455
MC14569B	Programmable Dual 4-Bit Binary/BCD Counter	6-471
Oscillators/Timers		
MC14521B	24-Stage Frequency Divider	6-301
MC14536B	Programmable Timer	6-354
MC14541B	Programmable Oscillator/Timer	6-377
Multivibrators		
MC14528B	Dual Monostable Multivibrator	6-321
MC14538B	Dual Precision Monostable Multivibrator	6-365

Device	Function	Page
Adders/Comparators		
MC14008B	4-Bit Full Adder	6-27
MC14032B	Triple Serial Adder (Positive Logic)	6-92
MC14038B	Triple Serial Adder (Negative Logic)	6-92
MC14560B	NBCD Adder	6-434
MC14561B	9's Complementer	6-445
MC14582B	Look-Ahead Carry Block	6-494
MC14585B	4-Bit Magnitude Comparator	6-507
ALU/Rate Multipliers		
MC14527B	BCD Rate Multiplier	6-315
MC14554B	2 x 2-Bit Parallel Binary Multiplier	6-418
MC14581B	4-Bit Arithmetic Logic Unit	6-489
Parity Checker		
MC14531B	12-Bit Parity Tree	6-338
Memory		
MC14580B	4 x 4 Multiport Register	6-484
Microprocessor/Industrial Control		
MC14500B	Industrial Control Unit	6-217
Other Complex Functions		
MC14046B	Phase-Locked Loop	6-120
MC14415	Quad Precision Timer/Driver	6-205
MC14490	Hex Contact Bounce Eliminator	6-210
MC14568B	Phase Comparator and Programmable Counters	6-461

The “Better” Program

3

THE "BETTER" PROGRAM

The "BETTER" program is offered on logic only, in dual-in-line plastic packages.

3

Better Processing — Standard Product Plus:

LEVEL II (Suffix D)

- 100% burn-in to MIL-STD-883 test conditions — 160 hours at +125°C or 1.0 eV Arrhenius time/temperature equivalent.
- 100% post burn-in functional and dc parametric tests at 25°C (or max rated T_A at Motorola's option). Maximum PDA of 2% (functional) and 5% (DC and functional).

HOW TO ORDER

<u>MC1400B</u>	<u>CP</u>	<u>D</u>
Part	Standard	BETTER
Identification	Package	PROCESSING
	Suffix	LEVEL II = SUFFIX D

Part Marking

The Standard motorola part number with the corresponding "BETTER" suffix can be ordered from your local authorized Motorola distributor or Motorola sales offices. "BETTER" pricing will be quoted as an adder to standard commercial product price.

"RAP" Reliability Audit Program for Logic Integrated Circuits

1.0 INTRODUCTION

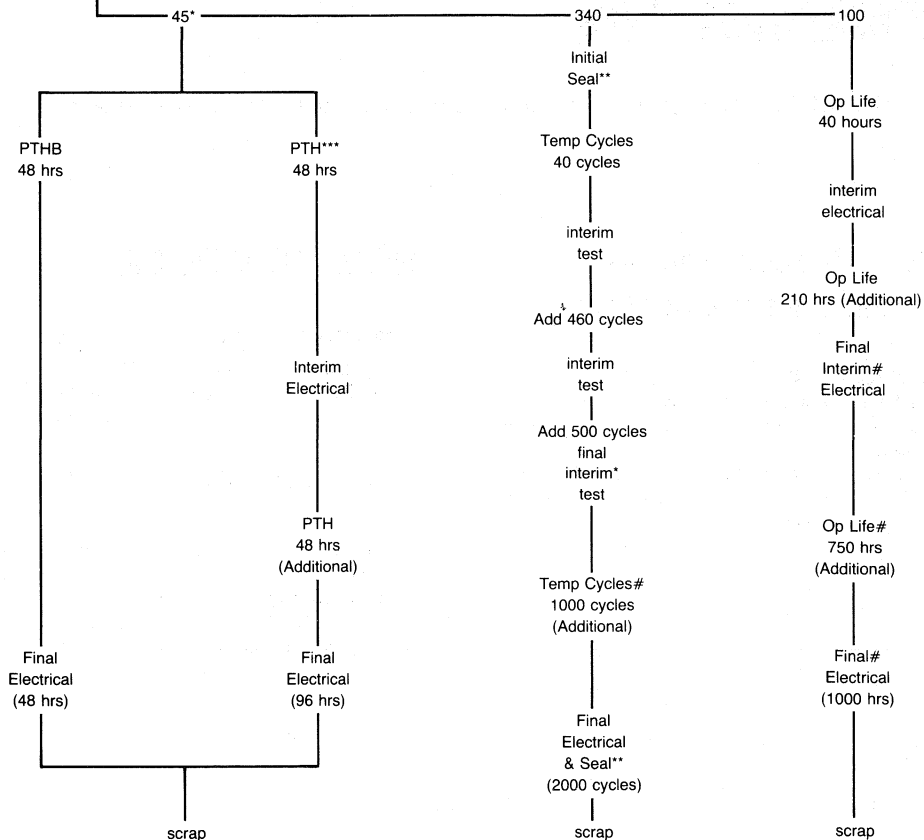
The Reliability Audit Program developed in March 1977 is the Motorola internal reliability audit which is designed to assess outgoing product performance under accelerated stress conditions. Logic Reliability Engineering has overall responsibility for RAP, including updating its requirements, interpreting its results, administration at offshore locations, and monthly reporting of results. These reports are avail-

able at all sales offices. Also available is the "Reliability and Quality Handbook" which contains data for all Motorola Semiconductors (#BR518S).

RAP is a system of environmental and electrical tests performed periodically on randomly selected samples of standard products. Each sample receives the tests specified in section 2.0. Frequency of testing is specified per internal document 12MRM15301A.

2.0 RAP TEST FLOW

Pull 500* piece sample from lot following Group A acceptance.



*One sample per month for FAST, LS, 10H, 10K, MG CMOS, and HSL CMOS.

**PTHB or PTH not required for hermetic products: reduce total sample size to 450 pcs.

**Seal (Fine & Gross Leak) required only for hermetic products.

***PTH to be used when sockets for PTHB are not available.

3.0 TEST CONDITIONS AND COMMENTS

PTHB — 15 psig/121°C/100% RH at rated V_{CC} or V_{EE}
— to be performed on plastic encapsulated devices only.

TEMP CYCLING — MIL-STD-883, Method 1010, Condition C, $-65^{\circ}\text{C}/+150^{\circ}\text{C}$.

OP LIFE — MIL-STD-883, Method 1005, Condition C (Power plus Reverse Bias), $T_A = 145^{\circ}\text{C}$.

NOTES:

1. All standard 25°C dc and functional parameters will be measured Go/No/Go at each readout.
2. Any indicated failure is first verified and then submitted to the Product Analysis Lab for detailed analysis.
3. Sampling to include all package types routinely.
4. Device types sampled will be by generic type within each logic I/C product family (CMOS, TTL, etc.) and will include all assembly locations (Korea, Philippines, Malaysia, etc.)
5. 16 hrs. PTHB is equivalent to approximately 800 hours of $85^{\circ}\text{C}/85\%$ RH THB for $V_{CC} \leq 15\text{ V}$.
6. Only moisture related failures (like corrosion) are criteria for failure on PTHB test.
7. Special device specifications (48A's) for logic products will reference 12MRM15301A as source of generic data for any customer required monthly audit reports.



B and UB Series Family Data

4

B AND UB SERIES CMOS FAMILY DATA

The CMOS Devices in this volume which have a B or UB suffix meet the minimum values for the industry-standardized# family specification. These standardized values are shown in the Maximum Ratings and Electrical Characteristics Tables. In addition to a standard minimum specification for characteristics the B/UB devices feature:

- 3-18 volt operational limits
- Capable of driving two low-power TTL loads or one low-power Schottky TTL load over the rated temperature range
- Direct Interface to High-Speed CMOS
- Maximum input current of $\pm 1 \mu\text{A}$ at 15 volt power supply over the temperature range
- Parameters specified at 5.0, 10, and 15 volt supply
- Noise margins: B Series
 - 1.0 V min @ 5.0 V supply
 - 2.0 V min @ 10 V supply
 - 2.5 V min @ 15 V supply
- UB Series
 - 0.5 V min @ 5.0 V supply
 - 1.0 V min @ 10 V supply
 - 1.0 V min @ 15 V supply

The industry-standardized maximum ratings are shown at the bottom of this page. Limits for the static characteristics are shown in two formats: Table 1 is in the industry format and Table 2 is in the equivalent Motorola format. The Motorola format is used throughout this data book. Additional specification values are shown on the individual data sheets.

Switching characteristics for the B and UB series devices are specified under the following conditions:

- Load Capacitance, C_L , of 50 pF
- Input Voltage equal to $V_{SS} - V_{DD}$ (Rail-to-Rail swing)
- Input pulse rise and fall times of 20 ns
- Propagation Delay times measured from 50% point of input voltage to 50% point of output voltage
- Three different supply voltages: 5, 10, and 15 V

Exceptions to the B and UB Series Family Specification

There are a number of devices which have a B or UB suffix whose inputs and/or outputs vary somewhat from the family specification because of functional requirements. Some categories of notable exceptions are:

- Devices with specialized outputs on the chip, such as NPN emitter-follower drivers or transmission gates, do not meet output specifications.

#Specifications coordinated by EIA/JEDEC Solid-State Products Council.

Devices with specialized inputs, such as oscillator inputs, have unique input specifications.

Input Voltage

The input voltage specification is interpreted as the worst-case input voltage to produce an output level of "1" or "0". This "1" or "0" output level is defined as a deviation from the supply (V_{DD}) and ground (V_{SS}) levels. For a 5.0 V supply, this deviation is 0.5 V; for a 10 V supply, 1.0 V; and for 15 V, 1.5 V. As an example, in a device operating at a 5.0 V supply, the device with the input starting at ground is guaranteed to switch on or before 3.5 V and not to switch up to 1.5 V. Switching and not switching are defined as within 0.5 V of the ideal output level for the example with a 5.0 V supply. The actual switching level referred to the input is between 1.5 V and 3.5 V.

Noise Margin

The values for input voltages and the defined output deviations lead to the calculated noise margins. Noise margin is defined as the difference between V_{IL} or V_{IH} and V_{out} (output deviation). As an example, for a noninverting buffer at $V_{DD} = 5.0$ volts: $V_{IL} = 1.5$ volts and $V_{out} = 0.5$ volts. Therefore, Noise Margin equals $V_{IL} - V_{out} = 1.0$ volt. This figure is useful while cascading stages (See Figure 1). With the input to the first stage at a worst-case voltage level ($V_{IL} = 1.5$ V), the output is guaranteed to be no greater than 0.5 volts with a 5.0 volt supply. Since the maximum allowable logic 0 for the second stage is 1.5 volts, this 0.5 volt output provides a 1.0 volt margin for noise to the next stage.

Output Drive Current

Devices in the B Series are capable of sinking a minimum of 0.36 mA over the temperature range with a 5.0 V supply. This value guarantees that these CMOS devices will drive one low-power Schottky TTL input.

B Series vs UB CMOS

The primary difference between B series and UB series devices is that UB series gates and inverters are constructed with a single inverting stage between input and output. The decreased gain caused by using a single stage results in less noise immunity and a transfer characteristic that is less ideal.

The decreased gain is quite useful when CMOS Gates and inverters are used in a "Linear" mode to form oscillators, monostables, or amplifiers. The decreased gain results in increased stability and a "cleaner" output waveform. In addition to linear operation, the UB gates and inverters offer an increase in speed, since only a single stage is involved.

The B and UB series, and devices with no suffix can be used interchangeably in digital circuits that interface to other CMOS devices, such as High-Speed CMOS Logic.

4

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	-0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	-0.5 to $V_{DD} + 0.5$	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	± 10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.

†Temperature Derating: Plastic "P and D/DW" Packages: -7.0 mW/°C From 65°C to 125°C
Ceramic "L" Packages: -12 mW/°C From 100°C to 125°C

FIGURE 1

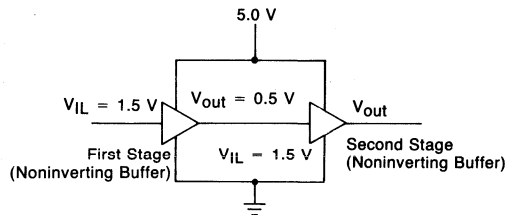


TABLE 1 – EIA/JEDEC FORMAT FOR CMOS INDUSTRY B AND UB SERIES SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

PARAMETER		TEMP RANGE	VDD (Vdc)	CONDITIONS	LIMITS						UNITS		
					T _{LOW} ^o		+ 25°C		T _{HIGH} ^o				
					Min	Max	Min	Max	Min	Max			
I _{DD}	Quiescent Device Current	Mil	5	V _{IN} = V _{SS} or V _{DD}		0.25		0.25		7.5	μAdc		
			10		0.5		0.5		15				
			15		1.0		1.0		30				
	GATES	Comm	5		All valid input combinations		1.0		1.0		7.5	μAdc	
			10			2.0		2.0		15			
			15			4.0		4.0		30			
	BUFFERS, FLIP-FLOPS	Mil	5			V _{IN} = V _{SS} or V _{DD}		1.0		1.0		30	μAdc
			10				2.0		2.0		60		
			15				4.0		4.0		120		
	MSI	Comm	5	All valid input combinations				4		4.0		30	μAdc
			10				8		8.0		60		
			15				16		16.0		120		
MSI	Mil	5	V _{IN} = V _{SS} or V _{DD}				5		5		150	μAdc	
		10			10			10		300			
		15			20			20		600			
MSI	Comm	5			All valid input combinations		20		20		150	μAdc	
		10				40		40		300			
		15				80		80		600			
V _{OL}	Low-Level Output Voltage	All		5 10 15		V _{IN} = V _{SS} or V _{DD} I _O < 1μA	0.05 0.05 0.05		0.05 0.05 0.05		0.05 0.05 0.05	Vdc	
V _{OH}	High-Level Output Voltage	All		5 10 15		V _{IN} = V _{SS} or V _{DD} I _O < 1μA	4.95 9.95 14.95		4.95 9.95 14.95		4.95 9.95 14.95	Vdc	
V _{IL}	Input Low Voltage # B Types	All		5 10 15		V _O = 0.5V or 4.5V V _O = 1.0V or 9.0V V _O = 1.5V or 13.5V I _O < 1μA	1.5 3.0 4.0		1.5 3.0 4.0		1.5 3.0 4.0	Vdc	
V _{IL}	Input Low Voltage # UB Types	All	5 10 15	V _O = 0.5V or 4.5V V _O = 1.0V or 9.0V V _O = 1.5V or 13.5V I _O < 1μA		1.0 2.0 2.5		1.0 2.0 2.5		1.0 2.0 2.5	Vdc		
V _{IH}	Input High Voltage # B Types	All	5 10 15	V _O = 0.5V or 4.5V V _O = 1.0V or 9.0V V _O = 1.5V or 13.5V I _O < 1μA		3.5 7.0 11.0		3.5 7.0 11.0		3.5 7.0 11.0	Vdc		
V _{IH}	Input High Voltage # UB Types	All	5 10 15	V _O = 0.5V or 4.5V V _O = 1.0V or 9.0V V _O = 1.5V or 13.5V I _O < 1μA		4.0 8.0 12.5		4.0 8.0 12.5		4.0 8.0 12.5	Vdc		
I _{OL}	Output Low (Sink) Current	Mil	5	V _O = 0.4V, V _{IN} = 0 or 5V V _O = 0.5V, V _{IN} = 0 or 10V V _O = 1.5V, V _{IN} = 0 or 15V	0.64		0.51		0.36	mAdc			
			10		1.6		1.3		0.9				
			15		4.2		3.4		2.4				
		Com	5		V _O = 0.4V, V _{IN} = 0 or 5V V _O = 0.5V, V _{IN} = 0 or 10V V _O = 1.5V, V _{IN} = 0 or 15V	0.52		0.44		0.36	mAdc		
			10			1.3		1.1		0.9			
			15			3.8		3.0		2.4			

4

TABLE 1 – Continued

ELECTRICAL CHARACTERISTICS

PARAMETER	TEMP RANGE	VDD (Vdc)	CONDITIONS	LIMITS						UNITS		
				T _{LOW} *		+ 25°C		T _{HIGH} *				
				Min	Max	Min	Max	Min	Max			
I _{OH} Output High (Source) Current	Mil	5	V _O = 4.6V, V _{IN} = 0 or 5V	-0.25		-0.2		-0.14		mA _{dc}		
				10	V _O = 9.5V, V _{IN} = 0 or 10V	-0.62		-0.5			-0.35	
						15	V _O = 13.5V, V _{IN} = 0 or 15V	-1.8			-1.5	
	Com	5	V _O = 4.6V, V _{IN} = 0 or 5V	-0.2				-0.16		-0.12		mA _{dc}
				10	V _O = 9.5V, V _{IN} = 0 or 10V	-0.5		-0.4		-0.3		
						15	V _O = 13.5V, V _{IN} = 0 or 15V	-1.4		-1.2		
I _{IN} Input Current	Mil	15	V _{IN} = 0 or 15V		±0.1				±0.1		±1.0	μA _{dc}
				Comm	15	V _{IN} = 0 or 15V		±0.3		±0.3		
I _{oz} 3-State Output Leakage Current	Mil	15	V _{IN} = 0 or 15V		±0.4		±0.4		±12	μA _{dc}		
				Comm	15	V _{IN} = 0 or 15V		±1.6		±1.6	±12	μA _{dc}
C _{IN} Input Capacitance per unit load	All	—	Any Input				7.5			pF		

*T_{LOW} = -55°C for Military temperature range device, -40°C for Commercial temperature range device.

T_{HIGH} = +125°C for Military temperature range device, +85°C for Commercial temperature range device.

#Applies for Worst Case input combinations.



TABLE 2 – MOTOROLA FORMAT FOR CMOS INDUSTRY B AND UB SERIES SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	VDD Vdc	-55°C		25°C		+125°C		Unit	
			Min	Max	Min	Max	Min	Max		
Output Voltage V _{in} = VDD or 0	V _{OL}	5.0	—	0.05	—	0.05	—	0.05	Vdc	
		10	—	0.05	—	0.05	—	0.05		
		15	—	0.05	—	0.05	—	0.05		
V _{in} = 0 or VDD	V _{OH}	5.0	4.95	—	4.95	—	4.95	—	Vdc	
		10	9.95	—	9.95	—	9.95	—		
		15	14.95	—	14.95	—	14.95	—		
Input Voltage B Types (V _O = 4.5 or 0.5 Vdc) (V _O = 9.0 or 1.0 Vdc) (V _O = 13.5 or 1.5 Vdc)	"0" Level	V _{IL}	5.0	—	1.5	—	1.5	—	1.5	Vdc
			10	—	3.0	—	3.0	—	3.0	
			15	—	4.0	—	4.0	—	4.0	
	"1" Level	V _{IH}	5.0	3.5	—	3.5	—	3.5	—	Vdc
			10	7.0	—	7.0	—	7.0	—	
			15	11	—	11	—	11	—	
Input Voltage UB Types (V _O = 4.5 or 0.5 Vdc) (V _O = 9.0 or 1.0 Vdc) (V _O = 13.5 or 1.5 Vdc)	"0" Level	V _{IL}	5.0	—	1.0	—	1.0	—	1.0	Vdc
			10	—	2.0	—	2.0	—	2.0	
			15	—	2.5	—	2.5	—	2.5	
	"1" Level	V _{IH}	5.0	4.0	—	4.0	—	4.0	—	Vdc
			10	8.0	—	8.0	—	8.0	—	
			15	12.5	—	12.5	—	12.5	—	

TABLE 2 – Continued

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V _{DD} Vdc	-55°C		25°C		+125°C		Unit	
			Min	Max	Min	Max	Min	Max		
Output Drive Current B Gates (V _{OH} = 2.5 Vdc) Source (V _{OH} = 4.6 Vdc) (V _{OH} = 9.5 Vdc) (V _{OH} = 13.5 Vdc) (V _{OL} = 0.4 Vdc) Sink (V _{OL} = 0.5 Vdc) (V _{OL} = 1.5 Vdc)	I _{OH}	5.0	-3.0	—	-2.4	—	-1.7	—	mAdc	
		5.0	-0.64	—	-0.51	—	-0.36	—		
		10	-1.6	—	-1.3	—	-0.9	—		
		15	-4.2	—	-3.4	—	-2.4	—		
	I _{OL}	5.0	0.64	—	0.51	—	0.36	—		
		10	1.6	—	1.3	—	0.9	—		
Output Drive Current UB Gates (V _{OH} = 2.5 Vdc) Source (V _{OH} = 4.6 Vdc) (V _{OH} = 9.5 Vdc) (V _{OH} = 13.5 Vdc) (V _{OL} = 0.4 Vdc) Sink (V _{OL} = 0.5 Vdc) (V _{OL} = 1.5 Vdc)	I _{OH}	5.0	-1.2	—	-1.0	—	-0.7	—	mAdc	
		5.0	-0.25	—	-0.2	—	-0.14	—		
		10	-0.62	—	-0.5	—	-0.35	—		
		15	-1.8	—	-1.5	—	-1.1	—		
	I _{OL}	5.0	0.64	—	0.51	—	0.36	—		
		10	1.6	—	1.3	—	0.9	—		
Output Drive Current Other Devices (V _{OH} = 4.6 Vdc) Source (V _{OH} = 9.5 Vdc) (V _{OH} = 13.5 Vdc) (V _{OL} = 0.4 Vdc) Sink (V _{OL} = 0.5 Vdc) (V _{OL} = 1.5 Vdc)	I _{OH}	5.0	-0.64	—	-0.51	—	-0.36	—	mAdc	
		10	-1.6	—	-1.3	—	-0.9	—		
		15	-4.2	—	-3.4	—	-2.4	—		
		I _{OL}	5.0	0.64	—	0.51	—	0.36		—
	10		1.6	—	1.3	—	0.9	—		
	Input Current	I _{in}	15	—	±0.1	—	±0.1	—		±1.0
Input Capacitance (V _{in} = 0)										
C _{in}			—	—	—	—	7.5	—	—	pF
Gate Quiescent Current (Per Package)	I _{DD}	5.0	—	0.25	—	0.25	—	7.5	μAdc	
		10	—	0.5	—	0.5	—	15		
		15	—	1.0	—	1.0	—	30		
Flip-Flop and Buffer Quiescent Current (Per Package)	I _{DD}	5.0	—	1.0	—	1.0	—	30	μAdc	
		10	—	2.0	—	2.0	—	60		
		15	—	4.0	—	4.0	—	120		
MSI Quiescent Current (Per Package)	I _{DD}	5.0	—	5.0	—	5.0	—	150	μAdc	
		10	—	10	—	10	—	300		
		15	—	20	—	20	—	600		
LSI Quiescent Current	I _{DD}	See Individual Data Sheets.								



CMOS Handling and Design Guidelines



HANDLING AND DESIGN GUIDELINES

HANDLING PRECAUTIONS

All MOS devices have insulated gates that are subject to voltage breakdown. The gate oxide for Motorola CMOS devices is about 900 Å thick and breaks down at a gate-source potential of about 100 volts. To guard against such a breakdown from static discharge or other voltage transients, the protection networks shown in Figures 1A and 1B are used on each input to the CMOS device.

Static damaged devices behave in various ways, depending on the severity of the damage. The most severely damaged inputs are the easiest to detect because the input has been completely destroyed and is either shorted to V_{DD} , shorted to V_{SS} , or open-circuited. The effect is that the device no longer responds to signals present at the damaged input. Less severe cases are more difficult to detect because they show up as intermittent failures or as degraded performance. Another effect of static damage is that the inputs generally have increased leakage currents.

Although the input protection network does provide a great deal of protection, CMOS devices are not immune to large static voltage discharges that can be generated during handling. For example, static voltages generated by a person walking across a waxed floor have been measured in the 4-15 kV range (depending on humidity, surface conditions, etc.). Therefore, the following precautions should be observed:

1. Do not exceed the Maximum Ratings specified by the data sheet.
2. All unused device inputs should be connected to V_{DD} or V_{SS} .
3. All low-impedance equipment (pulse generators, etc.) should be connected to CMOS inputs only after the device is powered up. Similarly, this type of equipment should be disconnected before power is turned off.
4. Circuit boards containing CMOS devices are merely extensions of the devices, and the same handling precautions apply. Contacting edge connectors wired directly to device inputs can cause damage. Plastic wrapping should be avoided. When external connections to a PC board are connected to an input of a CMOS device, a resistor should be used in series with the input. This resistor helps limit accidental damage if the PC board is removed and brought into contact with static generating materials. The limiting factor for the series resistor is the added delay. This is caused by the time constant formed by the series resistor and

input capacitance. Note that the maximum input rise and fall times should not be exceeded. In Figure 2, two possible networks are shown using a series resistor to reduce ESD (Electrostatic Discharge) damage. For convenience, an equation for added propagation delay and rise time effects due to series resistance size is given.

5. All CMOS devices should be stored or transported in materials that are antistatic. CMOS devices must not be inserted into conventional plastic "snow", styrofoam, or plastic trays, but should be left in their original container until ready for use.
6. All CMOS devices should be placed on a grounded bench surface and operators should ground themselves prior to handling devices, since a worker can be statically charged with respect to the bench surface. Wrist straps in contact with skin are strongly recommended. See Figure 3 for an example of a typical work station.
7. Nylon or other static generating materials should not come in contact with CMOS devices.
8. If automatic handlers are being used, high levels of static electricity may be generated by the movement of the device, the belts, or the boards. Reduce static build-up by using ionized air blowers or room humidifiers. All parts of machines which come into contact with the top, bottom, or sides of IC packages must be grounded to metal or other conductive material.
9. Cold chambers using CO_2 for cooling should be equipped with baffles, and the CMOS devices must be contained on or in conductive material.
10. When lead-straightening or hand-soldering is necessary, provide ground straps for the apparatus used and be sure that soldering ties are grounded.
11. The following steps should be observed during wave solder operations:
 - a. The solder pot and conductive conveyor system of the wave soldering machine must be grounded to an earth ground.
 - b. The loading and unloading work benches should have conductive tops which are grounded to an earth ground.
 - c. Operators must comply with precautions previously explained.
 - d. Completed assemblies should be placed in antistatic containers prior to being moved to subsequent stations.

INPUT PROTECTION NETWORK

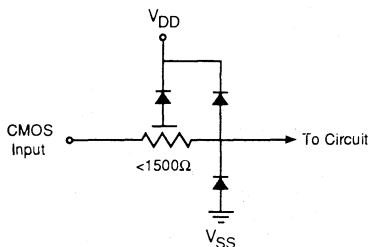


FIGURE 1A — INPUT PROTECTION NETWORK
Double Diode

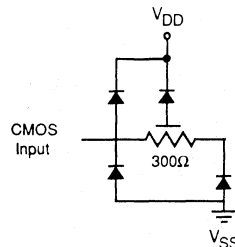


FIGURE 1B — INPUT PROTECTION NETWORK
Triple Diode

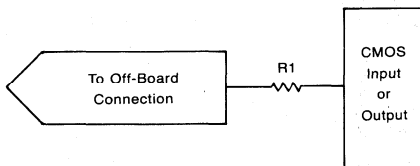
12. The following steps should be observed during board-cleaning operations:
 - a. Vapor degreasers and baskets must be grounded to an earth ground.
 - b. Brush or spray cleaning should not be used.
 - c. Assemblies should be placed into the vapor degreaser immediately upon removal from the antistatic container.
 - d. Cleaned assemblies should be placed in antistatic containers immediately after removal from the cleaning basket.
 - e. High velocity air movement or application of solvents and coatings should be employed only when assembled printed circuit boards are grounded and a static eliminator is directed at the board.
13. The use of static detection meters for production line surveillance is highly recommended.
14. Equipment specifications should alert users to the presence of CMOS devices and require familiarization with this specification prior to performing any kind of maintenance or replacement of devices or modules.
15. Do not insert or remove CMOS devices from test sockets with power applied. Check all power supplies to be used for testing devices to be certain there are no voltage transients present.
16. Double check test equipment setup for proper polarity of V_{DD} and V_{SS} before conducting parametric or functional testing.
17. Do not recycle shipping rails or trays. Repeated use causes deterioration of their antistatic coating.

RECOMMENDED FOR READING:

"Total Control of the Static in Your Business"

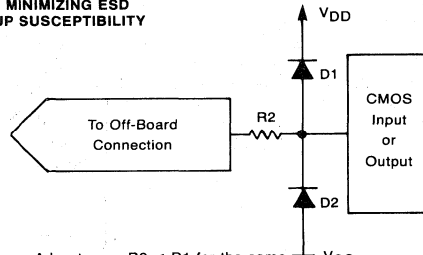
Available by writing to:
 3M Company
 Static Control Systems
 P.O. Box 2963
 Austin, Texas 78769-2963
 Or by Calling:
 1-800-328-1368

FIGURE 2 — NETWORKS FOR MINIMIZING ESD AND REDUCING CMOS LATCH UP SUSCEPTIBILITY



Advantage: Requires minimal board area

Disadvantage: $R1 > R2$ for the same level of protection, therefore rise and fall times, propagation delays, and output drives are severely affected.



Advantage: $R2 < R1$ for the same level of protection. Impact on ac and dc characteristics is minimized

Disadvantage: More board area, higher initial cost

Note: These networks are useful for protecting the following
 A digital inputs and outputs C 3-state outputs
 B analog inputs and outputs D bidirectional (I/O) ports

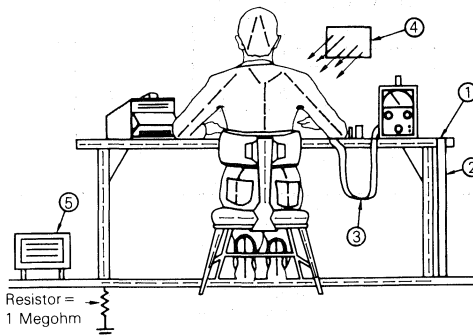
PROPAGATION DELAY AND RISE TIME vs. SERIES RESISTANCE

$$R = \frac{t}{C \cdot k}$$

where:

- R = the maximum allowable series resistance in ohms
- t = the maximum tolerable propagation delay or rise time in seconds
- C = the board capacitance plus the driven device's input capacitance in farads
- k = 0.7 for propagation delay calculations
- k = 2.3 for rise time calculations

FIGURE 3 — TYPICAL MANUFACTURING WORK STATION



- NOTES:
1. 1/16 inch conductive sheet stock covering bench top work area.
 2. Ground strap.
 3. Wrist strap in contact with skin.
 4. Static neutralizer. (ionized air blower directed at work.) Primarily for use in areas where direct grounding is impractical.
 5. Room humidifier. Primarily for use in areas where the relative humidity is less than 45%. Caution: building heating and cooling systems usually dry the air causing the relative humidity inside of buildings to be less than outside humidity.

POWER SUPPLIES

CMOS devices have low power requirements and the ability to operate over a wide range of supply voltages. These two characteristics allow CMOS designs to be implemented using inexpensive, conventional power supplies, instead of switching power supplies and power supplies with cooling fans. In addition, batteries may be used as either a primary power source or for emergency backup.

The *absolute* maximum power supply voltage for 14000 Series Metal-gate CMOS is 18.0 Vdc. Figure 4 offers some insight as to how this specification was derived. In the figure, V_S is the maximum power supply voltage and I_S is the sustaining current of the latch-up mode. The value of V_S was chosen so that the secondary breakdown effect may be avoided.

In an ideal system design, a power supply should be designed to deliver only enough current to insure proper operation of all devices. The obvious benefit of this type design is cost savings; an added benefit is protection

against the possibility of latch-up related failures. This system protection can be provided by the power supply filter and/or voltage regulator.

CMOS devices can be used with battery or battery backup systems. A few precautions should be taken when designing battery-operated systems:

1. The recommended power supply voltage should be observed. For battery backup systems such as the one in Figure 5, the battery voltage must be at least 3.7 Volts (3 Volts from the minimum power supply voltage and 0.7 Volts to account for the voltage drop across the series diode).
2. Inputs that might go above the battery backup voltage should either use a series resistor to limit the input current to less than 10 mA or use the MC14049UB or MC14050B high-to-low voltage translators.
3. Outputs that are subject to voltage levels above V_{DD} or below V_{SS} should be protected with a series resistor to limit the current to less than 10 mA or with clamping diodes.

FIGURE 4 — SECONDARY BREAKDOWN CHARACTERISTICS

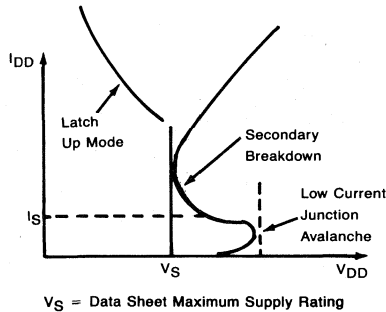
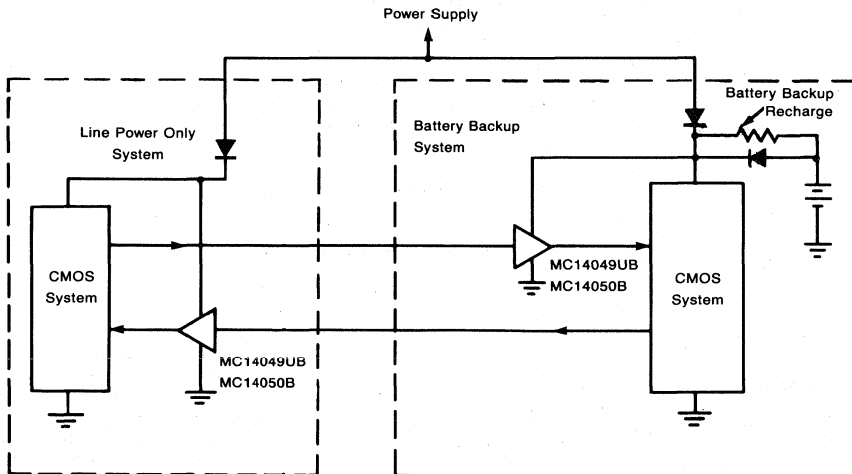


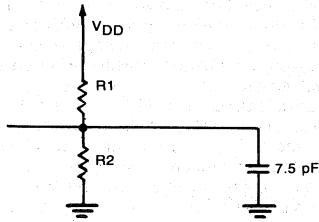
FIGURE 5 — BATTERY BACKUP INTERFACE



INPUTS

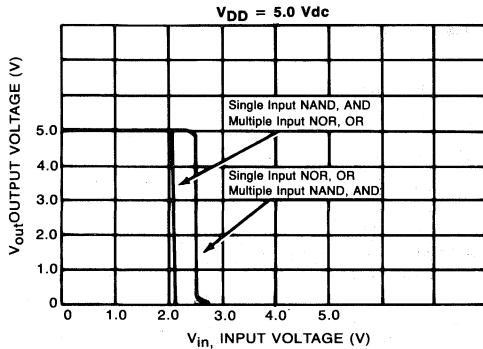
All inputs, while in the recommended operating range ($V_{SS} < V_{in} < V_{DD}$) can be modeled as shown in Figure 6. For input voltages in this range, diodes D1 and D2 are modeled as resistors, representing the reverse bias impedance of the diodes. The maximum input current is worst case, $1\mu\text{A}$, when the inputs are at V_{DD} or V_{SS} , and $V_{DD} = 15.0\text{ V}$. This model does not apply to inputs with pull-up or pull-down resistors.

FIGURE 6 — INPUT MODEL FOR $V_{SS} \leq V_{in} \leq V_{DD}$



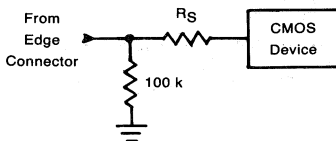
When left open-circuited, the inputs may self-bias at or near the typical switchpoint, where both the P-channel and N-channel transistors are conducting, causing excessive current drain. Due to the high gain of the inverters (see Figure 7), the device may also go into oscillation from any noise in the system. Since CMOS devices dissipate the most power during switching, this oscillation can cause very large current drain and undesired switching.

FIGURE 7 — TYPICAL TRANSFER CHARACTERISTICS FOR BUFFERED DEVICES



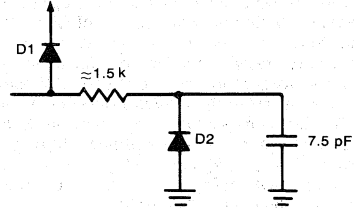
For these reasons, all unused inputs should be connected either to V_{DD} or V_{SS} . For applications with inputs going to edge connectors, a 100 kilohm resistor to V_{SS} should be used, as well as a series resistor for static protection and current limiting (Figure 8). The 100 kilohm resistor will help eliminate any static charges that might develop on the printed circuit board. See Figure 2 for other possible protection arrangements.

FIGURE 8 — EXTERNAL PROTECTION



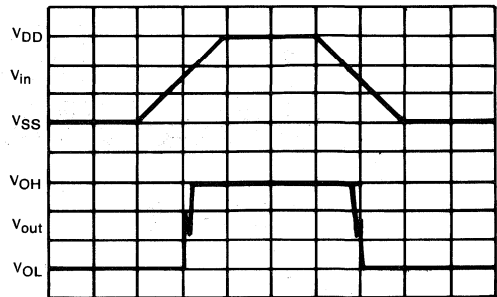
For input voltages outside of the recommended operating range, the CMOS input is modeled as in Figure 9. The resistor-diode protection network allows the user greater freedom when designing a worst case system. The device inputs are guaranteed to withstand voltages from $V_{SS} - 0.5\text{ V}$ to $V_{DD} + 0.5\text{ V}$ and a maximum current of 10 mA . With the above input ratings, most designs will require no special terminations or design considerations.

FIGURE 9 — INPUT MODEL FOR $V_{in} > V_{DD}$ or $V_{in} < V_{SS}$



Other specifications that should be noted are the maximum input rise and fall times. Figure 10 shows the oscillations that may result from exceeding the $15\mu\text{s}$ maximum rise and fall time at $V_{DD} = 5.0\text{ V}$, $5\mu\text{s}$ at 10 V , or $4\mu\text{s}$ at 15 V . As the voltage passes through the switching threshold region with a slow rise time, any noise that is on the input is amplified, and passed through to the output, causing oscillations. The oscillation may have a low enough frequency to cause succeeding stages to switch, giving unexpected results. If input rise or fall times are expected to exceed $15\mu\text{s}$ at 5.0 V , $5\mu\text{s}$ at 10 V , or $4\mu\text{s}$ at 15 V , Schmitt-trigger devices such as the MC14093B, MC14583B, MC14584B, MC14106B, HC14, or HC132 are recommended for squaring-up these slow transitions.

FIGURE 10 — MAXIMUM RISE AND FALL TIME VIOLATIONS



OUTPUTS

All CMOS B-Series outputs are buffered to insure consistent output voltage and current performance. All buffered outputs have guaranteed output voltages of $V_{OL} = 0.05 \text{ V}$ and $V_{OH} = V_{DD} - 0.05 \text{ V}$ for $V_{in} = V_{DD}$ or V_{SS} and $I_{out} = 0 \mu\text{A}$. The output drives for all buffered CMOS devices are such that 1 LSTTL load can be driven across the full temperature range.

CMOS outputs are limited to externally forced output voltages of $V_{SS} - 0.5 \text{ V} \leq V_{out} \leq V_{DD} + 0.5 \text{ V}$. When voltages are forced outside of this range, a silicon controlled rectifier (SCR) formed by parasitic transistors can be triggered, causing the device to latch up. For more information on this, see the explanation of CMOS Latch Up in this section.

The maximum rated output current for most outputs is 10 mA. The output short-circuit currents of these devices typically exceed these limits. Care must be taken not to exceed the maximum ratings found on every data sheet.

For applications that require driving high capacitive loads where fast propagation delays are needed (e.g., driving power MOSFETs), two or more outputs on the same chip may be externally paralleled.

CMOS LATCH UP

Latch up will not be a problem for most designs, but the designer should be aware of it, what causes it, and how to prevent it.

Figure 11 shows the cross-section of a typical CMOS inverter and Figure 12 shows the parasitic bipolar devices. The circuit formed by the parasitic transistors and resistors is the basic configuration of a silicon controlled rectifier, or SCR. In the latch up condition, transistors Q1 and Q2 are turned ON, each providing the base current necessary for the other to remain in saturation, thereby latching

the devices in the ON state. Unlike a conventional SCR, where the device is turned ON by applying a voltage to the base of the NPN transistor, the parasitic SCR is turned ON by applying a voltage to the emitter of either transistor. The two emitters that trigger the SCR are the same point, the CMOS output. Therefore, to latch up the CMOS device, the output voltage must be greater than $V_{DD} + 0.5 \text{ V}$ or less than $V_{SS} - 0.5 \text{ V}$ and have sufficient current to trigger the SCR. The latch-up mechanism is similar for the inputs.

Once a CMOS device is latched up, if the supply current is not limited, the device will be destroyed. Ways to prevent such occurrences are listed below:

1. Insure that inputs and outputs are limited to the maximum rated values, as follows:
 $-0.5 \text{ V} \leq V_{in} \text{ or } V_{out} \leq V_{DD} + 0.5 \text{ V}$ (referenced to V_{SS})
 $|I_{in} \text{ or } I_{out}| \leq 10 \text{ mA}$ (unless otherwise indicated on the data sheet)
2. If voltage transients of sufficient energy to latch up the device are expected on the inputs or outputs, external protection diodes can be used to clamp the voltage. Another method of protection is to use a series resistor to limit the expected worst case current to the maximum rating of 10 mA. (See Figure 2).
3. Sequence power supplies so that the inputs or outputs of CMOS devices are not active before the supply pins are powered up (e.g., recessed edge connectors and/or series resistors may be used in plug-in board applications).
4. Voltage regulating or filtering should be used in board design and layout to insure that power-supply lines are free of excessive noise.
5. Limit the available power supply current to the devices that are subject to latch-up conditions. This can be accomplished with the power supply filtering network or with a current-limiting regulator.

FIGURE 11 — CMOS WAFER CROSS SECTION

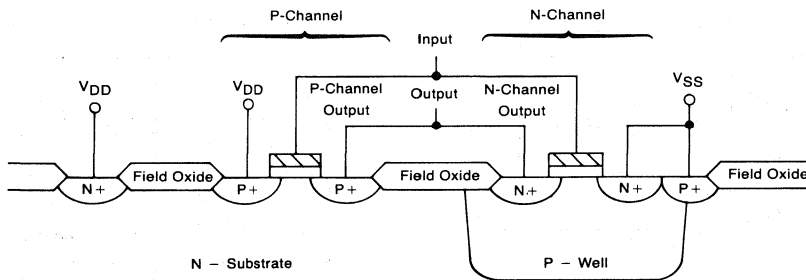
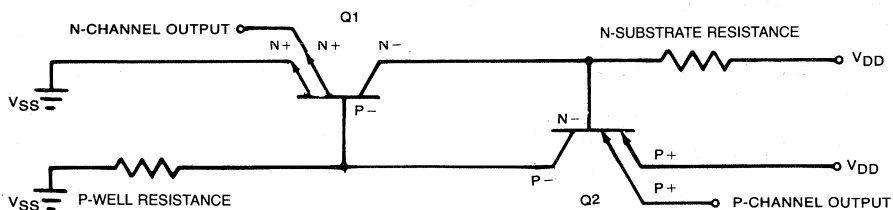


FIGURE 12 — LATCH UP CIRCUIT SCHEMATIC



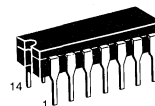


MC14000UB

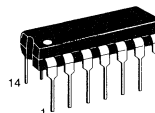
DUAL 3-INPUT "NOR" GATE PLUS INVERTER

The MC14000UB dual 3-input NOR gate plus inverter is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These complementary MOS logic gates find primary use where low power dissipation and/or high noise immunity is desired.

- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Logic Swing Independent of Fanout
- Pin-for-Pin Replacement for CD4000UB



L SUFFIX
CERAMIC
CASE 632



P SUFFIX
PLASTIC
CASE 646



D SUFFIX
SOIC
CASE 751A

ORDERING INFORMATION

MC14XXXUBCP Plastic
MC14XXXUBCL Ceramic
MC14XXXUBD SOIC

$T_A = -55^\circ$ to 125°C for all packages.

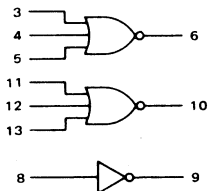
MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	-0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	-0.5 to $V_{DD} + 0.5$	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	± 10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	-65 to +150	$^\circ\text{C}$
T_L	Lead Temperature (8-Second Soldering)	260	$^\circ\text{C}$

*Maximum Ratings are those values beyond which damage to the device may occur.

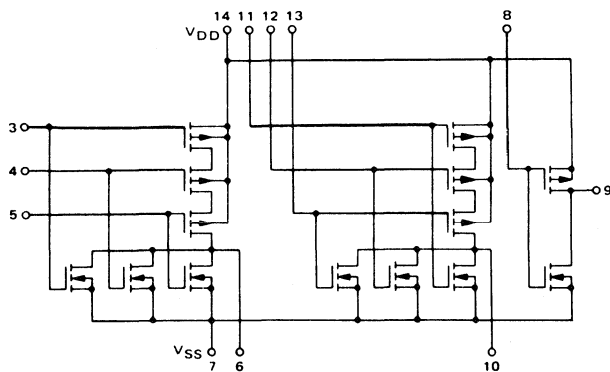
†Temperature Derating: Plastic "P and D/DW" Packages: -7.0 mW/ $^\circ\text{C}$ From 65 $^\circ\text{C}$ To 125 $^\circ\text{C}$
Ceramic "L" Packages: -12 mW/ $^\circ\text{C}$ From 100 $^\circ\text{C}$ To 125 $^\circ\text{C}$

LOGIC DIAGRAM

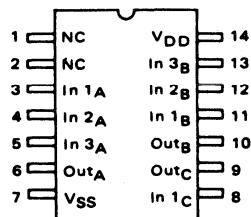


V_{DD} = Pin 14
 V_{SS} = Pin 7

CIRCUIT SCHEMATIC



PIN ASSIGNMENT



NC = NO CONNECTION

MC14000UB

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V _{DD} Vdc	55°C		25°C			+125°C		Unit	
			Min	Max	Min	Typ #	Max	Min	Max		
Output Voltage V _{in} = V _{DD} or 0	"0" Level V _{OL}	5.0	—	0.05	—	0	0.05	—	0.05	Vdc	
		10	—	0.05	—	0	0.05	—	0.05		
		15	—	0.05	—	0	0.05	—	0.05		
	"1" Level V _{in} = 0 or V _{DD}	V _{OH}	5.0	4.95	—	4.95	5.0	—	4.95		—
			10	9.95	—	9.95	10	—	9.95		—
			15	14.95	—	14.95	15	—	14.95		—
Input Voltage (V _O = 4.5 Vdc) (V _O = 9.0 Vdc) (V _O = 13.5 Vdc)	"0" Level V _{IL}	5.0	—	1.0	—	2.25	1.0	—	1.0	Vdc	
		10	—	2.0	—	4.50	2.0	—	2.0		
		15	—	2.5	—	6.75	2.5	—	2.5		
	"1" Level (V _O = 0.5 Vdc) (V _O = 1.0 Vdc) (V _O = 1.5 Vdc)	V _{IH}	5.0	4.0	—	4.0	2.75	—	4.0		—
			10	8.0	—	8.0	5.50	—	8.0		—
			15	12.5	—	12.5	8.25	—	12.5		—
Output Drive Current (V _{OH} = 2.5 Vdc) (V _{OH} = 4.6 Vdc) (V _{OH} = 9.5 Vdc) (V _{OH} = 13.5 Vdc)	Source I _{OH}	5.0	-1.2	—	-1.0	-1.7	—	-0.7	—	mAdc	
		5.0	-0.25	—	-0.2	-0.36	—	-0.14	—		
		10	-0.62	—	-0.5	-0.9	—	-0.35	—		
	Sink I _{OL}	5.0	0.64	—	0.51	0.88	—	0.36	—		
			10	1.6	—	1.3	2.25	—	0.9		—
			15	4.2	—	3.4	8.8	—	2.4		—
Input Current	I _{in}	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	μAdc	
Input Capacitance (V _{in} = 0)	C _{in}	—	—	—	—	5.0	7.5	—	—	pF	
Quiescent Current (Per Package)	I _{DD}	5.0	—	0.25	—	0.0005	0.25	—	7.5	μAdc	
		10	—	0.5	—	0.0010	0.5	—	15		
		15	—	1.0	—	0.0015	1.0	—	30		
Total Supply Current**† (Dynamic plus Quiescent, Per Gate, C _L = 50 pF)	I _T	5.0	I _T = (0.3 μA/kHz) f + I _{DD} /N							μAdc	
		10	I _T = (0.6 μA/kHz) f + I _{DD} /N								
		15	I _T = (0.8 μA/kHz) f + I _{DD} /N								

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) V/k$$

where: I_T is in μH (per package), C_L in pF, V = (V_{DD} - V_{SS}) in volts, f in kHz is input frequency, and k = 0.001 × the number of exercised gates per package.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range V_{SS} ≤ (V_{in} or V_{out}) ≤ V_{DD}. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

MC14000UB

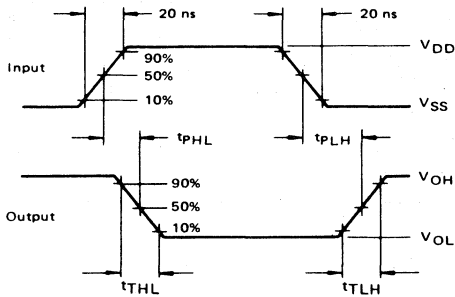
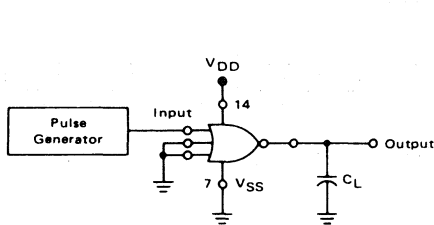
SWITCHING CHARACTERISTICS* ($C_L = 50 \text{ pF}$, $T_A = 25^\circ\text{C}$)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ #	Max	Unit
Output Rise Time $t_{TLH} = (3.0 \text{ ns/pF}) C_L + 30 \text{ ns}$ $t_{TLH} = (1.5 \text{ ns/pF}) C_L + 15 \text{ ns}$ $t_{TLH} = (1.1 \text{ ns/pF}) C_L + 10 \text{ ns}$	t_{TLH}	5.0 10 15	— — —	180 90 65	360 180 130	ns
Output Fall Time $t_{THL} = (1.5 \text{ ns/pF}) C_L + 25 \text{ ns}$ $t_{THL} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$ $t_{THL} = (0.55 \text{ ns/pF}) C_L + 9.5 \text{ ns}$	t_{THL}	5.0 10 15	— — —	100 50 40	200 100 80	ns
Propagation Delay Time $t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 30 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 22 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.50 \text{ ns/pF}) C_L + 15 \text{ ns}$	t_{PLH}, t_{PHL}	5.0 10 15	— — —	115 55 40	230 110 80	ns

*The formulas given are for the typical characteristics only at 25°C .

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

FIGURE 1 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



6

FIGURE 2 – TYPICAL VOLTAGE AND CURRENT TRANSFER CHARACTERISTICS

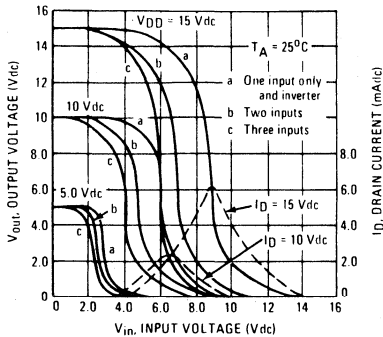
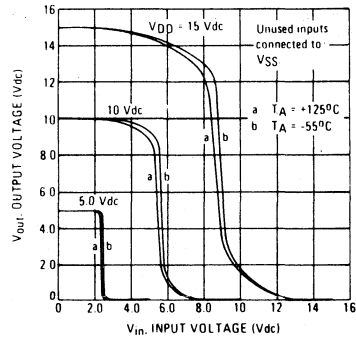


FIGURE 3 – TYPICAL VOLTAGE TRANSFER CHARACTERISTICS versus TEMPERATURE



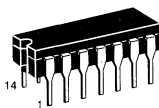


MOTOROLA

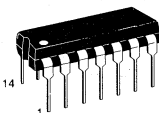
B-SUFFIX SERIES CMOS GATES

The B Series logic gates are constructed with P and N channel enhancement mode devices in a single monolithic structure (Complementary MOS). Their primary use is where low power dissipation and/or high noise immunity is desired.

- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- All Outputs Buffered
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range.
- Double Diode Protection on All Inputs Except: Triple Diode Protection on MC14011B and MC14081B
- Pin-for-Pin Replacements for Corresponding CD4000 Series B Suffix Devices (Exceptions: MC14068B and MC14078B)



L SUFFIX
CERAMIC
CASE 632



P SUFFIX
PLASTIC
CASE 646



D SUFFIX
SOIC
CASE 751A

ORDERING INFORMATION

- MC14XXXBCP Plastic
- MC14XXXBCL Ceramic
- MC14XXXBD SOIC

T_A = -55° to 125°C for all packages.

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V _{DD}	DC Supply Voltage	-0.5 to +18.0	V
V _{in} , V _{out}	Input or Output Voltage (DC or Transient)	-0.5 to V _{DD} +0.5	V
I _{in} , I _{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
P _D	Power Dissipation, per Package†	500	mW
T _{stg}	Storage Temperature	-65 to +150	°C
T _L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P and D/DW" Packages: -7.0 mW/°C From 65°C To 125°C
Ceramic "L" Packages: -12 mW/°C From 100°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range V_{SS} ≤ (V_{in} or V_{out}) ≤ V_{DD}. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

MC14001B
Quad 2-Input NOR Gate

MC14002B
Dual 4-Input Nor Gate

MC14011B
Quad 2-Input NAND Gate

MC14012B
Dual 4-Input NAND Gate

MC14023B
Triple 3-Input NAND Gate

MC14025B
Triple 3-Input NOR Gate

MC14068B
8-Input NAND Gate

MC14071B
Quad 2-Input OR Gate

MC14072B
Dual 4-Input OR Gate

MC14073B
Triple 3-Input AND Gate

MC14075B
Triple 3-Input OR Gate

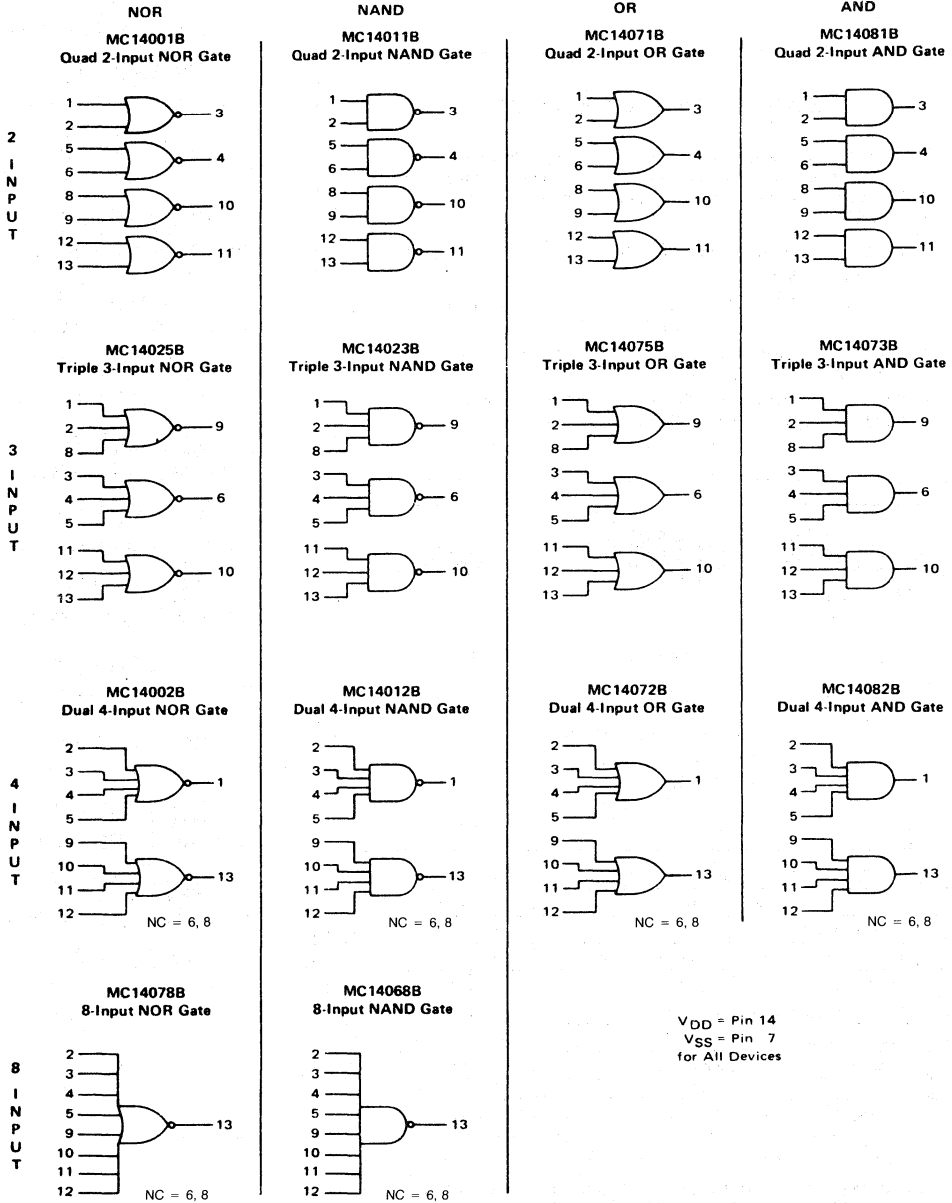
MC14078B
8-Input NOR Gate

MC14081B
Quad 2-Input AND Gate

MC14082B
Dual 4-Input AND Gate

CMOS B-SERIES GATES

LOGIC DIAGRAMS

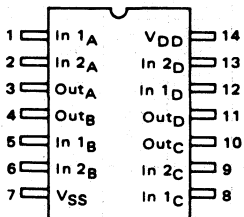


6

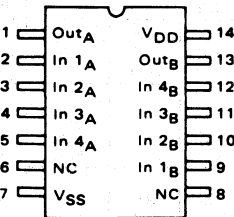
CMOS B-SERIES GATES

PIN ASSIGNMENTS

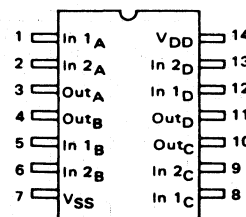
MC14001B
Quad 2-Input NOR Gate



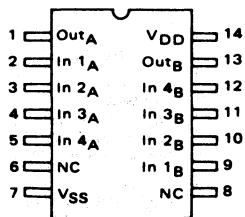
MC14002B
Dual 4-Input NOR Gate



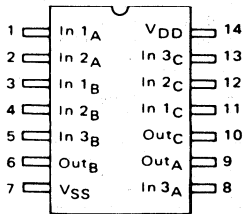
MC14011B
Quad 2-Input NAND Gate



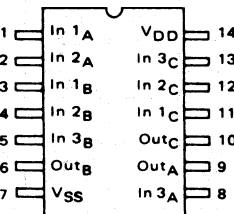
MC14012B
Dual 4-Input NAND Gate



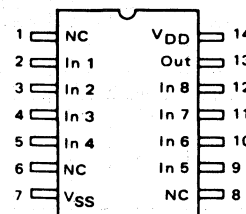
MC14023B
Triple 3-Input NAND Gate



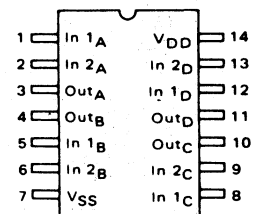
MC14025B
Triple 3-Input NOR Gate



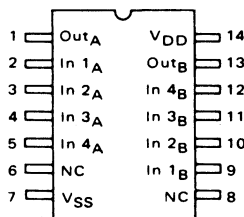
MC14068B
8-Input NAND Gate



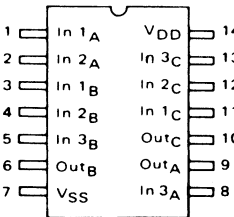
MC14071B
Quad 2-Input OR Gate



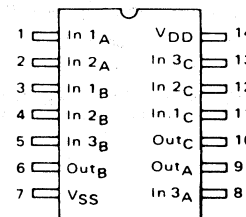
MC14072B
Dual 4-Input OR Gate



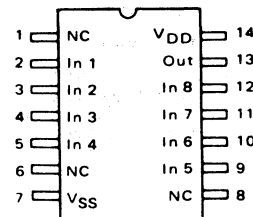
MC14073B
Triple 3-Input AND Gate



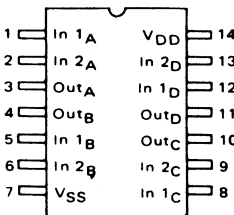
MC14075B
Triple 3-Input OR Gate



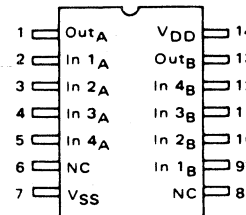
MC14078B
8-Input NOR Gate



MC14081B
Quad 2-Input AND Gate



MC14082B
Dual 4-Input AND Gate



NC = No Connection

CMOS B-SERIES GATES

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	-55°C		25°C			125°C		Unit	
			Min	Max	Min	Typ #	Max	Min	Max		
Output Voltage $V_{in} = V_{DD}$ or 0	"0" Level V_{OL}	5.0	—	0.05	—	0	0.05	—	0.05	Vdc	
		10	—	0.05	—	0	0.05	—	0.05		
		15	—	0.05	—	0	0.05	—	0.05		
	"1" Level $V_{in} = 0$ or V_{DD}	V_{OH}	5.0	4.95	—	4.95	5.0	—	4.95		—
			10	9.95	—	9.95	10	—	9.95		—
			15	14.95	—	14.95	15	—	14.95		—
Input Voltage ($V_O = 4.5$ or 0.5 Vdc) ($V_O = 9.0$ or 1.0 Vdc) ($V_O = 13.5$ or 1.5 Vdc)	"0" Level V_{IL}	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc	
		10	—	3.0	—	4.50	3.0	—	3.0		
		15	—	4.0	—	6.75	4.0	—	4.0		
	"1" Level ($V_O = 0.5$ or 4.5 Vdc) ($V_O = 1.0$ or 9.0 Vdc) ($V_O = 1.5$ or 13.5 Vdc)	V_{IH}	5.0	3.5	—	3.5	2.75	—	3.5		—
			10	7.0	—	7.0	5.50	—	7.0		—
			15	11	—	11	8.25	—	11		—
Output Drive Current ($V_{OH} = 2.5$ Vdc) ($V_{OH} = 4.6$ Vdc) ($V_{OH} = 9.5$ Vdc) ($V_{OH} = 13.5$ Vdc)	Source I_{OH}	5.0	-3.0	—	-2.4	-4.2	—	-1.7	—	mAdc	
		10	-0.64	—	-0.51	-0.88	—	-0.36	—		
		15	-1.6	—	-1.3	-2.25	—	-0.9	—		
	Sink I_{OL}	5.0	0.64	—	0.51	0.88	—	0.36	—		
			10	1.6	—	1.3	2.25	—	0.9		—
			15	4.2	—	3.4	8.8	—	2.4		—
Input Current	I_{in}	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	μAdc	
Input Capacitance ($V_{in} = 0$)	C_{in}	—	—	—	—	5.0	7.5	—	—	pF	
Quiescent Current (Per Package)	I_{DD}	5.0	—	0.25	—	0.0005	0.25	—	7.5	μAdc	
		10	—	0.5	—	0.0010	0.5	—	15		
		15	—	1.0	—	0.0015	1.0	—	30		
Total Supply Current**† (Dynamic plus Quiescent, Per Gate, $C_L = 50$ pF)	I_T	5.0	$I_T = (0.3 \mu A/kHz) f + I_{DD}/N$							μAdc	
		10	$I_T = (0.6 \mu A/kHz) f + I_{DD}/N$								
		15	$I_T = (0.9 \mu A/kHz) f + I_{DD}/N$								

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) V/k$$

where: I_T is in μA (per package), C_L in pF, $V = (V_{DD} - V_{SS})$ in volts, f in kHz is input frequency, and $k = 0.001 \times$ the number of exercised gates per package.

CMOS B-SERIES GATES

B-SERIES GATE SWITCHING TIMES

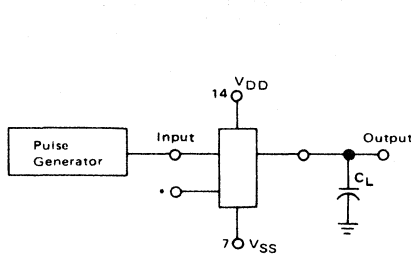
SWITCHING CHARACTERISTICS* ($C_L = 50 \text{ pF}$, $T_A = 25^\circ \text{C}$)

Characteristic	Symbol	V _{DD} V _{dC}	Min	Typ #	Max	Unit
Output Rise Time, All B-Series Gates $t_{TLH} = (1.35 \text{ ns/pF}) C_L + 33 \text{ ns}$ $t_{TLH} = (0.60 \text{ ns/pF}) C_L + 20 \text{ ns}$ $t_{TLH} = (0.40 \text{ ns/pF}) C_L + 20 \text{ ns}$	t_{TLH}	5.0 10 15	— — —	100 50 40	200 100 80	ns
Output Fall Time, All B-Series Gates $t_{THL} = (1.35 \text{ ns/pF}) C_L + 33 \text{ ns}$ $t_{THL} = (0.60 \text{ ns/pF}) C_L + 20 \text{ ns}$ $t_{THL} = (0.40 \text{ ns/pF}) C_L + 20 \text{ ns}$	t_{THL}	5.0 10 15	— — —	100 50 40	200 100 80	ns
Propagation Delay Time MC14001B, MC14011B only $t_{PLH}, t_{PHL} = (0.90 \text{ ns/pF}) C_L + 80 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.36 \text{ ns/pF}) C_L + 32 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.26 \text{ ns/pF}) C_L + 27 \text{ ns}$ All Other 2, 3, and 4 Input Gates $t_{PLH}, t_{PHL} = (0.90 \text{ ns/pF}) C_L + 115 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.36 \text{ ns/pF}) C_L + 47 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.26 \text{ ns/pF}) C_L + 37 \text{ ns}$ 8-Input Gates (MC14068B, MC14078B) $t_{PLH}, t_{PHL} = (0.90 \text{ ns/pF}) C_L + 155 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.36 \text{ ns/pF}) C_L + 62 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.26 \text{ ns/pF}) C_L + 47 \text{ ns}$	t_{PLH}, t_{PHL}	5.0 10 15 5.0 10 15 5.0 10 15	— — — — — — — — —	125 50 40 160 65 50 200 80 60	250 100 80 300 130 100 350 150 110	ns

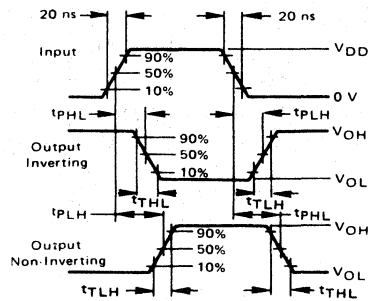
*The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

FIGURE 1 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



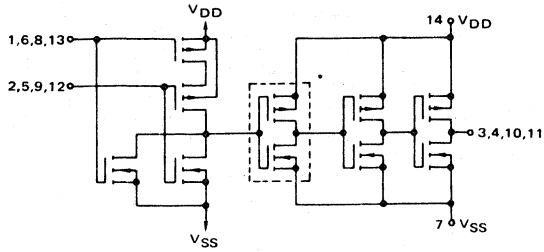
*All unused inputs of AND, NAND gates must be connected to V_{DD}.
 All unused inputs of OR, NOR gates must be connected to V_{SS}.



CMOS B-SERIES GATES

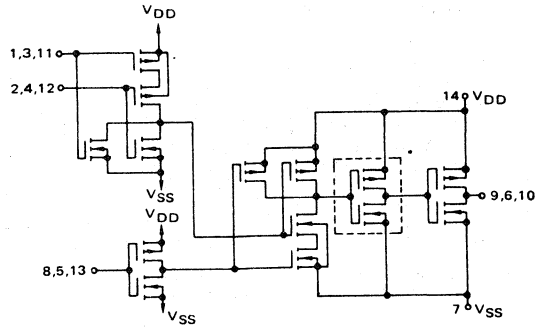
CIRCUIT SCHEMATIC NOR, OR Gates

MC14001B
MC14071B
One of Four
Gates Shown



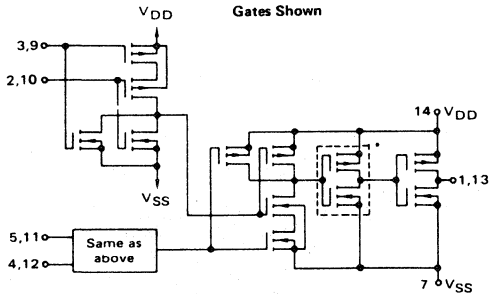
*Inverter Omitted in MC14001B

MC14025B
MC14075B
One of Three
Gates Shown



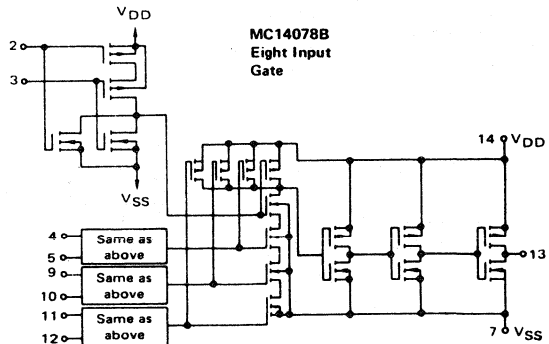
*Inverter Omitted in MC14025B

MC14002B
MC14072B
One of Two
Gates Shown



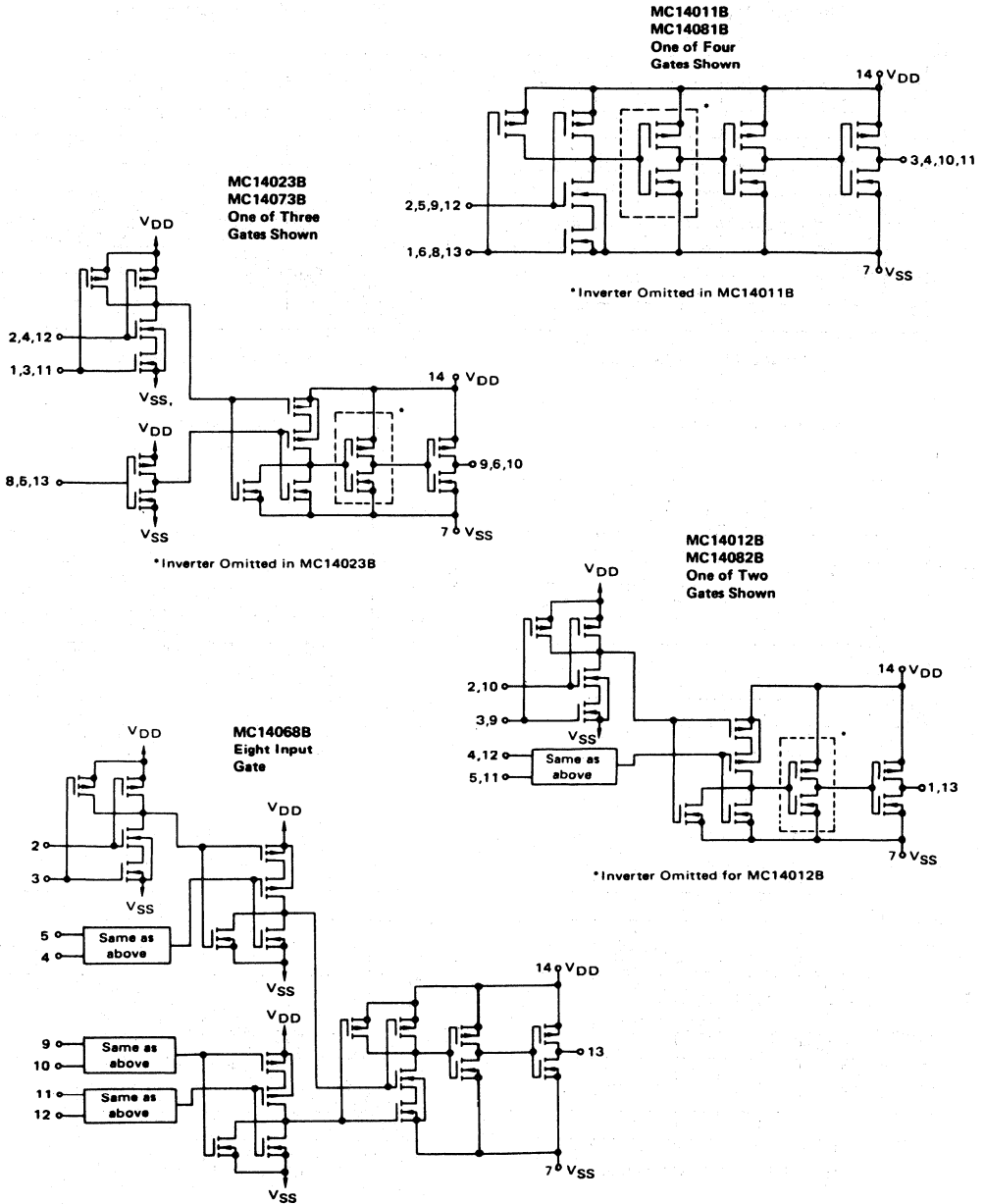
*Inverter Omitted in MC14002B

MC14078B
Eight Input
Gate



CMOS B-SERIES GATES

CIRCUIT SCHEMATICS NAND, AND Gates

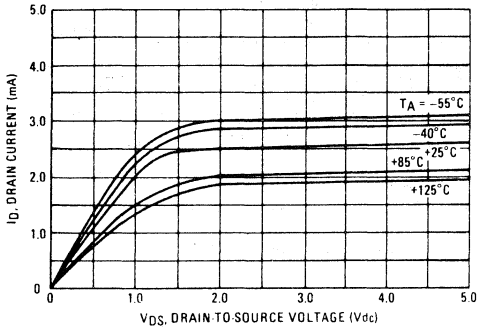


CMOS B-SERIES GATES

TYPICAL B-SERIES GATE CHARACTERISTICS

N-CHANNEL DRAIN CURRENT (SINK)

FIGURE 2 – $V_{GS} = 5.0$ Vdc



P-CHANNEL DRAIN CURRENT (SOURCE)

FIGURE 3 – $V_{GS} = -5.0$ Vdc

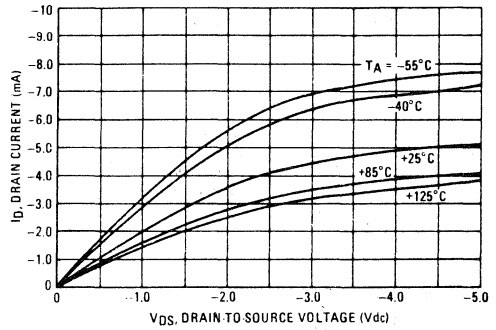


FIGURE 4 – $V_{GS} = 10$ Vdc

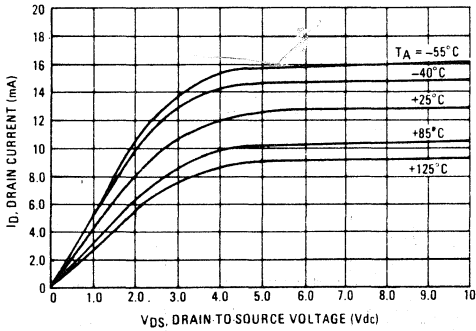


FIGURE 5 – $V_{GS} = -10$ Vdc

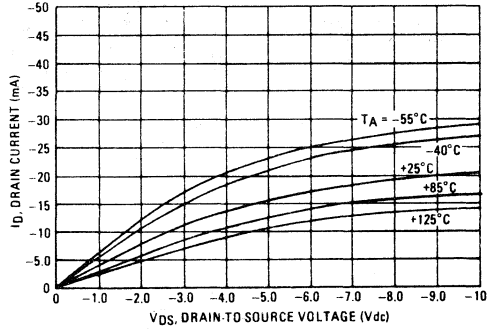


FIGURE 6 – $V_{GS} = 15$ Vdc

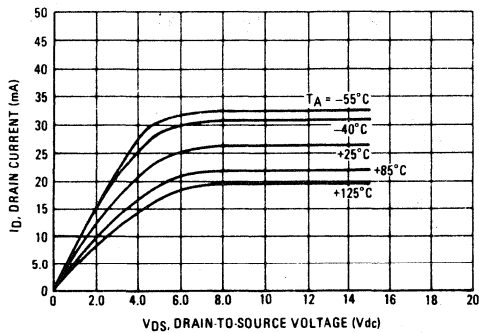
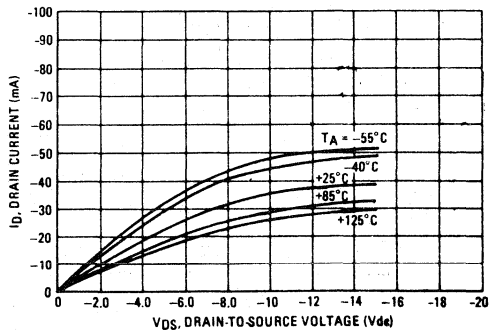


FIGURE 7 – $V_{GS} = -15$ Vdc



These typical curves are not guarantees, but are design aids.
Caution: The maximum rating for output current is 10 mA per pin.

CMOS B-SERIES GATES

TYPICAL B-SERIES GATE CHARACTERISTICS (cont'd)

VOLTAGE TRANSFER CHARACTERISTICS

FIGURE 8 - $V_{DD} = 5.0 \text{ Vdc}$

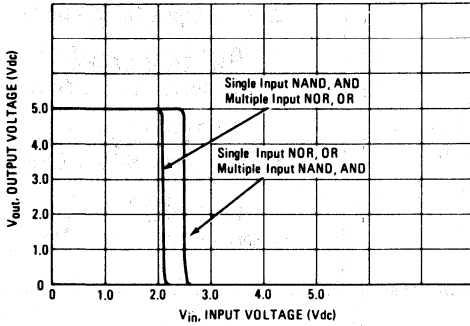


FIGURE 9 - $V_{DD} = 10 \text{ Vdc}$

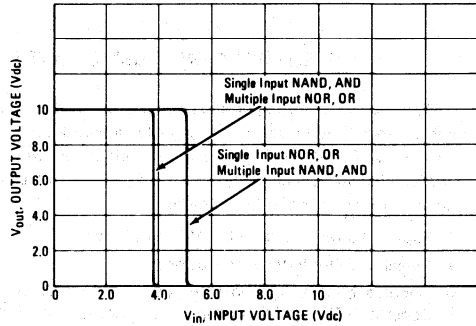
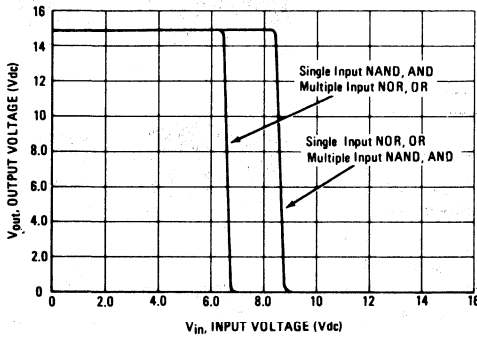


FIGURE 10 - $V_{DD} = 15 \text{ Vdc}$



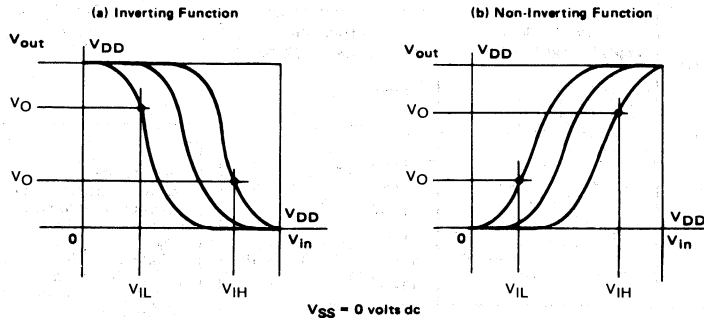
DC NOISE MARGIN

The DC noise margin is defined as the input voltage range from an ideal "1" or "0" input level which does not produce output state change(s). The typical and guaranteed limit values of the input values V_{IL} and V_{IH} for the output(s) to be at a fixed voltage V_O are given in the Electrical Characteristics table. V_{IL} and V_{IH} are presented graphically in Figure 11.

Guaranteed minimum noise margins for both the "1" and "0" levels =

- 1.0 V with a 5.0 V supply
- 2.0 V with a 10.0 V supply
- 2.5 V with a 15.0 V supply

FIGURE 11 - DC NOISE IMMUNITY





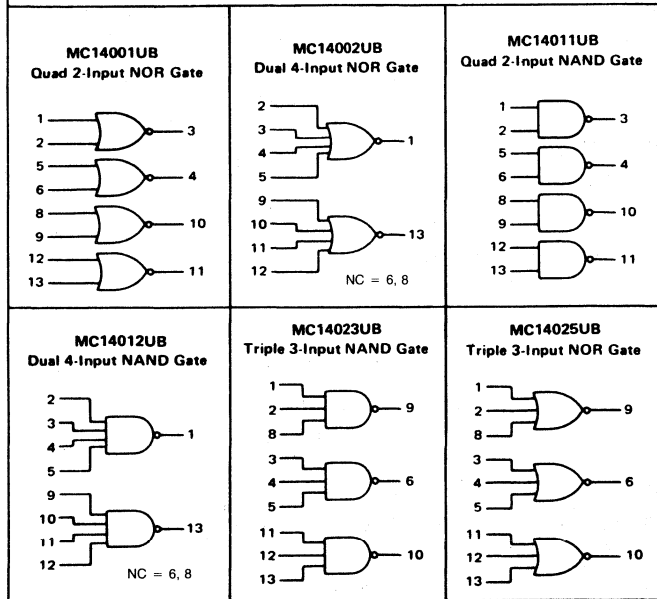
MOTOROLA

UB-SUFFIX SERIES CMOS GATES

The UB Series logic gates are constructed with P and N channel enhancement mode devices in a single monolithic structure (Complementary MOS). Their primary use is where low power dissipation and/or high noise immunity is desired. The UB set of CMOS gates are inverting non-buffered functions.

- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Linear and Oscillator Applications
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range.
- Double Diode Protection on All Inputs
- Pin-for-Pin Replacements for Corresponding CD4000 Series UB Suffix Devices

LOGIC DIAGRAMS



V_{DD} = Pin 14
V_{SS} = Pin 7
for All Devices

MC14001UB
Quad 2-Input NOR Gate

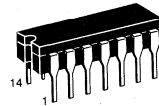
MC14002UB
Dual 4-Input NOR Gate

MC14011UB
Quad 2-Input NAND Gate

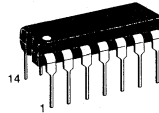
MC14012UB
Dual 4-Input NAND Gate

MC14023UB
Triple 3-Input NAND Gate

MC14025UB
Triple 3-Input NOR Gate



L SUFFIX
CERAMIC
CASE 632



P SUFFIX
PLASTIC
CASE 646



D SUFFIX
SOIC
CASE 751A

ORDERING INFORMATION

MC14XXXUBCP Plastic
MC14XXXUBCL Ceramic
MC14XXXUBD SOIC

T_A = -55° to 125°C for all packages.

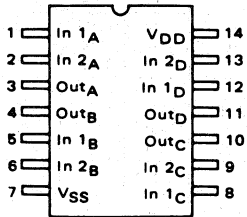
This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range V_{SS} ≤ (V_{IN} or V_{OUT}) ≤ V_{DD}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

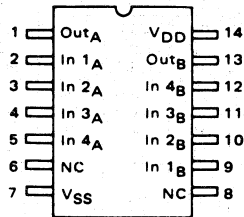
CMOS UB-SERIES GATES

PIN ASSIGNMENTS

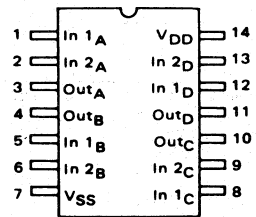
MC14001UB
Quad 2-Input NOR Gate



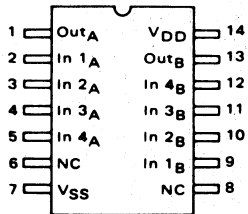
MC14002UB
Dual 4-Input NOR Gate



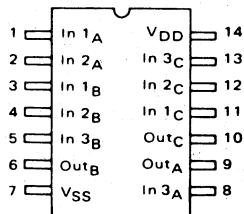
MC14011UB
Quad 2-Input NAND Gate



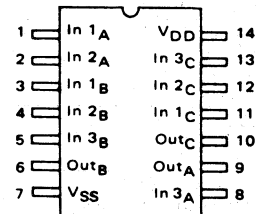
MC14012UB
Dual 4-Input NAND Gate



MC14023UB
Triple 3-Input NAND Gate



MC14025UB
Triple 3-Input NOR Gate



NC = No Connection

6

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V _{DD}	DC Supply Voltage	-0.5 to +18.0	V
V _{in} , V _{out}	Input or Output Voltage (DC or Transient)	-0.5 to V _{DD} + 0.5	V
I _{in} , I _{out}	Input or Output Current (DC or Transient), per Pin	± 10	mA
P _D	Power Dissipation, per Package†	500	mW
T _{stg}	Storage Temperature	-65 to +150	°C
T _L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.

†Temperature Derating: Plastic "P and D/DW" Packages: -7.0 mW/°C From 65°C To 125°C

Ceramic "L" Packages: -12 mW/°C From 100°C To 125°C

CMOS UB-SERIES GATES

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V _{DD} Vdc	-55°C		25°C			125°C		Unit
			Min	Max	Min	Typ #	Max	Min	Max	
Output Voltage V _{in} = V _{DD} or 0	V _{OL}	5.0 10 15	—	0.05	—	0	0.05	—	0.05	Vdc
			—	0.05	—	0	0.05	—	0.05	
—			0.05	—	0	0.05	—	0.05		
V _{in} = 0 or V _{DD}	V _{OH}	5.0 10 15	4.95	—	4.95	5.0	—	4.95	—	Vdc
			9.95	—	9.95	10	—	9.95	—	
			14.95	—	14.95	15	—	14.95	—	
Input Voltage (V _O = 4.5 Vdc) (V _O = 9.0 Vdc) (V _O = 13.5 Vdc)	V _{IL}	5.0 10 15	—	1.0	—	2.25	1.0	—	1.0	Vdc
			—	2.0	—	4.50	2.0	—	2.0	
—			2.5	—	6.75	2.5	—	2.5		
(V _O = 0.5 Vdc) (V _O = 1.0 Vdc) (V _O = 1.5 Vdc)	V _{IH}	5.0 10 15	4.0	—	4.0	2.75	—	4.0	—	Vdc
			8.0	—	8.0	5.50	—	8.0	—	
			12.5	—	12.5	8.25	—	12.5	—	
Output Drive Current (V _{OH} = 2.5 Vdc) (V _{OH} = 4.6 Vdc) (V _{OH} = 9.5 Vdc) (V _{OH} = 13.5 Vdc)	Source	I _{OH}	5.0	-1.2	—	-1.0	-1.7	—	-0.7	mAdc
			5.0	-0.25	—	-0.2	-0.36	—	-0.14	
10			-0.62	—	-0.5	-0.9	—	-0.35		
(V _{OL} = 0.4 Vdc) (V _{OL} = 0.5 Vdc) (V _{OL} = 1.5 Vdc)	Sink	I _{OL}	5.0	0.64	—	0.51	0.88	—	0.36	mAdc
			10	1.6	—	1.3	2.25	—	0.9	
			15	4.2	—	3.4	8.8	—	2.4	
Input Current	I _{in}	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	μAdc
Input Capacitance (V _{in} = 0)	C _{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)	I _{DD}	5.0 10 15	— — —	0.25 0.5 1.0	— — —	0.0005 0.0010 0.0015	0.25 0.5 1.0	— — —	7.5 15 30	μAdc
Total Supply Current**† (Dynamic plus Quiescent, Per Gate, C _L = 50 pF)	I _T	5.0 10 15	I _T = (0.3 μA/kHz) f + I _{DD} /N I _T = (0.6 μA/kHz) f + I _{DD} /N I _T = (0.8 μA/kHz) f + I _{DD} /N							μAdc

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) V/k$$

where: I_T is in μH (per package), C_L in pF, V = (V_{DD} - V_{SS}) in volts, f in kHz is input frequency, and k = 0.001 × the number of exercised gates per package.

CMOS UB-SERIES GATES

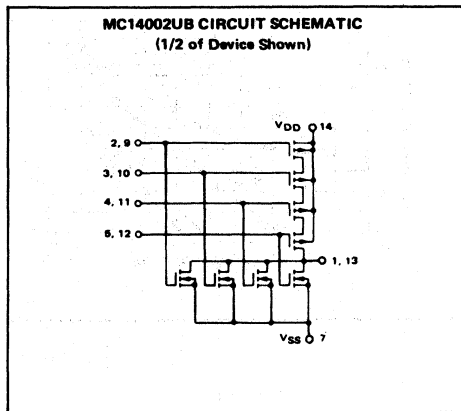
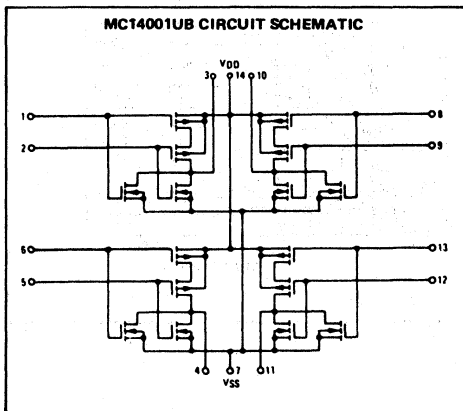
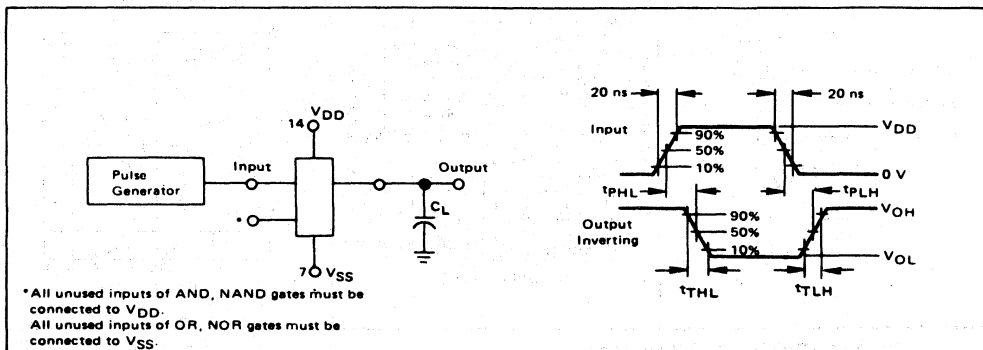
SWITCHING CHARACTERISTICS* ($C_L = 50 \text{ pF}$, $T_A = 25^\circ\text{C}$)

Characteristic	Symbol	VDD Vdc	Min	Typ #	Max	Unit
Output Rise Time $t_{TLH} = (3.0 \text{ ns/pF}) C_L + 30 \text{ ns}$ $t_{TLH} = (1.5 \text{ ns/pF}) C_L + 15 \text{ ns}$ $t_{TLH} = (1.1 \text{ ns/pF}) C_L + 10 \text{ ns}$	t_{TLH}	5.0 10 15	— — —	180 90 65	360 180 130	ns
Output Fall Time $t_{THL} = (1.5 \text{ ns/pF}) C_L + 25 \text{ ns}$ $t_{THL} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$ $t_{THL} = (0.55 \text{ ns/pF}) C_L + 9.5 \text{ ns}$	t_{THL}	5.0 10 15	— — —	100 50 40	200 100 80	ns
Propagation Delay Time $t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 30 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 22 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.50 \text{ ns/pF}) C_L + 15 \text{ ns}$	t_{PLH}, t_{PHL}	5.0 10 15	— — —	90 50 40	180 100 80	ns

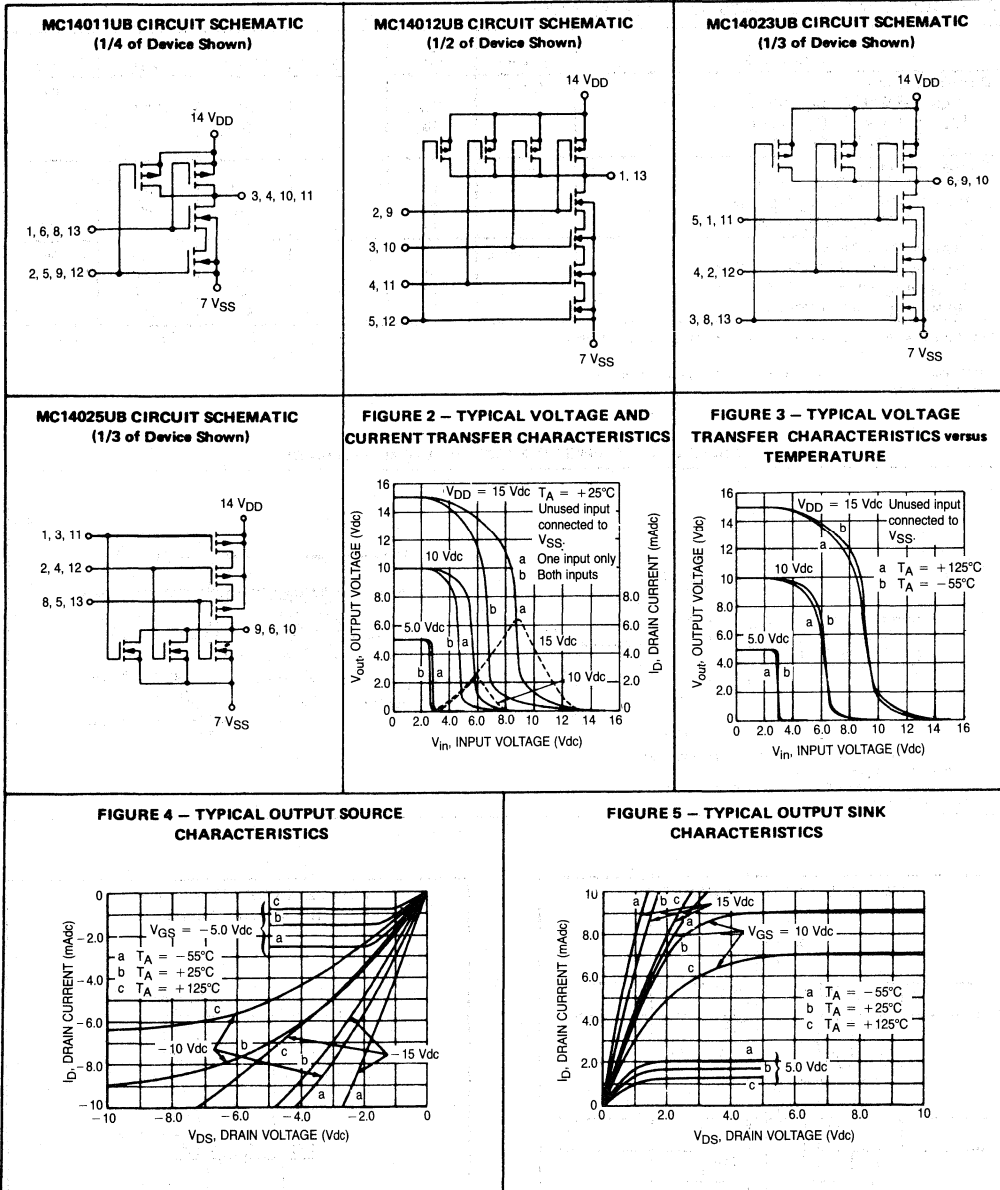
*The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

FIGURE 1 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



CMOS UB-SERIES GATES



6



MOTOROLA

MC14002B
See Page 6-5

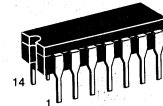
MC14002UB
See Page 6-14

MC14006B

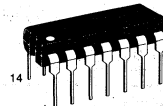
18-BIT STATIC SHIFT REGISTER

The MC14006B shift register is comprised of four separate shift register sections sharing a common clock: two sections have four stages, and two sections have five stages with an output tap on both the fourth and fifth stages. This makes it possible to obtain a shift register of 4, 5, 8, 9, 10, 12, 13, 14, 16, 17, or 18 bits by appropriate selection of inputs and outputs. This part is particularly useful in serial shift registers and time delay circuits.

- Output Transitions Occur on the Falling Edge of the Clock Pulse
- Fully Static Operation
- Can be Cascaded to Provide Longer Shift Register Lengths
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range
- Pin-for-Pin Replacement for CD4006B



L SUFFIX
CERAMIC
CASE 632



P SUFFIX
PLASTIC
CASE 646



D SUFFIX
SOIC
CASE 751A

ORDERING INFORMATION

- MC14XXXBCP Plastic
- MC14XXXBCL Ceramic
- MC14XXXBD SOIC

T_A = -55° to 125°C for all packages.

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V _{DD}	DC Supply Voltage	-0.5 to +18.0	V
V _{in} , V _{out}	Input or Output Voltage (DC or Transient)	-0.5 to V _{DD} + 0.5	V
I _{in} , I _{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
P _D	Power Dissipation, per Package†	500	mW
T _{stg}	Storage Temperature	-65 to +150	°C
T _L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.

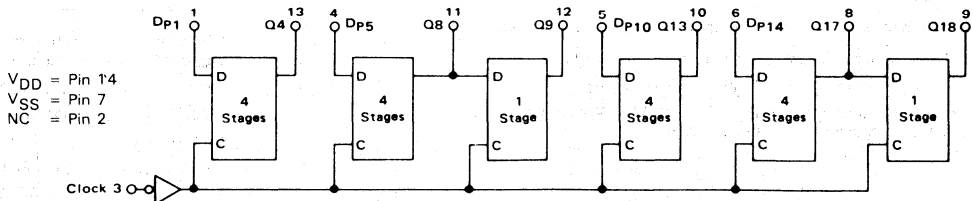
†Temperature Derating: Plastic "P" and D/DW" Packages: -7.0 mW/°C From 65°C To 125°C
Ceramic "L" Packages: -12 mW/°C From 100°C To 125°C

TRUTH TABLE
(Single Stage)

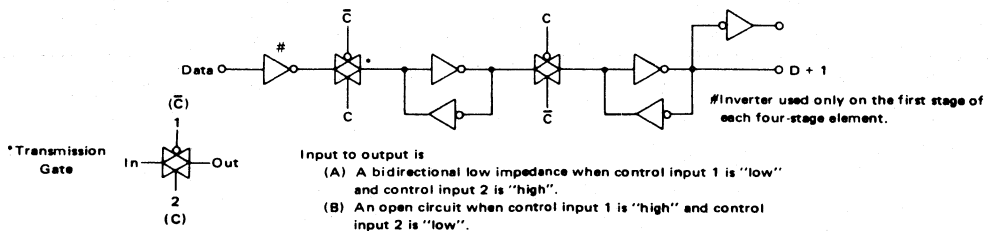
D _n	C	Q _{n+1}
0		0
1		1
X		Q _n

X = Don't Care

BLOCK DIAGRAM



LOGIC DIAGRAM
(ONE REGISTER STAGE)



MC14006B

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V _{DD} V _{dC}	-55°C		25°C			125°C		Unit	
			Min	Max	Min	Typ #	Max	Min	Max		
Output Voltage V _{in} = V _{DD} or 0	V _{OL}	5.0	—	0.05	—	0	0.05	—	0.05	V _{dC}	
		10	—	0.05	—	0	0.05	—	0.05		
15		—	0.05	—	0	0.05	—	0.05			
V _{in} = 0 or V _{DD}	V _{OH}	5.0	4.95	—	4.95	5.0	—	4.95	—	V _{dC}	
		10	9.95	—	9.95	10	—	9.95	—		
		15	14.95	—	14.95	15	—	14.95	—		
Input Voltage (V _O = 4.5 or 0.5 V _{dC}) (V _O = 9.0 or 1.0 V _{dC}) (V _O = 13.5 or 1.5 V _{dC})	V _{IL}	5.0	—	1.5	—	2.25	1.5	—	1.5	V _{dC}	
		10	—	3.0	—	4.50	3.0	—	3.0		
15		—	4.0	—	6.75	4.0	—	4.0			
(V _O = 0.5 or 4.5 V _{dC}) (V _O = 1.0 or 9.0 V _{dC}) (V _O = 1.5 or 13.5 V _{dC})	V _{IH}	5.0	3.5	—	3.5	2.75	—	3.5	—	V _{dC}	
		10	7.0	—	7.0	5.50	—	7.0	—		
		15	11	—	11	8.25	—	11	—		
Output Drive Current (V _{OH} = 2.5 V _{dC}) (V _{OH} = 4.6 V _{dC}) (V _{OH} = 9.5 V _{dC}) (V _{OH} = 13.5 V _{dC})	Source	I _{OH}	5.0	-3.0	—	-2.4	-4.2	—	-1.7	—	mA _{dC}
			5.0	-0.64	—	-0.51	-0.88	—	-0.36	—	
	10		-1.6	—	-1.3	-2.25	—	-0.9	—		
	15		-4.2	—	-3.4	-8.8	—	-2.4	—		
(V _{OL} = 0.4 V _{dC}) (V _{OL} = 0.5 V _{dC}) (V _{OL} = 1.5 V _{dC})	Sink	I _{OL}	5.0	0.64	—	0.51	0.88	—	0.36	—	mA _{dC}
	10		1.6	—	1.3	2.25	—	0.9	—		
	15		4.2	—	3.4	8.8	—	2.4	—		
Input Current	I _{in}	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	μA _{dC}	
Input Capacitance (V _{in} = 0)	C _{in}	—	—	—	—	5.0	7.5	—	—	pF	
Quiescent Current (Per Package)	I _{DD}	5.0	—	5.0	—	0.005	5.0	—	150	μA _{dC}	
		10	—	10	—	0.010	10	—	300		
		15	—	20	—	0.015	20	—	600		
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C _L = 50 pF on all outputs, all buffers switching)	I _T	5.0	I _T = (1.3 μA/kHz) f + I _{DD} I _T = (2.6 μA/kHz) f + I _{DD} I _T = (3.9 μA/kHz) f + I _{DD}						μA _{dC}		
	10										
	15										

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

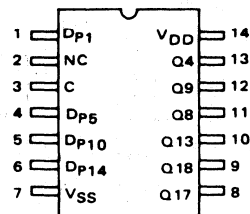
**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) V/fk$$

where: I_T is in μA (per package), C_L in pF, V = (V_{DD} - V_{SS}) in volts, f in kHz is input frequency, and k = 0.001.

PIN ASSIGNMENT



NC = No Connection

MC14006B

SWITCHING CHARACTERISTICS* ($C_L = 50 \text{ pF}$, $T_A = 25^\circ\text{C}$)

Characteristic	Symbol	V_{DD}	Min	Typ #	Max	Unit
Output Rise and Fall Time $t_{TLH}, t_{THL} = (1.5 \text{ ns/pF}) C_L + 25 \text{ ns}$ $t_{TLH}, t_{THL} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$ $t_{TLH}, t_{THL} = (0.55 \text{ ns/pF}) C_L + 9.5 \text{ ns}$	t_{TLH} , t_{THL}	5.0	—	100	200	ns
		10	—	50	100	
		15	—	40	80	
		—	—	—	—	
Propagation Delay Time $t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 220 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 77 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 55 \text{ ns}$	t_{PLH} , t_{PHL}	5.0	—	300	600	ns
		10	—	110	220	
		15	—	80	160	
		—	—	—	—	
Clock Pulse Width	t_{WH}	5.0	200	100	—	ns
		10	120	60	—	
		15	80	40	—	
Clock Pulse Frequency	f_{cl}	5.0	—	5.0	2.5	MHz
		10	—	8.3	4.2	
		15	—	12	6.0	
Clock Pulse Rise and Fall Time**	t_{TLH} , t_{THL}	5.0	—	—	15	μs
		10	—	—	5	
		15	—	—	4	
Setup Time	t_{su}	5.0	0	-50	—	ns
		10	0	-15	—	
		15	0	-8.0	—	
Hold Time	t_h	5.0	180	75	—	ns
		10	90	25	—	
		15	75	20	—	

*The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**When shift register sections are cascaded, the maximum rise and fall times of the clock input should be equal to or less than the rise and fall times of the data outputs driving data inputs, plus the propagation delay of the output driving stage for the output capacitance load.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

FIGURE 1 – TYPICAL OUTPUT SOURCE CURRENT CHARACTERISTICS TEST CIRCUIT

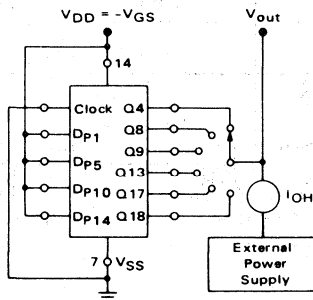
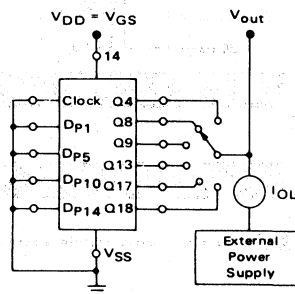


FIGURE 2 – TYPICAL OUTPUT SINK CURRENT CHARACTERISTICS TEST CIRCUIT



MC14006B

FIGURE 3 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

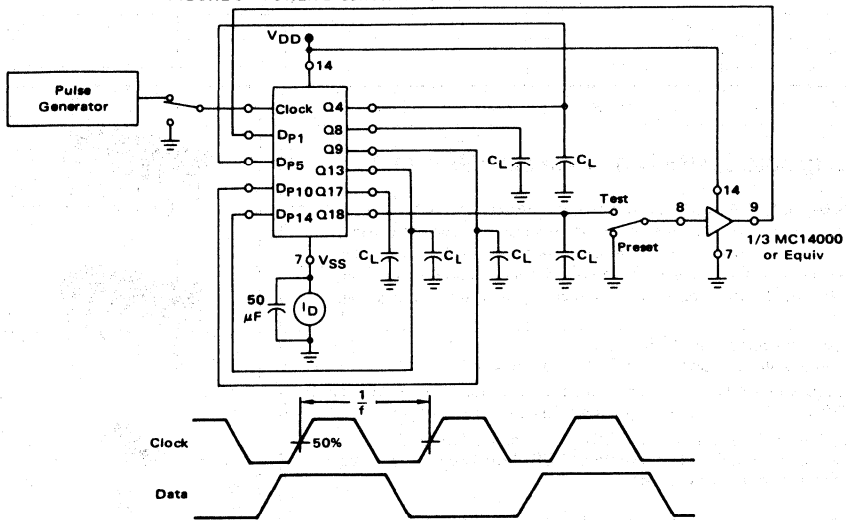
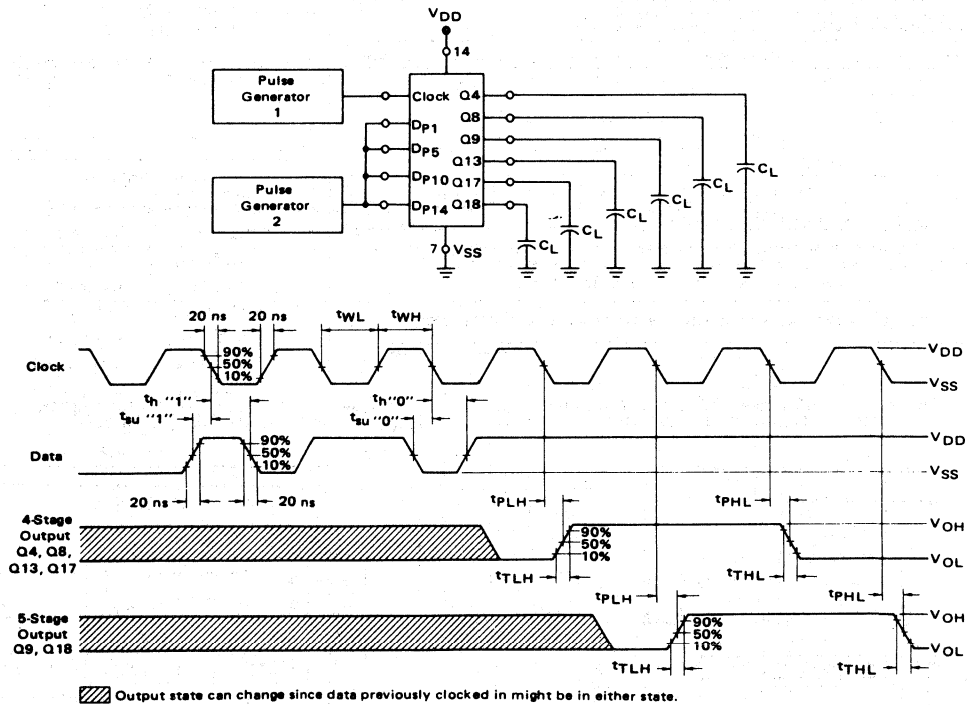


FIGURE 4 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS





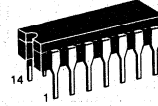
MOTOROLA

MC14007UB

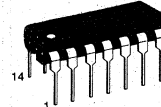
DUAL COMPLEMENTARY PAIR PLUS INVERTER

The MC14007UB multi-purpose device consists of three N-channel and three P-channel enhancement mode devices packaged to provide access to each device. These versatile parts are useful in inverter circuits, pulse-shapers, linear amplifiers, high input impedance amplifiers, threshold detectors, transmission gating, and functional gating.

- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range
- Pin-for-Pin Replacement for CD4007A or CD4007UB
- This device has 2 outputs without ESD Protection. Anti-static precautions must be taken.



L SUFFIX
CERAMIC
CASE 632



P SUFFIX
PLASTIC
CASE 646



D SUFFIX
SOIC
CASE 751A

ORDERING INFORMATION

- MC14XXXUBCP Plastic
- MC14XXXUBCL Ceramic
- MC14XXXUBD SOIC

T_A = -55° to 125°C for all packages.

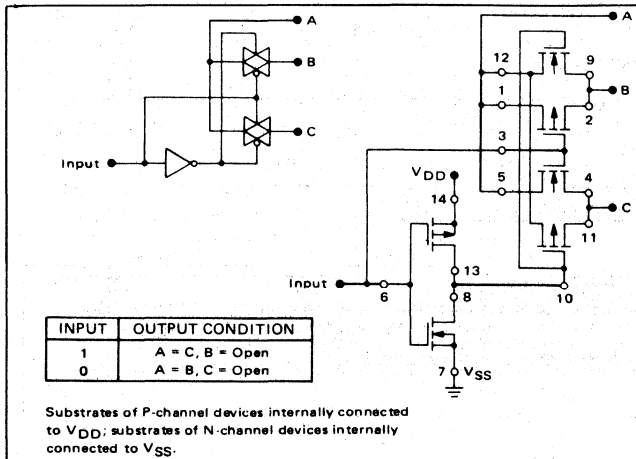
MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V _{DD}	DC Supply Voltage	-0.5 to +18.0	V
V _{in} , V _{out}	Input or Output Voltage (DC or Transient)	-0.5 to V _{DD} + 0.5	V
I _{in} , I _{out}	Input or Output Current (DC or Transient), per Pin	± 10	mA
P _D	Power Dissipation, per Package†	500	mW
T _{stg}	Storage Temperature	-65 to +150	°C
T _L	Lead Temperature (8-Second Soldering)	260	°C

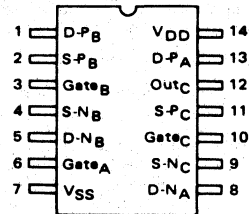
*Maximum Ratings are those values beyond which damage to the device may occur.

†Temperature Derating: Plastic "P and D/DW" Packages: -7.0 mW/°C From 65°C To 125°C
Ceramic "L" Packages: -12 mW/°C From 100°C To 125°C

FIGURE 1 — TYPICAL APPLICATION: 2-INPUT ANALOG MULTIPLEXER

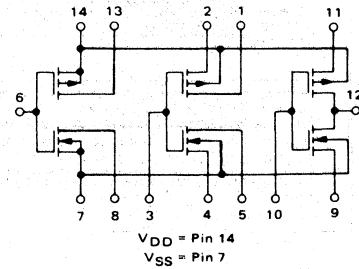


PIN ASSIGNMENT



D = Drain
S = Source

SCHEMATIC



MC14007UB

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V _{DD} Vdc	-55°C		25°C			125°C		Unit		
			Min	Max	Min	Typ #	Max	Min	Max			
Output Voltage V _{in} = V _{DD} or 0	V _{OL}	5.0 10 15	—	0.05	—	0	0.05	—	0.05	Vdc		
			—	0.05	—	0	0.05	—	0.05			
—			0.05	—	0	0.05	—	0.05				
V _{in} = 0 or V _{DD}	V _{OH}	5.0 10 15	4.95	—	4.95	5.0	—	4.95	—	Vdc		
			9.95	—	9.95	10	—	9.95	—			
			14.95	—	14.95	15	—	14.95	—			
Input Voltage (V _O = 4.5 Vdc) (V _O = 9.0 Vdc) (V _O = 13.5 Vdc)	V _{IL}	5.0 10 15	—	1.0	—	2.25	1.0	—	1.0	Vdc		
			—	2.0	—	4.50	2.0	—	2.0			
—			2.5	—	6.75	2.5	—	2.5				
(V _O = 0.5 Vdc) (V _O = 1.0 Vdc) (V _O = 1.5 Vdc)	V _{IH}	5.0 10 15	4.0	—	4.0	2.75	—	4.0	—	Vdc		
			8.0	—	8.0	5.50	—	8.0	—			
			12.5	—	12.5	8.25	—	12.5	—			
Output Drive Current (V _{OH} = 2.5 Vdc) (V _{OH} = 4.6 Vdc) (V _{OH} = 9.5 Vdc) (V _{OH} = 13.5 Vdc) (V _{OL} = 0.4 Vdc) (V _{OL} = 0.5 Vdc) (V _{OL} = 1.5 Vdc)	Source	I _{OH}	5.0	-3.0	—	-2.4	-5.0	—	-1.7	—	mAdc	
			5.0	-0.64	—	-0.51	-1.0	—	-0.36	—		
			10	-1.6	—	-1.3	-2.5	—	-0.9	—		
	15		-4.2	—	-3.4	-10	—	-2.4	—			
	Sink		I _{OL}	5.0	0.64	—	0.51	1.0	—	0.36		—
				10	1.6	—	1.3	2.5	—	0.9		—
15		4.2		—	3.4	10	—	2.4	—			
Input Current	I _{in}	15		—	±0.1	—	±0.00001	±0.1	—	±1.0	μAdc	
Input Capacitance (V _{in} = 0)	C _{in}	—		—	—	—	5.0	7.5	—	—	pF	
Quiescent Current (Per Package)	I _{DD}	5.0		—	0.25	—	0.0005	0.25	—	7.5	μAdc	
		10	—	0.5	—	0.0010	0.5	—	15			
		15	—	1.0	—	0.0015	1.0	—	30			
Total Supply Current**† (Dynamic plus Quiescent, Per Gate) (C _L = 50 pF)	I _T	5.0	I _T = (0.7 μA/kHz) f + I _{DD} /6							μAdc		
		10	I _T = (1.4 μA/kHz) f + I _{DD} /6									
		15	I _T = (2.2 μA/kHz) f + I _{DD} /6									

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) Vfk$$

where: I_T is in μA (per package), C_L in pF, V = (V_{DD} - V_{SS}) in volts, f in kHz is input frequency, and k = 0.003.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range V_{SS} ≤ (V_{in} or V_{out}) ≤ V_{DD}. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

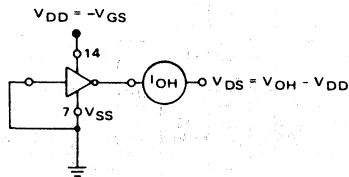
MC14007UB

SWITCHING CHARACTERISTICS* ($C_L = 50 \text{ pF}$, $T_A = 25^\circ\text{C}$)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ #	Max	Unit
Output Rise Time $t_{TLH} = (1.2 \text{ ns/pF}) C_L + 30 \text{ ns}$ $t_{TLH} = (0.5 \text{ ns/pF}) C_L + 20 \text{ ns}$ $t_{TLH} = (0.4 \text{ ns/pF}) C_L + 15 \text{ ns}$	t_{TLH}	5.0 10 15	— — —	90 45 35	180 90 70	ns
Output Fall Time $t_{THL} = (1.2 \text{ ns/pF}) C_L + 15 \text{ ns}$ $t_{THL} = (0.5 \text{ ns/pF}) C_L + 15 \text{ ns}$ $t_{THL} = (0.4 \text{ ns/pF}) C_L + 10 \text{ ns}$	t_{THL}	5.0 10 15	— — —	75 40 30	150 80 60	ns
Turn-Off Delay Time $t_{PLH} = (1.5 \text{ ns/pF}) C_L + 35 \text{ ns}$ $t_{PLH} = (0.2 \text{ ns/pF}) C_L + 20 \text{ ns}$ $t_{PLH} = (0.15 \text{ ns/pF}) C_L + 17.5 \text{ ns}$	t_{PLH}	5.0 10 15	— — —	60 30 25	125 75 55	ns
Turn-On Delay Time $t_{PHL} = (1.0 \text{ ns/pF}) C_L + 10 \text{ ns}$ $t_{PHL} = (0.3 \text{ ns/pF}) C_L + 15 \text{ ns}$ $t_{PHL} = (0.2 \text{ ns/pF}) C_L + 15 \text{ ns}$	t_{PHL}	5.0 10 15	— — —	60 30 25	125 75 55	ns

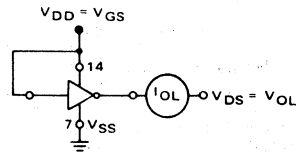
* The formulas given are for the typical characteristics only.
 Switching specifications are for device connected as an inverter.
 #Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

FIGURE 2 – TYPICAL OUTPUT SOURCE CHARACTERISTICS

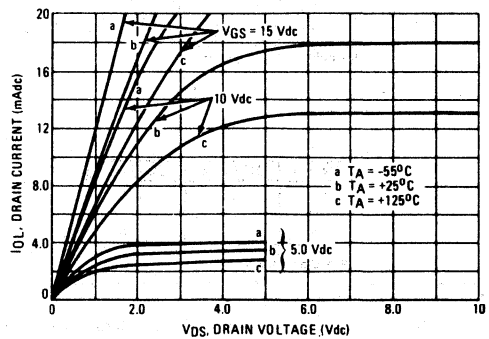
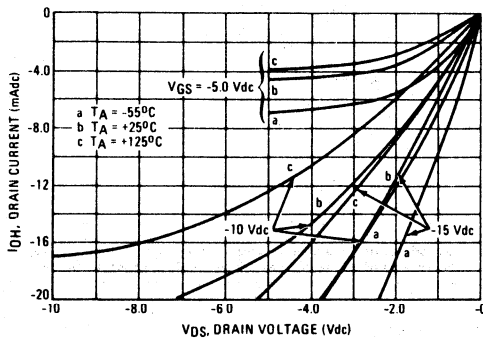


All unused inputs connected to ground.

FIGURE 3 – TYPICAL OUTPUT SINK CHARACTERISTICS



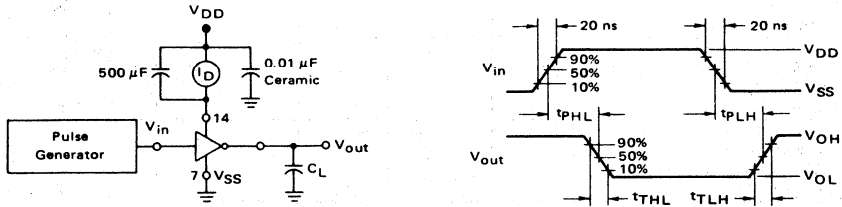
All unused inputs connected to ground.



These typical curves are not guarantees, but are design aids.
 Caution: The maximum current rating is 10 mA per pin.

MC14007UB

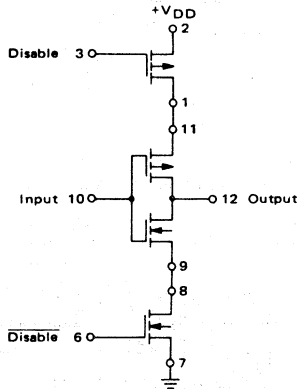
FIGURE 4 - SWITCHING TIME AND POWER DISSIPATION TEST CIRCUIT AND WAVEFORMS



APPLICATIONS

The MC14007UB dual pair plus inverter, which has access to all its elements offers a number of unique circuit applications. Figures 1, 5, and 6 are a few examples of the device flexibility.

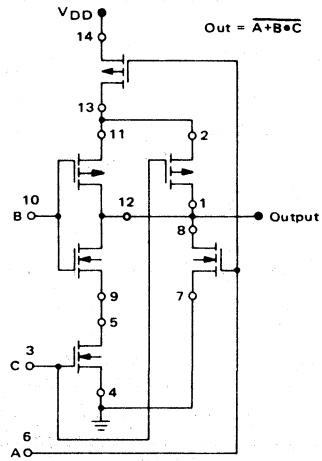
FIGURE 5 - 3-STATE BUFFER



INPUT	DISABLE	OUTPUT
1	0	0
0	0	1
X	1	Open

X = Don't Care

FIGURE 6 - AOI FUNCTIONS USING TREE LOGIC



Substrates of P-channel devices internally connected to VDD;
Substrates of N-channel devices internally connected to VSS.



MOTOROLA

MC14008B

4-BIT FULL ADDER

The MC14008B 4-bit full adder is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. This device consists of four full adders with fast internal look-ahead carry output. It is useful in binary addition and other arithmetic applications. The fast parallel carry output bit allows high-speed operation when used with other adders in a system.

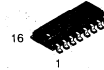
- Look-Ahead Carry Output
- Diode Protection on All Inputs
- All Outputs Buffered
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range
- Pin-for-Pin Replacement for CD4008B



**L SUFFIX
CERAMIC
CASE 620**



**P SUFFIX
PLASTIC
CASE 648**



**D SUFFIX
SOIC
CASE 751B**

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V _{DD}	DC Supply Voltage	-0.5 to +18.0	V
V _{in} , V _{out}	Input or Output Voltage (DC or Transient)	-0.5 to V _{DD} + 0.5	V
I _{in} , I _{out}	Input or Output Current (DC or Transient), per Pin	± 10	mA
P _D	Power Dissipation, per Package†	500	mW
T _{stg}	Storage Temperature	-65 to +150	°C
T _L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P and D/DW" Packages: -7.0 mW/°C From 65°C To 125°C
Ceramic "L" Packages: -12 mW/°C From 100°C To 125°C

ORDERING INFORMATION

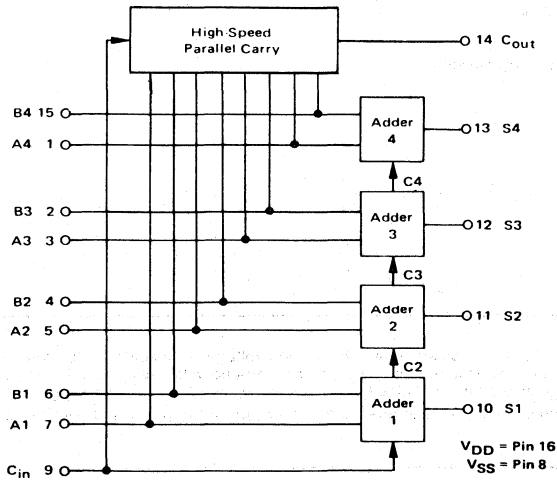
MC14XXXBCP Plastic
MC14XXXBCL Ceramic
MC14XXXBD SOIC

T_A = -55° to 125°C for all packages.

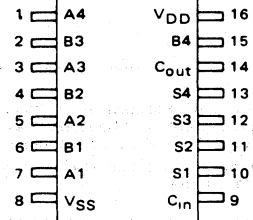
**TRUTH TABLE
(One Stage)**

C _{in}	B	A	C _{out}	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

BLOCK DIAGRAM



PIN ASSIGNMENT



6

MC14008B

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V _{DD} Vdc	-55°C		25°C			125°C		Unit	
			Min	Max	Min	Typ #	Max	Min	Max		
Output Voltage V _{in} = V _{DD} or 0 V _{in} = 0 or V _{DD}	V _{OL}	5.0	—	0.05	—	0	0.05	—	0.05	Vdc	
		10	—	0.05	—	0	0.05	—	0.05		
		15	—	0.05	—	0	0.05	—	0.05		
"1" Level	V _{OH}	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc	
		10	9.95	—	9.95	10	—	9.95	—		
		15	14.95	—	14.95	15	—	14.95	—		
Input Voltage (V _O = 4.5 or 0.5 Vdc) (V _O = 9.0 or 1.0 Vdc) (V _O = 13.5 or 1.5 Vdc) (V _O = 0.5 or 4.5 Vdc) (V _O = 1.0 or 9.0 Vdc) (V _O = 1.5 or 13.5 Vdc)	"0" Level	V _{IL}	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc
			10	—	3.0	—	4.50	3.0	—	3.0	
			15	—	4.0	—	6.75	4.0	—	4.0	
	"1" Level	V _{IH}	5.0	3.5	—	3.5	2.75	—	3.5	—	Vdc
			10	7.0	—	7.0	5.50	—	7.0	—	
			15	11	—	11	8.25	—	11	—	
Output Drive Current (V _{OH} = 2.5 Vdc) (V _{OH} = 4.6 Vdc) (V _{OH} = 9.5 Vdc) (V _{OH} = 13.5 Vdc) (V _{OL} = 0.4 Vdc) (V _{OL} = 0.5 Vdc) (V _{OL} = 1.5 Vdc)	Source	I _{OH}	5.0	-3.0	—	-2.4	-4.2	—	-1.7	—	mA _{dc}
			10	-0.64	—	-0.51	-0.88	—	-0.36	—	
			15	-1.6	—	-1.3	-2.25	—	-0.9	—	
	Sink	I _{OL}	5.0	0.64	—	0.51	0.88	—	0.36	—	mA _{dc}
			10	1.6	—	1.3	2.25	—	0.9	—	
			15	4.2	—	3.4	8.8	—	2.4	—	
Input Current	I _{in}	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	μA _{dc}	
Input Capacitance (V _{in} = 0)	C _{in}	—	—	—	—	5.0	7.5	—	—	pF	
Quiescent Current (Per Package)	I _{DD}	5.0	—	5.0	—	0.005	5.0	—	150	μA _{dc}	
		10	—	10	—	0.010	10	—	300		
		15	—	20	—	0.015	20	—	600		
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C _L = 50 pF on all outputs, all buffers switching)	I _T	5.0	I _T = (1.7 μA/kHz) f + I _{DD}							μA _{dc}	
10	I _T = (3.4 μA/kHz) f + I _{DD}										
15	I _T = (5.0 μA/kHz) f + I _{DD}										

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) V/fk$$

where: I_T is in μA (per package), C_L in pF, V = (V_{DD} - V_{SS}) in volts, f in kHz is input frequency, and k = 0.005.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range V_{SS} ≤ (V_{in} or V_{out}) ≤ V_{DD}. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

MC14008B

SWITCHING CHARACTERISTICS* ($C_L = 50 \text{ pF}$, $T_A = 25^\circ\text{C}$)

Characteristic	Symbol	VDD Vdc	Min	Typ #	Max	Unit
Output Rise and Fall Time	t_{TLH} , t_{THL}	5.0	—	100	200	ns
t_{TLH} , $t_{THL} = (1.5 \text{ ns/pF}) C_L + 25 \text{ ns}$		10	—	50	100	
t_{TLH} , $t_{THL} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$		15	—	40	80	
Propagation Delay Time	t_{PLH} , t_{PHL}					ns
Sum In to Sum Out						
t_{PLH} , $t_{PHL} = (1.7 \text{ ns/pF}) C_L + 315 \text{ ns}$		5.0	—	400	800	
t_{PLH} , $t_{PHL} = (0.66 \text{ ns/pF}) C_L + 127 \text{ ns}$		10	—	160	320	
t_{PLH} , $t_{PHL} = (0.5 \text{ ns/pF}) C_L + 90 \text{ ns}$		15	—	115	230	
Sum In to Carry Out						
t_{PLH} , $t_{PHL} = (1.7 \text{ ns/pF}) C_L + 220 \text{ ns}$		5.0	—	305	610	
t_{PLH} , $t_{PHL} = (0.66 \text{ ns/pF}) C_L + 112 \text{ ns}$		10	—	145	290	
t_{PLH} , $t_{PHL} = (0.5 \text{ ns/pF}) C_L + 85 \text{ ns}$		15	—	110	220	
Carry In to Sum Out						
t_{PLH} , $t_{PHL} = (1.7 \text{ ns/pF}) C_L + 290 \text{ ns}$		5.0	—	375	750	
t_{PLH} , $t_{PHL} = (0.66 \text{ ns/pF}) C_L + 122 \text{ ns}$		10	—	155	310	
t_{PLH} , $t_{PHL} = (0.5 \text{ ns/pF}) C_L + 90 \text{ ns}$		15	—	115	230	
Carry In to Carry Out						
t_{PLH} , $t_{PHL} = (1.7 \text{ ns/pF}) C_L + 85 \text{ ns}$		5.0	—	170	340	
t_{PLH} , $t_{PHL} = (0.66 \text{ ns/pF}) C_L + 42 \text{ ns}$		10	—	75	150	
t_{PLH} , $t_{PHL} = (0.5 \text{ ns/pF}) C_L + 30 \text{ ns}$		15	—	55	110	

*The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

FIGURE 1 – TYPICAL SOURCE CURRENT CHARACTERISTICS TEST CIRCUIT

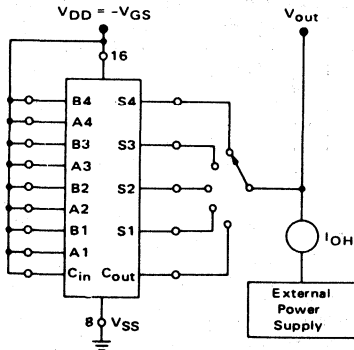
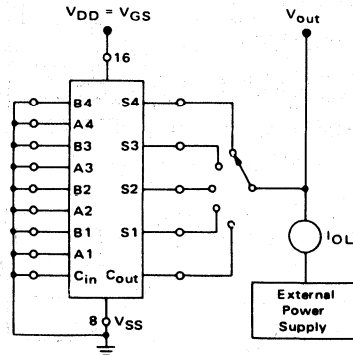


FIGURE 2 – TYPICAL SINK CURRENT CHARACTERISTICS TEST CIRCUIT



MC14008B

FIGURE 3 – DYNAMIC POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

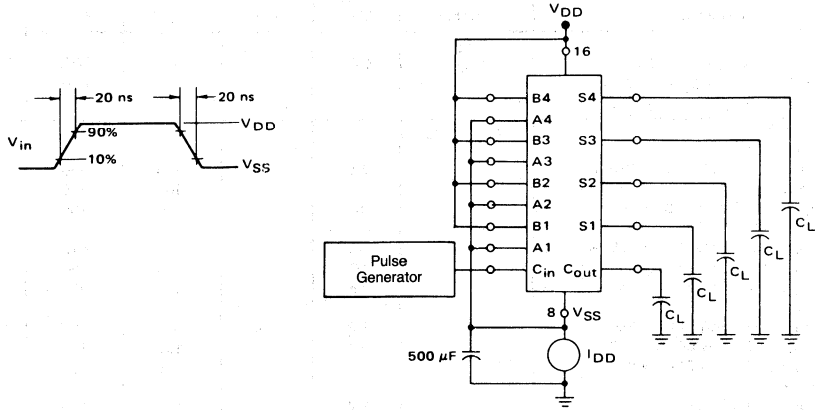
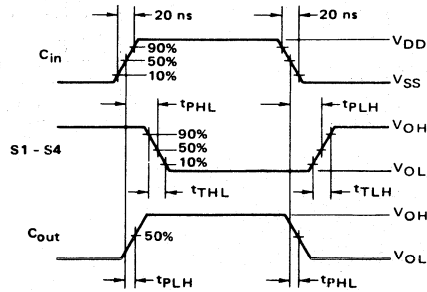
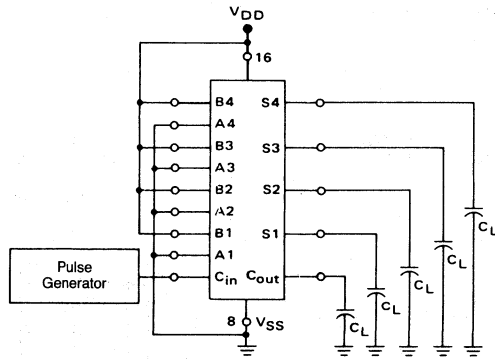


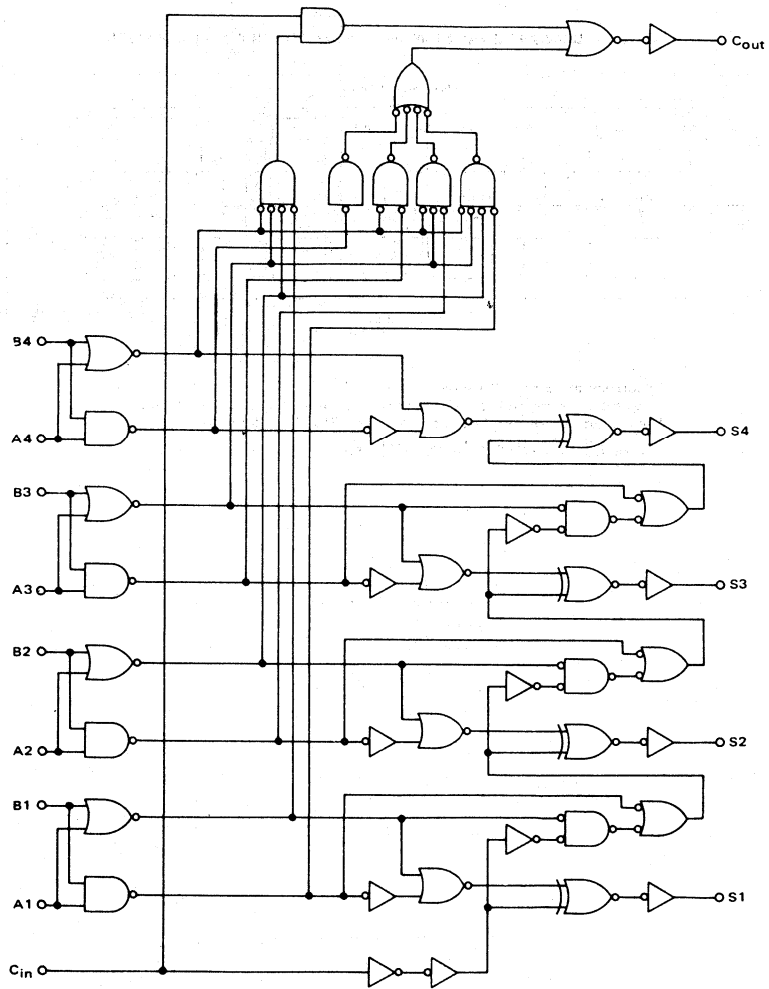
FIGURE 4 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



6

MC14008B

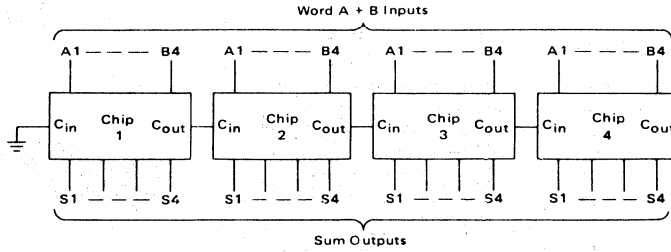
FIGURE 5 - LOGIC DIAGRAM



MC14008B

TYPICAL APPLICATION

FIGURE 6 – USING THE MC14008B IN A 16-BIT ADDER CONFIGURATION



Calculation of 16-bit adder speed:

$$t_p \text{ total} = t_p (\text{Sum to Carry}) + t_p (\text{Carry to Sum}) + 2 t_p (\text{Carry to Carry})$$

The guaranteed 16-bit adder speed at 10 V, 25°C, C_L = 50 pF is:

$$t_p \text{ total} = 290 + 310 + 300 = 900 \text{ ns}$$



MOTOROLA

MC14011B, MC14012B

See Page 6-5

MC14011UB, MC14012UB

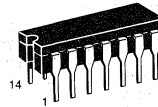
See Page 6-14

MC14013B

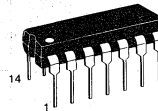
DUAL TYPE D FLIP-FLOP

The MC14013B dual type D flip-flop is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. Each flip-flop has independent Data, (D), Direct Set, (S), Direct Reset, (R), and Clock (C) inputs and complementary outputs (Q and \bar{Q}). These devices may be used as shift register elements or as type T flip-flops for counter and toggle applications.

- Static Operation
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Logic Edge-Clocked Flip-Flop Design
Logic state is retained indefinitely with clock level either high or low; information is transferred to the output only on the positive-going edge of the clock pulse
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range
- Pin-for-Pin Replacement for CD4013B



**L SUFFIX
CERAMIC
CASE 632**



**P SUFFIX
PLASTIC
CASE 646**



**D SUFFIX
SOIC
CASE 751A**

ORDERING INFORMATION

- MC14XXXBCP Plastic
- MC14XXXBCL Ceramic
- MC14XXXBD SOIC

T_A = -55° to 125°C for all packages.

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V _{DD}	DC Supply Voltage	-0.5 to +18.0	V
V _{in} , V _{out}	Input or Output Voltage (DC or Transient)	-0.5 to V _{DD} + 0.5	V
I _{in} , I _{out}	Input or Output Current (DC or Transient), per Pin	± 10	mA
P _D	Power Dissipation, per Package†	500	mW
T _{stg}	Storage Temperature	-65 to +150	°C
T _L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.

†Temperature Derating: Plastic "P and D/DW" Packages: -7.0 mW/°C From 65°C To 125°C
Ceramic "L" Packages: -12 mW/°C From 100°C To 125°C

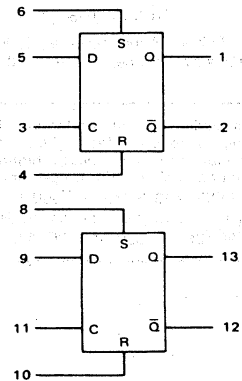
TRUTH TABLE

CLOCK†	INPUTS			OUTPUTS	
	DATA	RESET	SET	Q	\bar{Q}
	0	0	0	0	1
	1	0	0	1	0
	x	0	0	Q	\bar{Q}
x	x	1	0	0	1
x	x	0	1	1	0
x	x	1	1	1	1

No Change

X = Don't Care
† = Level Change

BLOCK DIAGRAM



V_{DD} = Pin 14
V_{SS} = Pin 7

6

MC14013B

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	-55°C		25°C			125°C		Unit
			Min	Max	Min	Typ #	Max	Min	Max	
Output Voltage $V_{in} = V_{DD}$ or 0	"0" Level V_{OL}	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
		10	—	0.05	—	0	0.05	—	0.05	
		15	—	0.05	—	0	0.05	—	0.05	
	"1" Level V_{OH}	5.0	4.95	—	4.95	5.0	—	4.95	—	
		10	9.95	—	9.95	10	—	9.95	—	
		15	14.95	—	14.95	15	—	14.95	—	
Input Voltage ($V_O = 4.5$ or 0.5 Vdc) ($V_O = 9.0$ or 1.0 Vdc) ($V_O = 13.5$ or 1.5 Vdc)	"0" Level V_{IL}	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc
		10	—	3.0	—	4.50	3.0	—	3.0	
		15	—	4.0	—	6.75	4.0	—	4.0	
	"1" Level V_{IH}	5.0	3.5	—	3.5	2.75	—	3.5	—	
		10	7.0	—	7.0	5.50	—	7.0	—	
		15	11	—	11	8.25	—	11	—	
Output Drive Current ($V_{OH} = 2.5$ Vdc) ($V_{OH} = 4.6$ Vdc) ($V_{OH} = 9.5$ Vdc) ($V_{OH} = 13.5$ Vdc)	Source I_{OH}	5.0	-3.0	—	-2.4	-4.2	—	-1.7	—	mAdc
		10	-0.64	—	-0.51	-0.88	—	-0.36	—	
		15	-1.6	—	-1.3	-2.25	—	-0.9	—	
	Sink I_{OL}	5.0	0.64	—	0.51	0.88	—	0.36	—	
		10	1.6	—	1.3	2.25	—	0.9	—	
		15	4.2	—	3.4	8.8	—	2.4	—	
Input Current	I_{in}	15	—	± 0.1	—	± 0.00001	± 0.1	—	± 1.0	μ Adc
Input Capacitance ($V_{in} = 0$)	C_{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)	I_{DD}	5.0	—	1.0	—	0.002	1.0	—	30	μ Adc
		10	—	2.0	—	0.004	2.0	—	60	
		15	—	4.0	—	0.006	4.0	—	120	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) ($C_L = 50$ pF on all outputs, all buffers switching)	I_T	5.0	$I_T = (0.75 \mu\text{A/kHz}) f + I_{DD}$							μ Adc
		10	$I_T = (1.5 \mu\text{A/kHz}) f + I_{DD}$							
		15	$I_T = (2.3 \mu\text{A/kHz}) f + I_{DD}$							

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C.

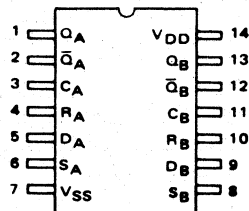
†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) \text{ Vfk}$$

where: I_T is in μA (per package), C_L in pF, $V = (V_{DD} - V_{SS})$ in volts, f in kHz is input frequency, and $k = 0.002$.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

PIN ASSIGNMENT



MC14013B

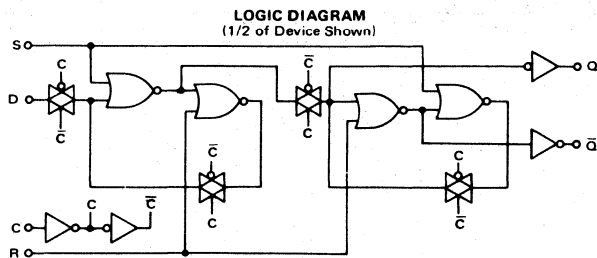
SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V _{DD}	Min	Typ #	Max	Unit
Output Rise and Fall Time t _{TLH} , t _{THL} = (1.5 ns/pF) C _L + 25 ns t _{TLH} , t _{THL} = (0.75 ns/pF) C _L + 12.5 ns t _{TLH} , t _{THL} = (0.55 ns/pF) C _L + 9.5 ns	t _{TLH} , t _{THL}	5.0 10 15	— — —	100 50 40	200 100 80	ns
Propagation Delay Time Clock to Q, \bar{Q} t _{PLH} , t _{PHL} = (1.7 ns/pF) C _L + 90 ns t _{PLH} , t _{PHL} = (0.66 ns/pF) C _L + 42 ns t _{PLH} , t _{PHL} = (0.5 ns/pF) C _L + 25 ns Set to Q, \bar{Q} t _{PLH} , t _{PHL} = (1.7 ns/pF) C _L + 90 ns t _{PLH} , t _{PHL} = (0.66 ns/pF) C _L + 42 ns t _{PLH} , t _{PHL} = (0.5 ns/pF) C _L + 25 ns Reset to Q, \bar{Q} t _{PLH} , t _{PHL} = (1.7 ns/pF) C _L + 265 ns t _{PLH} , t _{PHL} = (0.66 ns/pF) C _L + 67 ns t _{PLH} , t _{PHL} = (0.5 ns/pF) C _L + 50 ns	t _{PLH} , t _{PHL}	5.0 10 15 5.0 10 15 5.0 10 15	— — — — — — — — —	175 75 50 175 75 50 225 100 75	350 150 100 350 150 100 450 200 150	ns
Setup Times**	t _{su}	5.0 10 15	40 20 15	20 10 7.5	— — —	ns
Hold Times**	t _h	5.0 10 15	40 20 15	20 10 7.5	— — —	ns
Clock Pulse Width	t _{WL} , t _{WH}	5.0 10 15	250 100 70	125 50 35	— — —	ns
Clock Pulse Frequency	f _{cl}	5.0 10 15	— — —	4.0 10 14	2.0 5.0 7.0	MHz
Clock Pulse Rise and Fall Time	t _{TLH} , t _{THL}	5.0 10 15	— — —	— — —	15 5.0 4.0	μs
Set and Reset Pulse Width	t _{WL} , t _{WH}	5.0 10 15	250 100 70	125 50 35	— — —	ns
Removal Times	t _{rem}					ns
Set		5 10 15	80 45 35	0 5 5	— — —	
Reset		5 10 15	50 30 25	-35 -10 -5	— — —	

*The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**Data must be valid for 250 ns with a 5 V supply, 100 ns with 10 V, and 70 ns with 15 V.



MC14013B

FIGURE 1 — DYNAMIC SIGNAL WAVEFORMS
(Data, Clock, and Output)

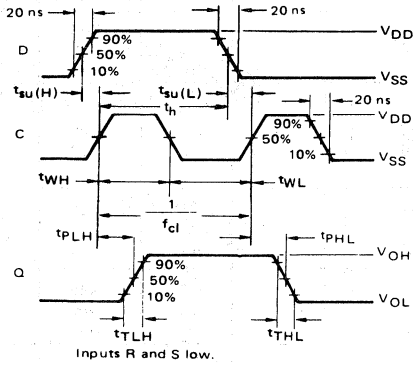
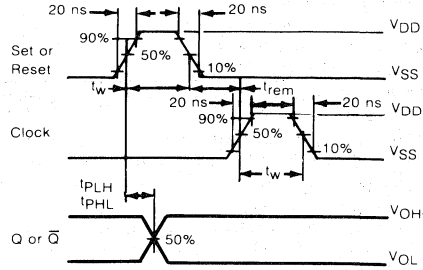
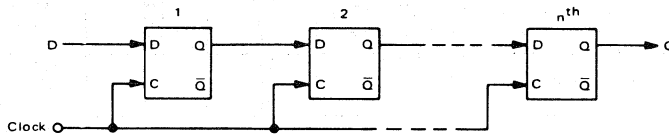


FIGURE 2 — DYNAMIC SIGNAL WAVEFORMS
(Set, Reset, Clock, and Output)

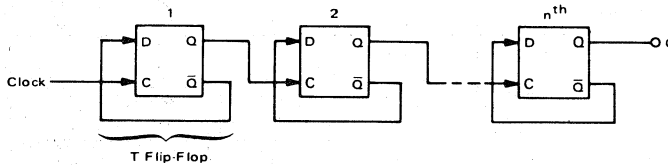


TYPICAL APPLICATIONS

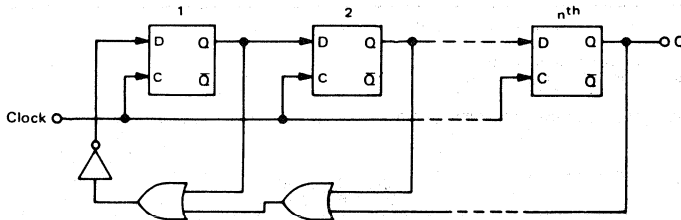
n-STAGE SHIFT REGISTER



BINARY RIPPLE UP-COUNTER (Divide-by- 2^n)



MODIFIED RING COUNTER (Divide-by-(n + 1))





MC14014B MC14021B

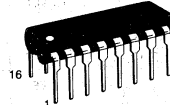
8-BIT STATIC SHIFT REGISTER

The MC14014B and MC14021B 8-bit static shift registers are constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These shift registers find primary use in parallel-to-serial data conversion, synchronous and asynchronous parallel input, serial output data queueing; and other general purpose register applications requiring low power and/or high noise immunity.

- Synchronous Parallel Input/Serial Output (MC14014B)
- Asynchronous Parallel Input/Serial Output (MC14021B)
- Synchronous Serial Input/Serial Output
- Full Static Operation
- "Q" Outputs from Sixth, Seventh, and Eighth Stages
- Double Diode Input Protection
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range
- MC14014B Pin-for-Pin Replacement for CD4014B
- MC14021B Pin-for-Pin Replacement for CD4021B



L SUFFIX
CERAMIC
CASE 620



P SUFFIX
PLASTIC
CASE 648



D SUFFIX
SOIC
CASE 751B

ORDERING INFORMATION

MC14XXXBCP Plastic
MC14XXXBCL Ceramic
MC14XXXBD SOIC

T_A = -55° to 125°C for all packages.

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V _{DD}	DC Supply Voltage	-0.5 to +18.0	V
V _{in} , V _{out}	Input or Output Voltage (DC or Transient)	-0.5 to V _{DD} + 0.5	V
I _{in} , I _{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
P _D	Power Dissipation, per Package†	500	mW
T _{stg}	Storage Temperature	-65 to +150	°C
T _L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.

†Temperature Derating: Plastic "P and D/DW" Packages: -7.0 mW/°C From 65°C To 125°C
Ceramic "L" Packages: -12 mW/°C From 100°C To 125°C

TRUTH TABLE SERIAL OPERATION:

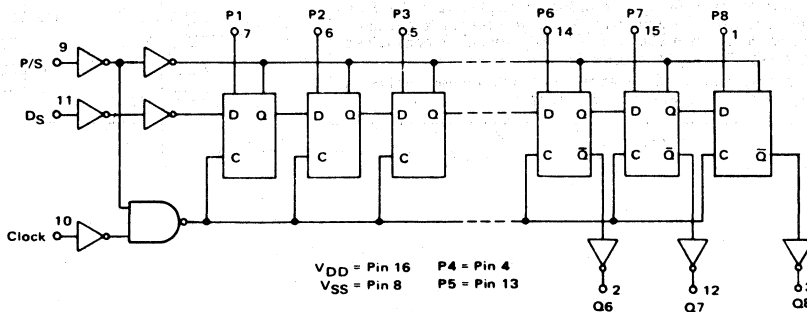
t	CLOCK	D _S	P/S	Q ₆ t = n+6	Q ₇ t = n+7	Q ₈ t = n+8
n		0	0	0	?	?
n+1		1	0	1	0	?
n+2		0	0	0	1	0
n+3		1	0	1	0	1
		X	0	Q ₆	Q ₇	Q ₈

PARALLEL OPERATION:

CLOCK		D _S	P/S	P _n	*Q _n
MC14014B	MC14021B				
		X	X	1	0
		X	X	1	1

*Q₆, Q₇, & Q₈ are available externally
X = Don't Care

LOGIC DIAGRAM



MC14014B•MC14021B

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V _{DD} Vdc	-55°C		25°C			125°C		Unit
			Min	Max	Min	Typ #	Max	Min	Max	
Output Voltage V _{in} = V _{DD} or 0	V _{OL}	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
		10	—	0.05	—	0	0.05	—	0.05	
V _{in} = 0 or V _{DD}	V _{OH}	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc
		10	9.95	—	9.95	10	—	9.95	—	
Input Voltage (V _O = 4.5 or 0.5 Vdc) (V _O = 9.0 or 1.0 Vdc) (V _O = 13.5 or 1.5 Vdc)	V _{IL}	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc
		10	—	3.0	—	4.50	3.0	—	3.0	
(V _O = 0.5 or 4.5 Vdc) (V _O = 1.0 or 9.0 Vdc) (V _O = 1.5 or 13.5 Vdc)	V _{IH}	5.0	3.5	—	3.5	2.75	—	3.5	—	Vdc
		10	7.0	—	7.0	5.50	—	7.0	—	
Output Drive Current (V _{OH} = 2.5 Vdc) (V _{OH} = 4.6 Vdc) (V _{OH} = 9.5 Vdc) (V _{OH} = 13.5 Vdc)	I _{OH}	5.0	-3.0	—	-2.4	-4.2	—	-1.7	—	mAdc
		5.0	-0.64	—	-0.51	-0.88	—	-0.36	—	
(V _{OL} = 0.4 Vdc) (V _{OL} = 0.5 Vdc) (V _{OL} = 1.5 Vdc)	I _{OL}	5.0	0.64	—	0.51	0.88	—	0.36	—	mAdc
		10	1.6	—	1.3	2.25	—	0.9	—	
		15	4.2	—	3.4	8.8	—	2.4	—	
Input Current	I _{in}	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	μAdc
Input Capacitance (V _{in} = 0)	C _{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)	I _{DD}	5.0	—	5.0	—	0.005	5.0	—	150	μAdc
		10	—	10	—	0.010	10	—	300	
		15	—	20	—	0.015	20	—	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C _L = 50 pF on all outputs, all buffers switching)	I _T	5.0	I _T = (0.75 μA/kHz) f + I _{DD}							μAdc
10	I _T = (1.50 μA/kHz) f + I _{DD}									
15	I _T = (2.25 μA/kHz) f + I _{DD}									

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

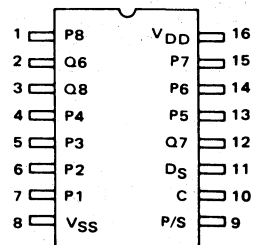
$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) V/k$$

where: I_T is in μA (per package), C_L in pF, V = (V_{DD} - V_{SS}) in volts, f in kHz is input frequency, and k = 0.0015.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range V_{SS} ≤ (V_{in} or V_{out}) ≤ V_{DD}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

PIN ASSIGNMENT



MC14014B•MC14021B

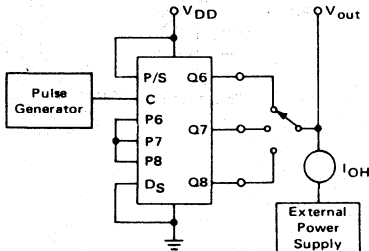
SWITCHING CHARACTERISTICS (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V _{DD} V _{dC}	Min	Typ #	Max	Unit
Output Rise and Fall Time t _{TLH} , t _{THL} = (1.5 ns/pF) C _L + 25 ns t _{TLH} , t _{THL} = (0.75 ns/pF) C _L + 12.5 ns t _{TLH} , t _{THL} = (0.55 ns/pF) C _L + 9.5 ns	t _{TLH} , t _{THL}	5.0 10 15	— — —	100 50 40	200 100 80	ns
Propagation Delay Time (Clock to Q, P/S to Q) t _{PHL} , t _{PLH} = (1.7 ns/pF) C _L + 315 ns t _{PHL} , t _{PLH} = (0.66 ns/pF) C _L + 137 ns t _{PHL} , t _{PLH} = (0.5 ns/pF) C _L + 90 ns	t _{PLH} , t _{PHL}	5.0 10 15	— — —	400 170 115	800 340 230	ns
Clock Pulse Width	t _{WH}	5.0 10 15	400 175 135	150 75 40	— — —	ns
Clock Frequency	f _{cl}	5.0 10 15	— — —	3.0 6.0 8.0	1.5 3.0 4.0	MHz
Parallel/Serial Control Pulse Width	t _{WH}	5.0 10 15	400 175 135	150 75 40	— — —	ns
Setup Time P/S to Clock	t _{su}	5.0 10 15	200 100 80	100 50 40	— — —	ns
Hold Time Clock to P/S	t _h	5.0 10 15	20 20 25	-2.5 -10 0	— — —	ns
Setup Time Data (Parallel or Serial) to Clock or P/S	t _{su}	5.0 10 15	350 80 60	150 50 30	— — —	ns
Hold Time Clock to D _S	t _h	5.0 10 15	45 35 35	0 0 5	— — —	ns
Hold Time Clock to P _n	t _h	5.0 10 15	50 45 45	25 20 20	— — —	ns
Input Clock Rise Time	t _{r(cl)}	5.0 10 15	— — —	— — —	15 5 4	μs

*The formulas given are for the typical characteristics only at 25°C.

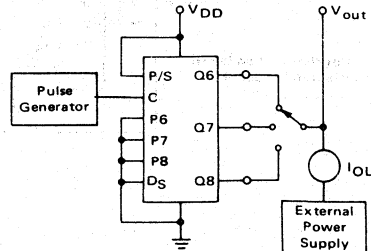
#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

FIGURE 1 – OUTPUT SOURCE CURRENT TEST CIRCUIT



Preset output under test to a logic "1" level.

FIGURE 2 – OUTPUT SINK CURRENT TEST CIRCUIT



MC14014B•MC14021B

FIGURE 3 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

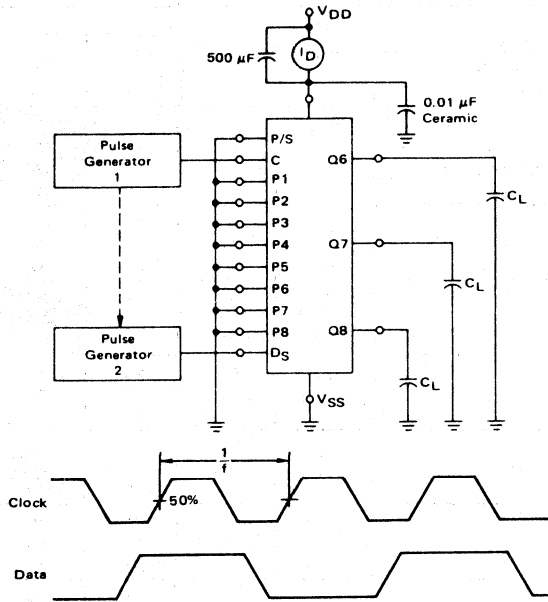
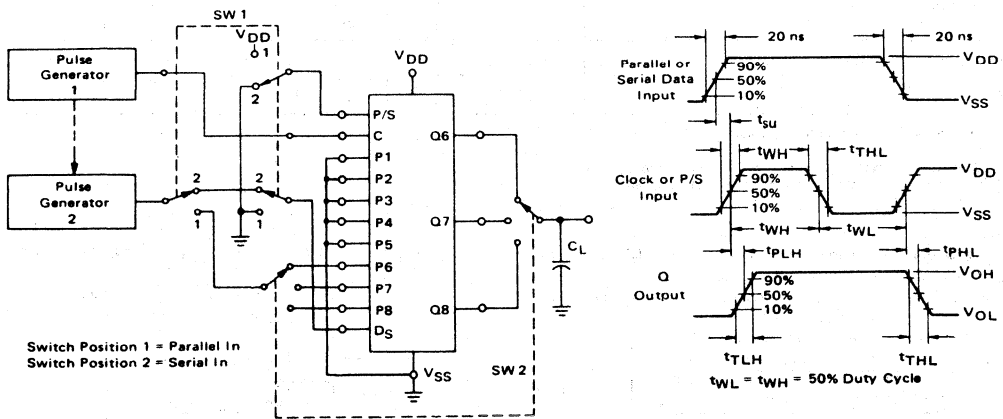


FIGURE 4 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



6



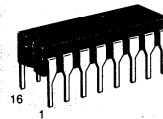
MOTOROLA

MC14015B

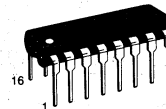
DUAL 4-BIT STATIC SHIFT REGISTER

The MC14015B dual 4-bit static shift register is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. It consists of two identical, independent 4-state serial-input/parallel-output registers. Each register has independent Clock and Reset inputs with a single serial Data input. The register states are type D master-slave flip-flops. Data is shifted from one stage to the next during the positive-going clock transition. Each register can be cleared when a high level is applied on the Reset line. These complementary MOS shift registers find primary use in buffer storage and serial-to-parallel conversion where low power dissipation and/or noise immunity is desired.

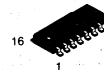
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Logic Edge-Clocked Flip-Flop Design – Logic state is retained indefinitely with clock level either high or low; information is transferred to the output only on the positive going edge of the clock pulse.
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range.



**L SUFFIX
CERAMIC
CASE 620**



**P SUFFIX
PLASTIC
CASE 648**



**D SUFFIX
SOIC
CASE 751B**

ORDERING INFORMATION

- MC14XXXBCP Plastic
- MC14XXXBCL Ceramic
- MC14XXXBD SOIC

T_A = -55° to 125°C for all packages.

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V _{DD}	DC Supply Voltage	-0.5 to +18.0	V
V _{in} , V _{out}	Input or Output Voltage (DC or Transient)	-0.5 to V _{DD} + 0.5	V
I _{in} , I _{out}	Input or Output Current (DC or Transient), per Pin	± 10	mA
P _D	Power Dissipation, per Package†	500	mW
T _{stg}	Storage Temperature	-65 to +150	°C
T _L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.

†Temperature Derating: Plastic "P and D/DW" Packages: -7.0 mW/°C From 65°C To 125°C
Ceramic "L" Packages: -12 mW/°C From 100°C To 125°C

TRUTH TABLE

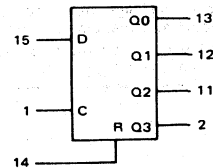
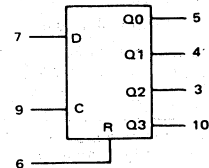
C	D	R	Q ₀	Q _n
	0	0	0	Q _{n-1}
	1	0	1	Q _{n-1}
	X	0	No Change	No Change
X	X	1	0	0

X = Don't Care

Q_n = Q₀, Q₁, Q₂, or Q₃, as applicable.

Q_{n-1} = Output of prior stage.

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

6

MC14015B

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V _{DD} Vdc	-55°C		25°C			125°C		Unit	
			Min	Max	Min	Typ #	Max	Min	Max		
Output Voltage V _{in} = V _{DD} or 0	V _{OL}	5.0	—	0.05	—	0	0.05	—	0.05	Vdc	
		10	—	0.05	—	0	0.05	—	0.05		
		15	—	0.05	—	0	0.05	—	0.05		
V _{in} = 0 or V _{DD}	V _{OH}	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc	
		10	9.95	—	9.95	10	—	9.95	—		
		15	14.95	—	14.95	15	—	14.95	—		
Input Voltage (V _O = 4.5 or 0.5 Vdc) (V _O = 9.0 or 1.0 Vdc) (V _O = 13.5 or 1.5 Vdc)	V _{IL}	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc	
		10	—	3.0	—	4.50	3.0	—	3.0		
		15	—	4.0	—	6.75	4.0	—	4.0		
	V _{OH}	5.0	3.5	—	3.5	2.75	—	3.5	—	Vdc	
		10	7.0	—	7.0	5.50	—	7.0	—		
		15	11	—	11	8.25	—	11	—		
Output Drive Current (V _{OH} = 2.5 Vdc) (V _{OH} = 4.6 Vdc) (V _{OH} = 9.5 Vdc) (V _{OH} = 13.5 Vdc)	Source	I _{OH}	5.0	-3.0	—	-2.4	-4.2	—	-1.7	—	mA _{dc}
			5.0	-0.64	—	-0.51	-0.88	—	-0.36	—	
			10	-1.6	—	-1.3	-2.25	—	-0.9	—	
	Sink	I _{OL}	5.0	0.64	—	0.51	0.88	—	0.36	—	mA _{dc}
			10	1.6	—	1.3	2.25	—	0.9	—	
			15	4.2	—	3.4	8.8	—	2.4	—	
Input Current	I _{in}	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	μA _{dc}	
Input Capacitance (V _{in} = 0)	C _{in}	—	—	—	—	5.0	7.5	—	—	pF	
Quiescent Current (Per Package)	I _{DD}	5.0	—	5.0	—	0.005	5.0	—	150	μA _{dc}	
		10	—	10	—	0.010	10	—	300		
		15	—	20	—	0.015	20	—	600		
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C _L = 50 pF on all outputs, all buffers switching)	I _T	5.0	I _T = (1.2 μA/kHz) f + I _{DD}							μA _{dc}	
		10	I _T = (2.4 μA/kHz) f + I _{DD}								
		15	I _T = (3.6 μA/kHz) f + I _{DD}								

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C.

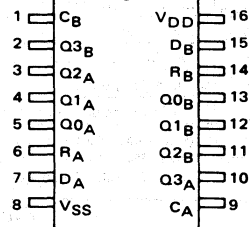
†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) V/k$$

where: I_T is in μA (per package), C_L in pF, V = (V_{DD} - V_{SS}) in volts, f in kHz is input frequency, and k = 0.002.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range V_{SS} ≤ (V_{in} or V_{out}) ≤ V_{DD}. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

PIN ASSIGNMENT



MC14015B

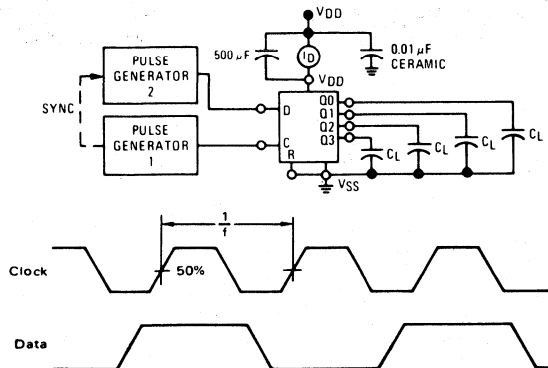
SWITCHING CHARACTERISTICS* ($C_L = 50$ pf, $T_A = 25^\circ\text{C}$)

Characteristic	Symbol	V _{DD}	Min	Typ #	Max	Unit
Output Rise and Fall Time $t_{TLH}, t_{THL} = (1.5 \text{ ns/pF}) C_L + 25 \text{ ns}$ $t_{TLH}, t_{THL} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$ $t_{TLH}, t_{THL} = (0.55 \text{ ns/pF}) C_L + 9.5 \text{ ns}$	t_{TLH}, t_{THL}	5.0 10 15	— — —	100 50 40	200 100 80	ns
Propagation Delay Time Clock, Data to Q $t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 225 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 92 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 65 \text{ ns}$ Reset to Q $t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 375 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 147 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 95 \text{ ns}$	t_{PLH}, t_{PHL}	5.0 10 15	— — —	310 125 90	750 250 170	ns
Clock Pulse Width	t_{WH}	5.0 10 15	400 175 135	185 85 55	— — —	ns
Clock Pulse Frequency	f_{cl}	5.0 10 15	— — —	2.0 6.0 7.5	1.5 3.0 3.75	MHz
Clock Pulse Rise and Fall Times	t_{TLH}, t_{THL}	5.0 10 15	— — —	— — —	15 5 4	μs
Reset Pulse Width	t_{WH}	5.0 10 15	400 160 120	200 80 60	— — —	ns
Setup Time	t_{su}	5.0 10 15	350 100 75	100 50 40	— — —	ns

*The formulas given are for typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

FIGURE 1 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM



MC14015B

FIGURE 2 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

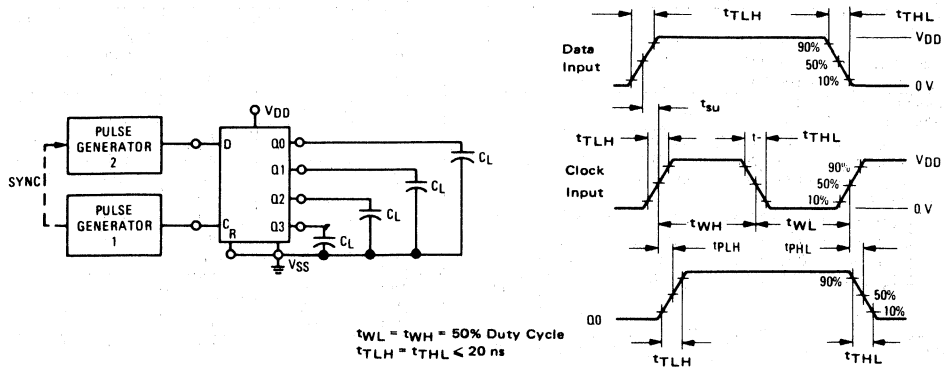
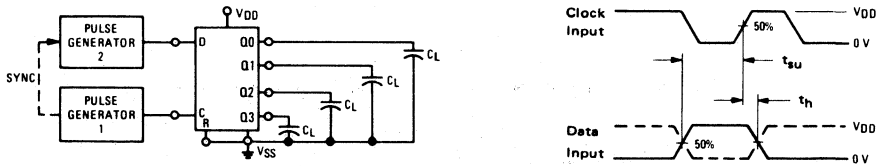
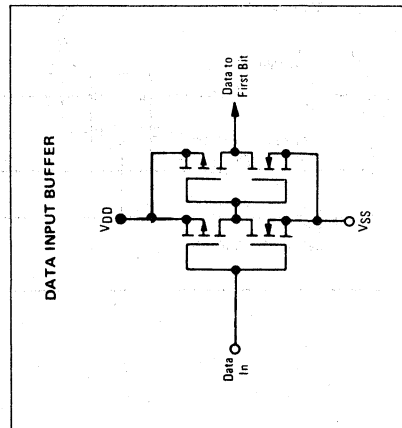
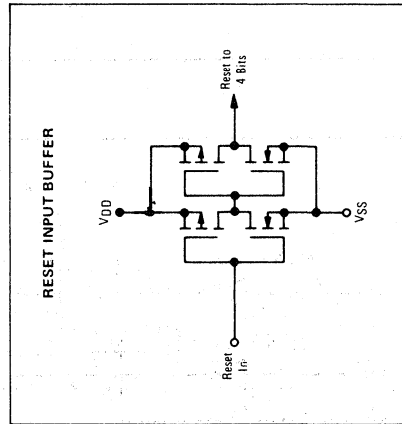
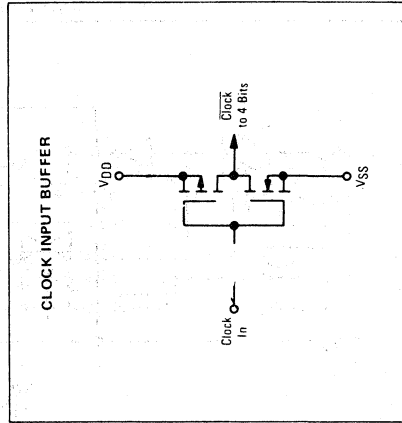
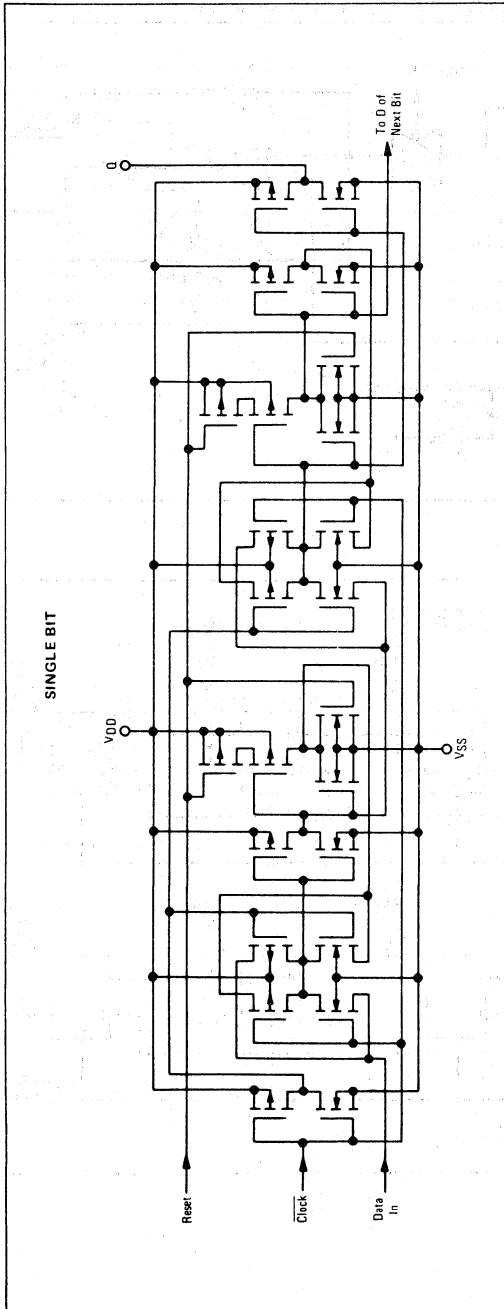


FIGURE 3 – SETUP AND HOLD TIME TEST CIRCUIT AND WAVEFORMS



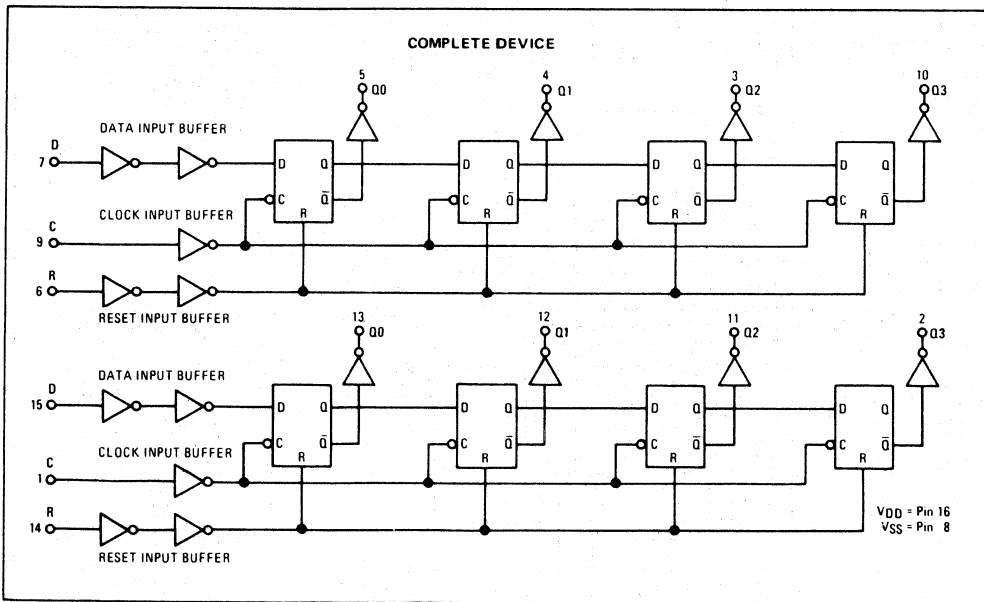
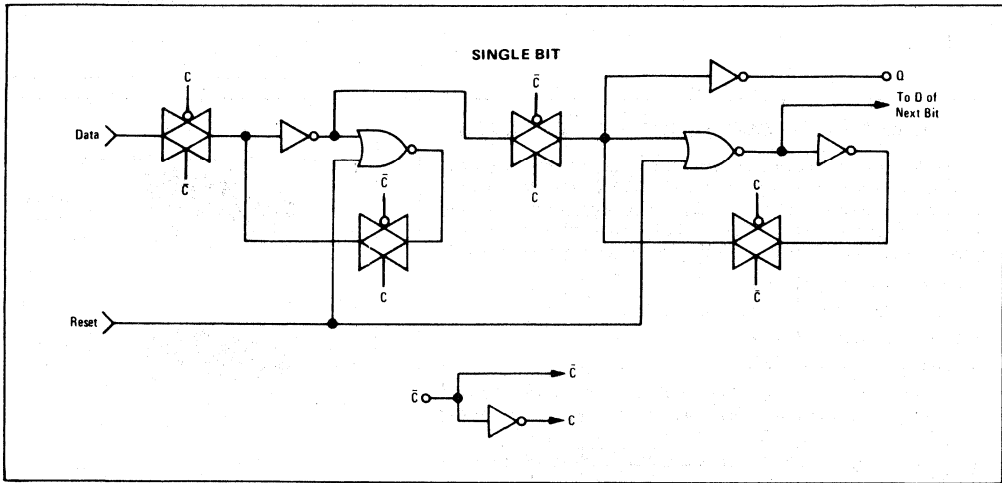
MC14015B

CIRCUIT SCHEMATICS



MC14015B

LOGIC DIAGRAMS



6

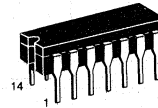


MC14016B

QUAD ANALOG SWITCH/QUAD MULTIPLEXER

The MC14016B quad bilateral switch is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. Each MC14016B consists of four independent switches capable of controlling either digital or analog signals. The quad bilateral switch is used in signal gating, chopper, modulator, demodulator and CMOS logic implementation.

- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Linearized Transfer Characteristics
- Low Noise — $12 \text{ nV}/\sqrt{\text{Cycle}}$, $f \geq 1.0 \text{ kHz}$ typical
- Pin-for-Pin Replacements for CD4016B, CD4066B (Note improved transfer characteristic design causes more parasitic coupling capacitance than CD4016)
- For Lower R_{ON} , Use The HC4016 High-Speed CMOS Device or The MC14066B
- This Device Has Inputs and Outputs Which Do Not Have ESD Protection. Antistatic Precautions Must Be Taken.



L SUFFIX
CERAMIC
CASE 632



P SUFFIX
PLASTIC
CASE 646



D SUFFIX
SOIC
CASE 751A

ORDERING INFORMATION

MC14XXXBCP Plastic
MC14XXXBCL Ceramic
MC14XXXBD SOIC

$T_A = -55^\circ$ to 125°C for all packages.

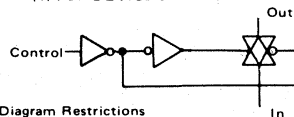
MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	-0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	-0.5 to $V_{DD} + 0.5$	V
I_{in}	Input Current (DC or Transient), per Control Pin	± 10	mA
I_{sw}	Switch Through Current	± 25	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	-65 to +150	$^\circ\text{C}$
T_L	Lead Temperature (8-Second Soldering)	260	$^\circ\text{C}$

*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P and D/DW" Packages: -7.0 mW/ $^\circ\text{C}$ From 65°C To 125°C
Ceramic "L" Packages: -12 mW/ $^\circ\text{C}$ From 100°C To 125°C

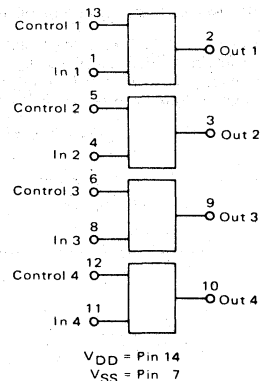
This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

LOGIC DIAGRAM (1/4 OF DEVICE SHOWN)



Logic Diagram Restrictions
 $V_{SS} \leq V_{in} \leq V_{DD}$
 $V_{SS} < V_{out} \leq V_{DD}$

BLOCK DIAGRAM



CONTROL	SWITCH
0 = V_{SS}	OFF
1 = V_{DD}	ON

MC14016B

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Figure	Symbol	V _{DD} Vdc	-55°C		25°C			125°C		Unit	
				Min	Max	Min	Typ #	Max	Min	Max		
Input Voltage Control Input	1	V _{IL}	5.0	—	—	—	1.5	0.9	—	—	Vdc	
			10	—	—	—	1.5	0.9	—	—		
			15	—	—	—	1.5	0.9	—	—		
		V _{IH}	5.0	—	—	3.0	2.0	—	—	—	Vdc	
			10	—	—	8.0	6.0	—	—	—		
			15	—	—	13	11	—	—	—		
Input Current Control	—	I _{in}	15	—	±0.1	—	±0.0001	±0.1	—	±1.0	μAdc	
Input Capacitance Control Switch Input Switch Output Feed Through	—	C _{in}	—	—	—	—	5.0	—	—	—	—	pF
			—	—	—	—	5.0	—	—	—	—	
			—	—	—	—	5.0	—	—	—	—	
			—	—	—	—	0.2	—	—	—	—	
Quiescent Current (Per Package)	2,3	I _{DD}	5.0	—	0.25	—	0.0005	0.25	—	7.5	μAdc	
			10	—	0.5	—	0.0010	0.5	—	15		
			15	—	1.0	—	0.0015	1.0	—	30		
"ON" Resistance (V _C = V _{DD} , R _L = 10 kΩ) (V _{in} = +5.0 Vdc) (V _{in} = -5.0 Vdc) V _{SS} = -5.0 Vdc (V _{in} = ±0.25 Vdc) (V _{in} = +7.5 Vdc) (V _{in} = -7.5 Vdc) V _{SS} = -7.5 Vdc (V _{in} = ±0.25 Vdc) (V _{in} = +10 Vdc) (V _{in} = +0.25 Vdc) V _{SS} = 0 Vdc (V _{in} = +5.6 Vdc) (V _{in} = +15 Vdc) (V _{in} = +0.25 Vdc) V _{SS} = 0 Vdc (V _{in} = +9.3 Vdc)	4,5,6	R _{ON}	—	—	—	—	—	—	—	—	Ohms	
			—	600	—	300	660	—	840			
			—	600	—	300	660	—	840			
			5.0	600	—	280	660	—	840			
			—	360	—	240	400	—	520			
			—	360	—	240	400	—	520			
			7.5	360	—	180	400	—	520			
			—	600	—	260	660	—	840			
			—	600	—	310	660	—	840			
			10	600	—	310	660	—	840			
			—	360	—	260	400	—	520			
			—	360	—	260	400	—	520			
15	360	—	300	400	—	520						
Δ"ON" Resistance Between any 2 circuits in a common package (V _C = V _{DD}) (V _{in} = ±5.0 Vdc) V _{SS} = -5.0 Vdc (V _{in} = ±7.5 Vdc) V _{SS} = -7.5 Vdc	—	ΔR _{ON}	—	—	—	—	—	—	—	—	Ohms	
			5.0	—	—	—	15	—	—	—		
			7.5	—	—	—	10	—	—	—		
Input/Output Leakage Current (V _C = V _{SS}) (V _{in} = +7.5, V _{out} = -7.5 Vdc) (V _{in} = -7.5, V _{out} = +7.5 Vdc)	—	—	7.5	—	±0.1	—	±0.0015	±0.1	—	+1.0	μAdc	
			7.5	—	±0.1	—	±0.0015	±0.1	—	±1.0		

NOTE: All unused inputs must be returned to V_{DD} or V_{SS} as appropriate for the circuit application.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**For voltage drops across the switch (ΔV_{switch}) >600 mV (>300 mV at high temperature), excessive V_{DD} current may be drawn; i.e., the current out of the switch may contain both V_{DD} and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded. (See first page of this data sheet.) Reference Figure 14.

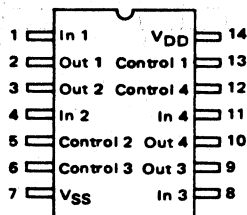
MC14016B

ELECTRICAL CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Figure	Symbol	VDD Vdc	Min	Typ #	Max	Unit	
Propagation Delay Time (V _{SS} = 0 Vdc) V _{in} to V _{out} (V _C = V _{DD} , R _L = 10 kΩ)	7	t _{PLH}	5.0	—	15	45	ns	
		t _{PHL}	10	—	7.0	15		
			15	—	6.0	12		
Control to Output (V _{in} ≤ 10 Vdc, R _L = 10 kΩ)	8	t _{PHZ}	5.0	—	34	90	ns	
		t _{PLZ}	10	—	20	45		
		t _{PZH}	15	—	15	35		
		t _{PZL}	15	—	15	35		
Crosstalk, Control to Output (V _{SS} = 0 Vdc) (V _C = V _{DD} , R _{in} = 10 kΩ, R _{out} = 10 kΩ, f = 1.0 kHz)	9	—	5.0	—	30	—	mV	
			10	—	50	—		
			15	—	100	—		
Crosstalk between any two switches (V _{SS} = 0 Vdc) (R _L = 1.0 kΩ, f = 1.0 MHz, crosstalk = 20 log ₁₀ $\frac{V_{out1}}{V_{out2}}$)	—	—	5.0	—	-80	—	dB	
Noise Voltage (V _{SS} = 0 Vdc) (V _C = V _{DD} , f = 100 Hz) (V _C = -V _{DD} , f = 100 kHz)	10,11	—	5.0	—	24	—	nV/√Cycle	
			10	—	25	—		
			15	—	30	—		
			5.0	—	12	—		
			10	—	12	—		
			15	—	15	—		
Second Harmonic Distortion (V _{SS} = -5.0 Vdc) (V _{in} = 1.77 Vdc, RMS Centered @ 0.0 Vdc, R _L = 10 kΩ, f = 1.0 kHz)	—	—	5.0	—	0.16	—	%	
Insertion Loss (V _C = V _{DD} , V _{in} = 1.77 Vdc, V _{SS} = -5.0 Vdc, RMS centered = 0.0 Vdc, f = 1.0 MHz) $I_{loss} = 20 \log_{10} \frac{V_{out}}{V_{in}}$ (R _L = 1.0 kΩ) (R _L = 10 kΩ) (R _L = 100 kΩ) (R _L = 1.0 MΩ)	12	—	5.0	—	—	—	dB	
					—	2.3		—
					—	0.2		—
					—	0.1		—
					—	0.05		—
Bandwidth (-3.0 dB) (V _C = V _{DD} , V _{in} = 1.77 Vdc, V _{SS} = -5.0 Vdc, RMS centered @ 0.0 Vdc) (R _L = 1.0 kΩ) (R _L = 10 kΩ) (R _L = 100 kΩ) (R _L = 1.0 MΩ)	12,13	BW	5.0	—	—	—	MHz	
					—	54		—
					—	40		—
					—	38		—
					—	37		—
OFF Channel Feedthrough Attenuation (V _{SS} = -5.0 Vdc) (V _C = V _{SS} , 20 log ₁₀ $\frac{V_{out}}{V_{in}}$ = -50 dB) (R _L = 1.0 kΩ) (R _L = 10 kΩ) (R _L = 100 kΩ) (R _L = 1.0 MΩ)	—	—	5.0	—	—	—	kHz	
					—	1250		—
					—	140		—
					—	18		—
					—	2.0		—

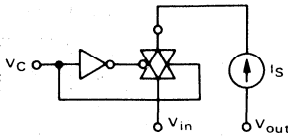
*Data labeled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

PIN ASSIGNMENT



MC14016B

FIGURE 1 – INPUT VOLTAGE TEST CIRCUIT



V_{IL} : V_C is raised from V_{SS} until $V_C = V_{IL}$.
 at $V_C = V_{IL}$: $I_S = \pm 10 \mu A$ with $V_{in} = V_{SS}$, $V_{out} = V_{DD}$ or $V_{in} = V_{DD}$, $V_{out} = V_{SS}$.

V_{IH} : When $V_C = V_{IH}$ to V_{DD} , the switch is ON and the R_{ON} specifications are met.

FIGURE 2 – QUIESCENT POWER DISSIPATION TEST CIRCUIT

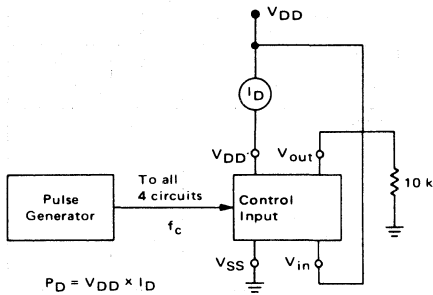
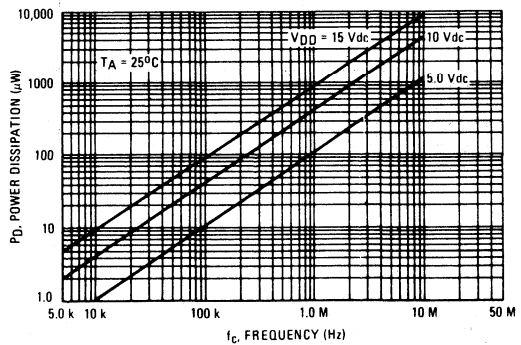


FIGURE 3 – TYPICAL POWER DISSIPATION PER CIRCUIT (1/4 OF DEVICE SHOWN)



TYPICAL R_{ON} versus INPUT VOLTAGE

FIGURE 4 – $V_{SS} = -5.0 V$ AND $-7.5 V$

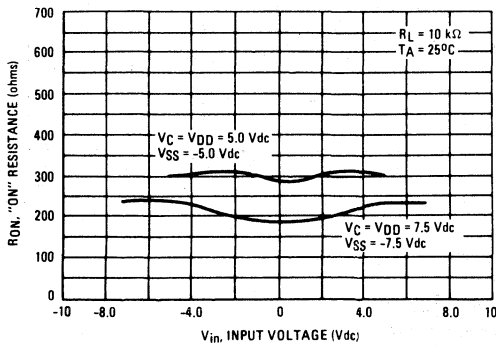
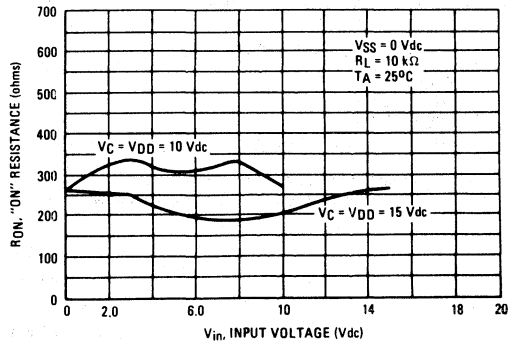


FIGURE 5 – $V_{SS} = 0 V$



MC14016B

FIGURE 6 – R_{ON} CHARACTERISTICS TEST CIRCUIT

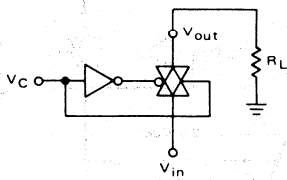


FIGURE 7 – PROPAGATION DELAY TEST CIRCUIT AND WAVEFORMS

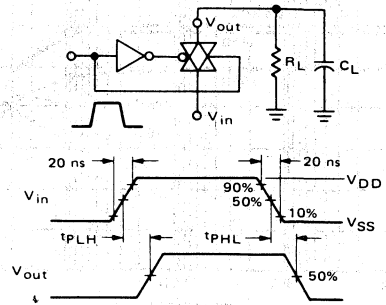


FIGURE 8 – TURN-ON DELAY TIME TEST CIRCUIT AND WAVEFORMS

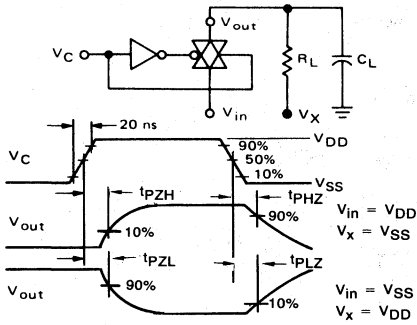


FIGURE 9 – CROSSTALK TEST CIRCUIT

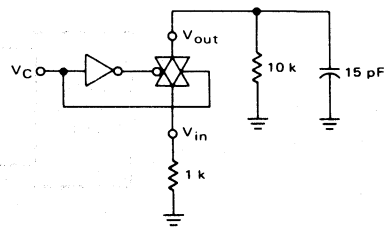


FIGURE 10 – NOISE VOLTAGE TEST CIRCUIT

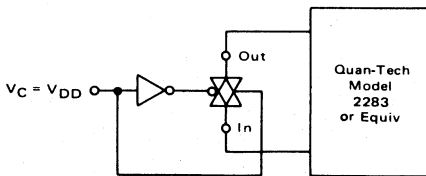
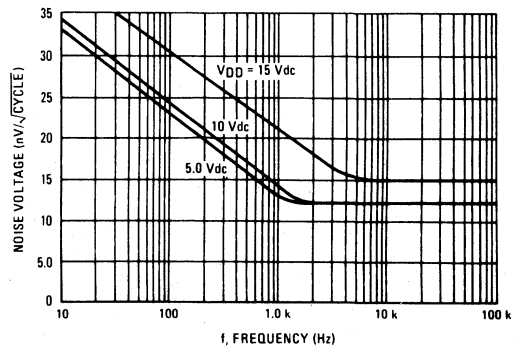


FIGURE 11 – TYPICAL NOISE CHARACTERISTICS



MC14016B

FIGURE 12 – TYPICAL INSERTION LOSS/BANDWIDTH CHARACTERISTICS

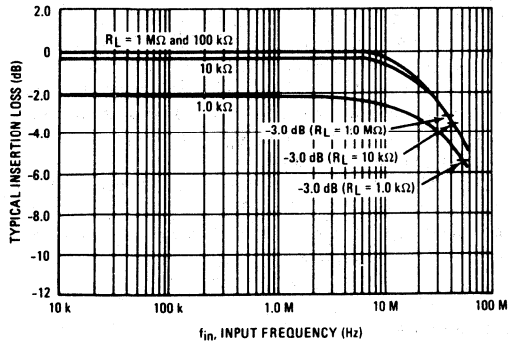


FIGURE 13 – FREQUENCY RESPONSE TEST CIRCUIT

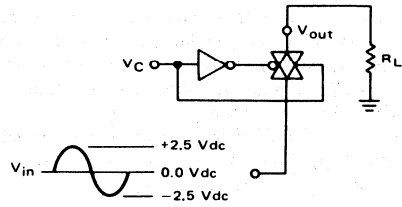
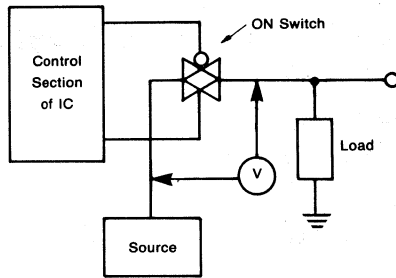


FIGURE 14 – ΔV ACROSS SWITCH



MC14016B

APPLICATIONS INFORMATION

Figure A illustrates use of the Analog Switch. The 0-to-5 V Digital Control signal is used to directly control a 5 V_{p-p} analog signal.

The digital control logic levels are determined by V_{DD} and V_{SS}. The V_{DD} voltage is the logic high voltage; the V_{SS} voltage is logic low. For the example, V_{DD} = +5V = logic high at the control inputs; V_{SS} = GND = 0V = logic low.

The maximum analog signal level is determined by V_{DD} and V_{SS}. The analog voltage must not swing higher than V_{DD} or lower than V_{SS}.

The example shows a 5 V_{p-p} signal which allows no margin at either peak. If voltage transients above V_{DD} and/or below V_{SS} are anticipated on the analog channels, external diodes (D_x) are recommended as shown in Figure B. These diodes should be small signal types able to absorb the maximum anticipated current surges during clipping.

The *absolute* maximum potential difference between V_{DD} and V_{SS} is 18.0V. Most parameters are specified up to 15V which is the *recommended* maximum difference between V_{DD} and V_{SS}.

FIGURE A — APPLICATION EXAMPLE

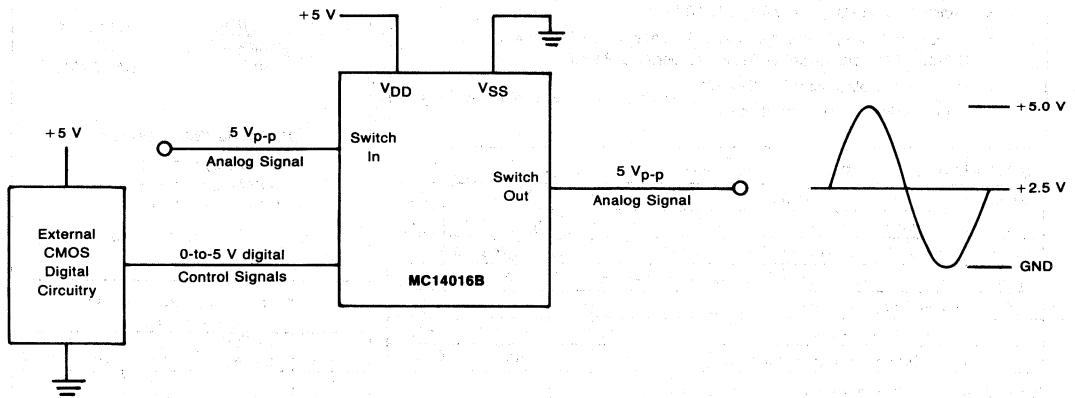
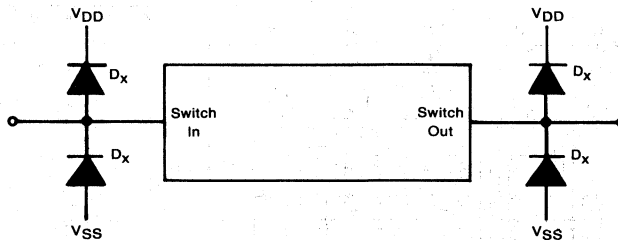


FIGURE B — EXTERNAL GERMANIUM OR SCHOTTKY CLIPPING DIODES





MOTOROLA

MC14017B

DECADE COUNTER

The MC14017B is a five-stage Johnson decade counter with built-in code converter. High speed operation and spike-free outputs are obtained by use of a Johnson decade counter design. The ten decoded outputs are normally low, and go high only at their appropriate decimal time period. The output changes occur on the positive-going edge of the clock pulse. This part can be used in frequency division applications as well as decade counter or decimal decode display applications.

- Fully Static Operation
- DC Clock Input Circuit Allows Slow Rise Times
- Carry Out Output for Cascading
- Divide-by-N Counting
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range
- Pin-for-Pin Replacement for CD4017B
- Triple Diode Protection on All Inputs

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V _{DD}	DC Supply Voltage	-0.5 to +18.0	V
V _{in} , V _{out}	Input or Output Voltage (DC or Transient)	-0.5 to V _{DD} + 0.5	V
I _{in} , I _{out}	Input or Output Current (DC or Transient), per Pin	± 10	mA
P _D	Power Dissipation, per Package†	500	mW
T _{stg}	Storage Temperature	-65 to +150	°C
T _L	Lead Temperature (8-Second Soldering)	260	°C

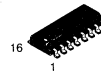
*Maximum Ratings are those values beyond which damage to the device may occur.
 †Temperature Derating: Plastic "P and D/DW" Packages: -7.0 mW/°C From 65°C To 125°C
 Ceramic "L" Packages: -12 mW/°C From 100°C To 125°C



L SUFFIX
CERAMIC
CASE 620



P SUFFIX
PLASTIC
CASE 648



D SUFFIX
SOIC
CASE 751B

ORDERING INFORMATION

- MC14XXXBCP Plastic
- MC14XXXBCL Ceramic
- MC14XXXBD SOIC

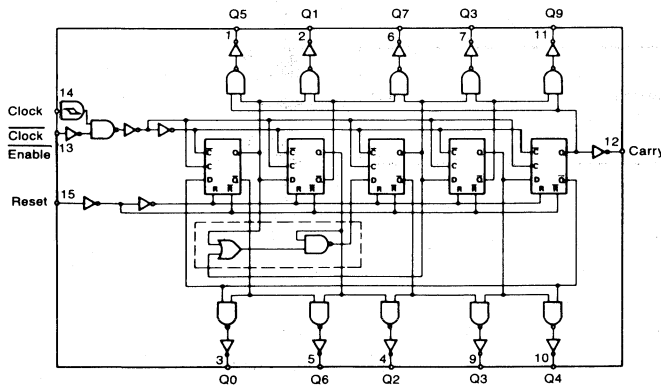
T_A = -55° to 125°C for all packages.

FUNCTIONAL TRUTH TABLE
(Positive Logic)

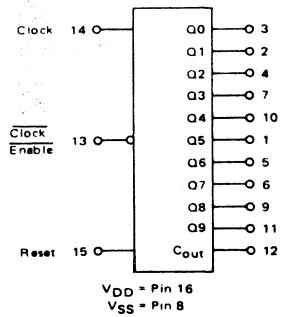
CLOCK	CLOCK ENABLE	RESET	DECODE OUTPUT : n
0	X	0	n
X	1	0	n
X	X	1	Q0
X	0	0	n+1
X	X	0	n
X	X	0	n
1	X	0	n+1

X = "Don't Care" if n < 5 Carry = "1", Otherwise = "0"

LOGIC DIAGRAM



BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

MC14017B

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V _{DD} Vdc	-55°C		25°C			125°C		Unit
			Min	Max	Min	Typ #	Max	Min	Max	
Output Voltage V _{in} = V _{DD} or 0	V _{OL}	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
		10	—	0.05	—	0	0.05	—	0.05	
V _{in} = 0 or V _{DD}	V _{OH}	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc
		10	9.95	—	9.95	10	—	9.95	—	
Input Voltage (V _O = 4.5 or 0.5 Vdc) (V _O = 9.0 or 1.0 Vdc) (V _O = 13.5 or 1.5 Vdc)	V _{IL}	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc
		10	—	3.0	—	4.50	3.0	—	3.0	
(V _O = 0.5 or 4.5 Vdc) (V _O = 1.0 or 9.0 Vdc) (V _O = 1.5 or 13.5 Vdc)	V _{IH}	5.0	3.5	—	3.5	2.75	—	3.5	—	Vdc
		10	7.0	—	7.0	5.50	—	7.0	—	
Output Drive Current (V _{OH} = 2.5 Vdc) (V _{OH} = 4.6 Vdc) (V _{OH} = 9.5 Vdc) (V _{OH} = 13.5 Vdc)	Source	I _{OH}	5.0	-3.0	—	-2.4	—	-1.7	—	mAdc
	Sink		5.0	-0.64	—	-0.51	-0.88	—	-0.36	
(V _{OL} = 0.4 Vdc) (V _{OL} = 0.5 Vdc) (V _{OL} = 1.5 Vdc)		I _{OL}	10	-1.6	—	-1.3	-2.25	—	-0.9	—
	15		-4.2	—	-3.4	-8.8	—	-2.4	—	
Input Current	I _{in}	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	μAdc
Input Capacitance (V _{in} = 0)	C _{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)	I _{DD}	5.0	—	5.0	—	0.005	5.0	—	150	μAdc
		10	—	10	—	0.010	10	—	300	
		15	—	20	—	0.015	20	—	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C _L = 50 pF on all outputs, all buffers switching)	I _T	5.0	I _T = (0.27 μA/kHz) f + I _{DD}							μAdc
10	I _T = (0.55 μA/kHz) f + I _{DD}									
15	I _T = (0.83 μA/kHz) f + I _{DD}									

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

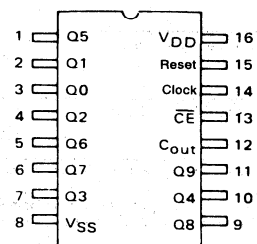
**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) Vfk$$

where: I_T is in μA (per package), C_L in pF, V = (V_{DD} - V_{SS}) in volts, f in kHz is input frequency, and k = 0.0011.

PIN ASSIGNMENT



This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper op-

eration, V_{in} and V_{out} should be constrained to the range V_{SS} ≤ (V_{in} or V_{out}) ≤ V_{DD}. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

MC14017B

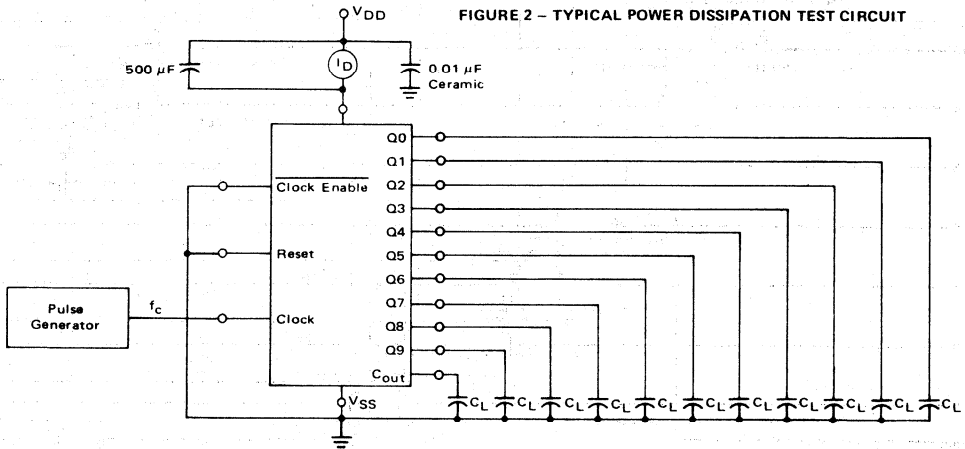
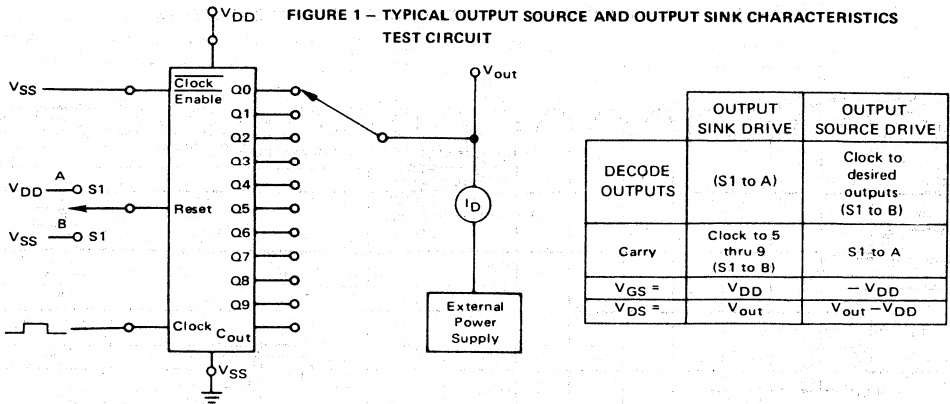
SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	VDD Vdc	Min	Typ #	Max	Unit
Output Rise and Fall Time t _{TLH} , t _{THL} = (1.5 ns/pF) C _L + 25 ns t _{TLH} , t _{THL} = (0.75 ns/pF) C _L + 12.5 ns t _{TLH} , t _{THL} = (0.55 ns/pF) C _L + 9.5 ns	t _{TLH} , t _{THL}	5.0 10 15	— — —	100 50 40	200 100 80	ns
Propagation Delay Time Reset to Decade Output t _{PLH} , t _{PHL} = (1.7 ns/pF) C _L + 415 ns t _{PLH} , t _{PHL} = (0.66 ns/pF) C _L + 197 ns t _{PLH} , t _{PHL} = (0.5 ns/pF) C _L + 150 ns	t _{PLH} , t _{PHL}	5.0 10 15	— — —	500 230 175	1000 460 350	ns
Propagation Delay Time Clock to C _{out} t _{PLH} , t _{PHL} = (1.7 ns/pF) C _L + 315 ns t _{PLH} , t _{PHL} = (0.66 ns/pF) C _L + 142 ns t _{PLH} , t _{PHL} = (0.5 ns/pF) C _L + 100 ns	t _{PLH} , t _{PHL}	5.0 10 15	— — —	400 175 125	800 350 250	ns
Propagation Delay Time Clock to Decode Output t _{PLH} , t _{PHL} = (1.7 ns/pF) C _L + 415 ns t _{PLH} , t _{PHL} = (0.66 ns/pF) C _L + 197 ns t _{PLH} , t _{PHL} = (0.5 ns/pF) C _L + 150 ns	t _{PLH} , t _{PHL}	5.0 10 15	— — —	500 230 175	1000 460 350	ns
Turn-Off Delay Time Reset to C _{out} t _{PLH} = (1.7 ns/pF) C _L + 315 ns t _{PLH} = (0.66 ns/pF) C _L + 142 ns t _{PLH} = (0.5 ns/pF) C _L + 100 ns	t _{PLH}	5.0 10 15	— — —	400 175 125	800 350 250	ns
Clock Pulse Width	t _{w(H)}	5.0 10 15	250 100 75	125 50 35	— — —	ns
Clock Frequency	f _{cl}	5.0 10 15	— — —	5.0 12 16	2.0 5.0 6.7	MHz
Reset Pulse Width	t _{w(H)}	5.0 10 15	500 250 190	250 125 95	— — —	ns
Reset Removal Time	t _{rem}	5.0 10 15	750 275 210	375 135 105	— — —	ns
Clock Input Rise and Fall Time	t _{TLH} , t _{THL}	5.0 10 15	No Limit			—
Clock Enable Setup Time	t _{su}	5.0 10 15	350 150 115	175 75 52	— — —	ns
Clock Enable Removal Time	t _{rem}	5.0 10 15	420 200 140	260 100 70	— — —	ns

*The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

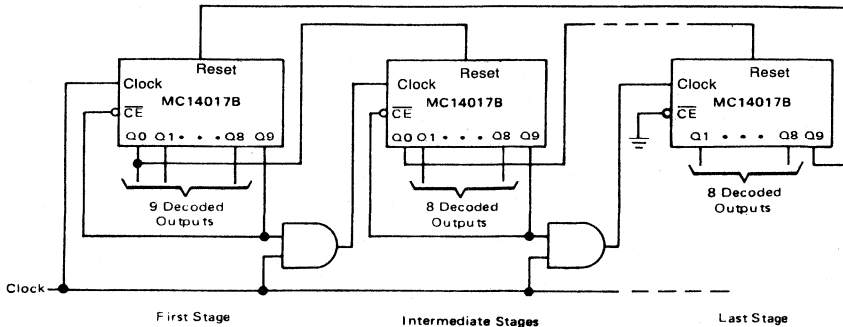
MC14017B



APPLICATIONS INFORMATION

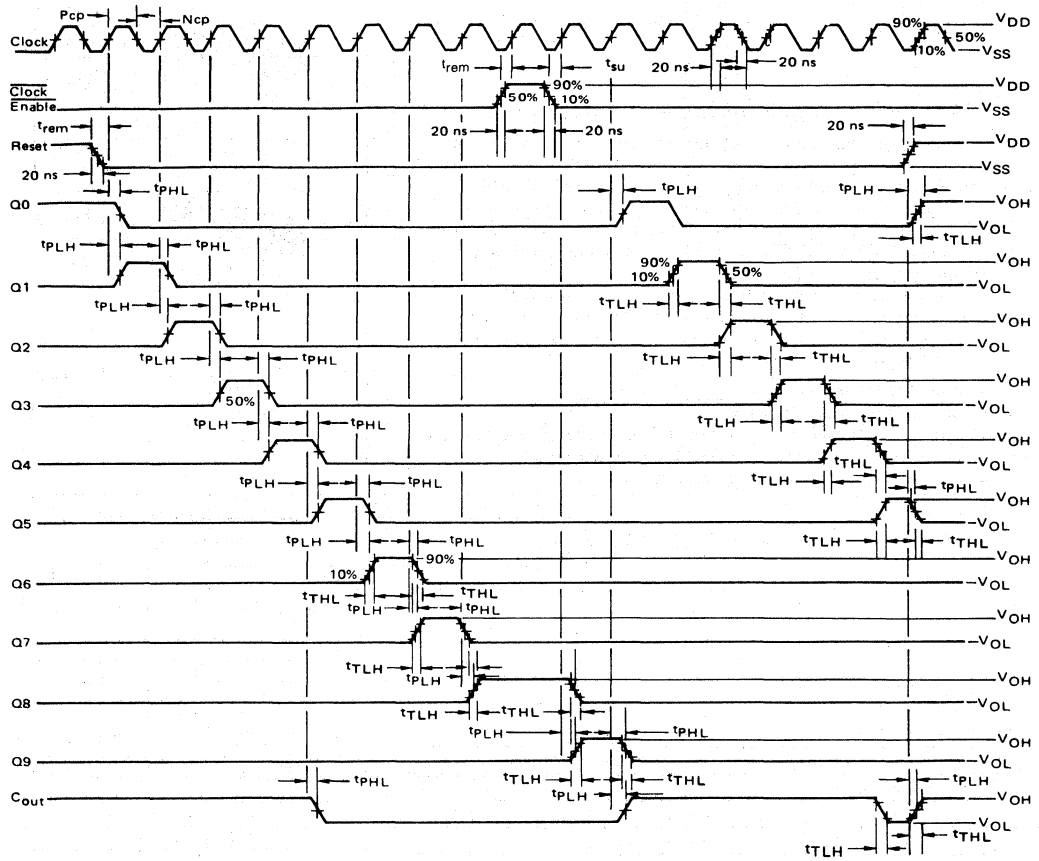
Figure 3 shows a technique for extending the number of decoded output states for the MC14017B. Decoded outputs are sequential within each stage and from stage to stage, with no dead time (except propagation delay).

FIGURE 3 – COUNTER EXPANSION



MC14017B

FIGURE 4 – AC MEASUREMENT DEFINITION AND FUNCTIONAL WAVEFORMS



6



MOTOROLA

PRESETTABLE DIVIDE-BY-N COUNTER

The MC14018B contains five Johnson counter stages which are asynchronously presettable and resettable. The counters are synchronous, and increment on the positive going edge of the clock.

Presetting is accomplished by a logic 1 on the preset enable input. Data on the Jam inputs will then be transferred to their respective \bar{Q} outputs (inverted). A logic 1 on the reset input will cause all \bar{Q} outputs to go to a logic 1 state.

Division by any number from 2 to 10 can be accomplished by connecting appropriate \bar{Q} outputs to the data input, as shown in the Function Selection table. Anti-lock gating is included in the MC14018B to assure proper counting sequence.

- Fully Static Operation
- Schmitt Trigger on Clock Input
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range
- Pin-for-Pin Replacement for CD4018B

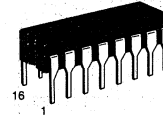
MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	-0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	-0.5 to $V_{DD} + 0.5$	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	± 10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

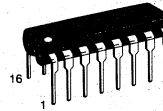
*Maximum Ratings are those values beyond which damage to the device may occur.
 †Temperature Derating: Plastic "P and D/DW" Packages: -7.0 mW/°C From 65°C To 125°C
 Ceramic "L" Packages: -12 mW/°C From 100°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

MC14018B



L SUFFIX
 CERAMIC
 CASE 620



P SUFFIX
 PLASTIC
 CASE 648



D SUFFIX
 SOIC
 CASE 751B

ORDERING INFORMATION

MC14XXXBCP Plastic
 MC14XXXBCL Ceramic
 MC14XXXBD SOIC

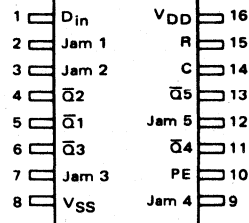
$T_A = -55^\circ \text{ to } 125^\circ \text{C}$ for all packages.

FUNCTIONAL TRUTH TABLE

Clock	Reset	Preset Enable	Jam Input	\bar{Q}_n
	0	0	X	\bar{Q}_n
	0	0	X	\bar{D}_n^*
X	0	1	0	1
X	0	1	1	0
X	1	X	X	1

* D_n is the Data input for that stage. Stage 1 has Data brought out to Pin 1.

PIN ASSIGNMENT



MC14018B

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V _{DD} Vdc	-55°C		25°C			125°C		Unit	
			Min	Max	Min	Typ #	Max	Min	Max		
Output Voltage V _{in} = V _{DD} or 0	V _{OL}	5.0	—	0.05	—	0	0.05	—	0.05	Vdc	
		10	—	0.05	—	0	0.05	—	0.05		
15		—	0.05	—	0	0.05	—	0.05			
V _{in} = 0 or V _{DD}	V _{OH}	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc	
		10	9.95	—	9.95	10	—	9.95	—		
		15	14.95	—	14.95	15	—	14.95	—		
Input Voltage (V _O = 4.5 or 0.5 Vdc) (V _O = 9.0 or 1.0 Vdc) (V _O = 13.5 or 1.5 Vdc)	V _{IL}	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc	
		10	—	3.0	—	4.50	3.0	—	3.0		
	V _{IH}	5.0	3.5	—	3.5	2.75	—	3.5	—	Vdc	
		10	7.0	—	7.0	5.50	—	7.0	—		
Output Drive Current (V _{OH} = 2.5 Vdc) (V _{OH} = 4.6 Vdc) (V _{OH} = 9.5 Vdc) (V _{OH} = 13.5 Vdc) (V _{OL} = 0.4 Vdc) (V _{OL} = 0.5 Vdc) (V _{OL} = 1.5 Vdc)	Source	I _{OH}	5.0	-3.0	—	-2.4	-4.2	—	-1.7	—	mAdc
			10	-0.64	—	-0.51	-0.88	—	-0.36	—	
			15	-1.6	—	-1.3	-2.25	—	-0.9	—	
	Sink	I _{OL}	5.0	0.64	—	0.51	0.88	—	0.36	—	mAdc
			10	1.6	—	1.3	2.25	—	0.9	—	
			15	4.2	—	3.4	8.8	—	2.4	—	
Input Current	I _{in}	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	μAdc	
Input Capacitance (V _{in} = 0)	C _{in}	—	—	—	—	5.0	7.5	—	—	pF	
Quiescent Current (Per Package)	I _{DD}	5.0	—	5.0	—	0.005	5.0	—	150	μAdc	
10	—	10	—	0.010	10	—	300				
15	—	20	—	0.015	20	—	600				
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C _L = 50 pF on all outputs, all buffers switching)	I _T	5.0	I _T = (0.3 μA/kHz) f + I _{DD} I _T = (0.7 μA/kHz) f + I _{DD} I _T = (1.0 μA/kHz) f + I _{DD}							μAdc	
10											
15											

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) \text{ Vfk}$$

where: I_T is in μA (per package), C_L in pF, V = (V_{DD} - V_{SS}) in volts, f in kHz is input frequency, and k = 0.001.

MC14018B

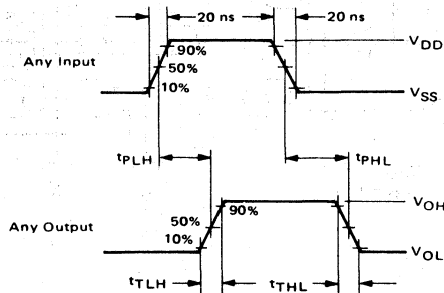
SWITCHING CHARACTERISTICS* ($C_L = 50 \text{ pF}$, $T_A = 25^\circ\text{C}$)

Characteristic	Symbol	V _{DD} V _{dC}	All Types			Unit
			Min	Typ #	Max	
Output Rise and Fall Time $t_{TLH}, t_{THL} = (1.35 \text{ ns/pF}) C_L + 32 \text{ ns}$ $t_{TLH}, t_{THL} = (0.6 \text{ ns/pF}) C_L + 20 \text{ ns}$ $t_{TLH}, t_{THL} = (0.4 \text{ ns/pF}) C_L + 20 \text{ ns}$	t_{TLH}, t_{THL}	5.0 10 15	— — —	100 50 40	200 100 80	ns
Propagation Delay Time Clock to \bar{Q} $t_{PLH}, t_{PHL} = (0.90 \text{ ns/pF}) C_L + 265 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.36 \text{ ns/pF}) C_L + 102 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.26 \text{ ns/pF}) C_L + 72 \text{ ns}$ Reset to \bar{Q} $t_{PLH} = (0.90 \text{ ns/pF}) C_L + 325 \text{ ns}$ $t_{PLH} = (0.36 \text{ ns/pF}) C_L + 132 \text{ ns}$ $t_{PLH} = (0.26 \text{ ns/pF}) C_L + 81 \text{ ns}$ Preset Enable to \bar{Q} $t_{PLH}, t_{PHL} = (0.90 \text{ ns/pF}) C_L + 325 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.36 \text{ ns/pF}) C_L + 132 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.26 \text{ ns/pF}) C_L + 81 \text{ ns}$	t_{PLH}, t_{PHL}	5.0 10 15	— — —	310 120 85	620 240 170	ns
Setup Time Data (Pin 1) to Clock Jam Inputs to Preset Enable	t_{su}	5.0 10 15	200 100 80	0 0 0	— — —	ns
Data (Jam Inputs)-to-Preset Enable Hold Time	t_h	5.0 10 15	540 500 480	270 250 240	— — —	ns
Clock Pulse Width	t_{WH}	5.0 10 15	400 200 160	200 100 80	— — —	ns
Reset or Preset Enable Pulse Width	t_{WH}	5.0 10 15	290 130 110	145 65 55	— — —	ns
Clock Rise and Fall Time	t_{TLH}, t_{THL}	5.0 10 15	No Limit			ns
Clock Pulse Frequency	f_{cl}	5.0 10 15	— — —	2.5 6.5 8.0	1.25 3.25 4.0	MHz

*The formulas given are for typical characteristics only at 25°C.

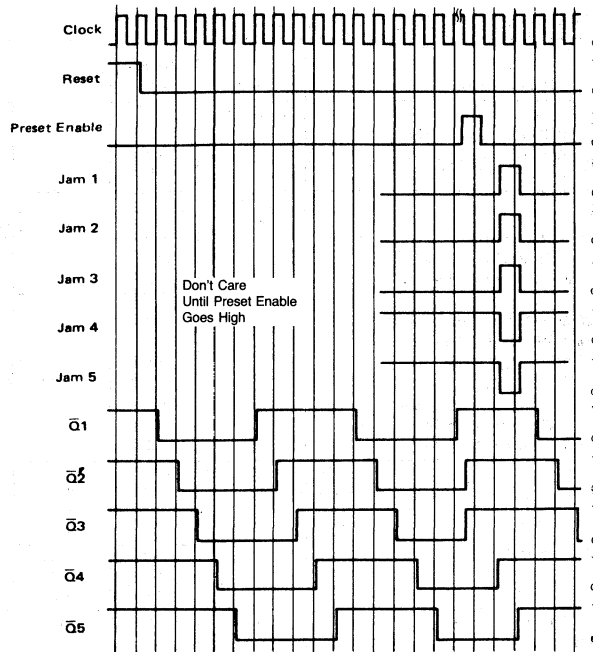
#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

FIGURE 1 – SWITCHING TIME WAVEFORMS



MC14018B

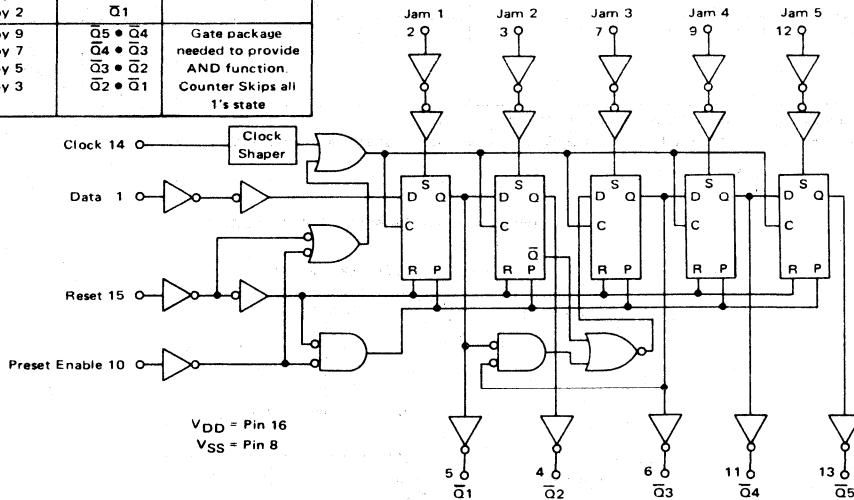
TIMING DIAGRAM
(Q5 Connected to Data Input)



FUNCTION SELECTION

Counter Mode	Connect Data Input (Pin 1) to:	Comments
Divide by 10 Divide by 8 Divide by 6 Divide by 4 Divide by 2	Q5 Q4 Q3 Q2 Q1	No external components needed.
Divide by 9 Divide by 7 Divide by 5 Divide by 3	Q5 * Q4 Q4 * Q3 Q3 * Q2 Q2 * Q1	Gate package needed to provide AND function. Counter Skips all 1's state

LOGIC DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

6



MC14020B

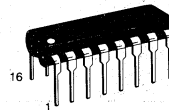
14-BIT BINARY COUNTER

The MC14020B 14-stage binary counter is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. This part is designed with an input wave shaping circuit and 14 stages of ripple-carry binary counter. The device advances the count on the negative-going edge of the clock pulse. Applications include time delay circuits, counter controls, and frequency-dividing circuits.

- Fully Static Operation
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range
- Buffered Outputs Available from stages 1 and 4 thru 14
- Common Reset Line
- Pin-for-Pin Replacement for CD4020B



L SUFFIX
CERAMIC
CASE 620



P SUFFIX
PLASTIC
CASE 648



D SUFFIX
SOIC
CASE 751B

ORDERING INFORMATION

MC14XXXBCP Plastic
MC14XXXBCL Ceramic
MC14XXXBD SOIC

T_A = -55° to 125°C for all packages.

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V _{DD}	DC Supply Voltage	-0.5 to +18.0	V
V _{in} , V _{out}	Input or Output Voltage (DC or Transient)	-0.5 to V _{DD} +0.5	V
I _{in} , I _{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
P _D	Power Dissipation, per Package†	500	mW
T _{stg}	Storage Temperature	-65 to +150	°C
T _L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.

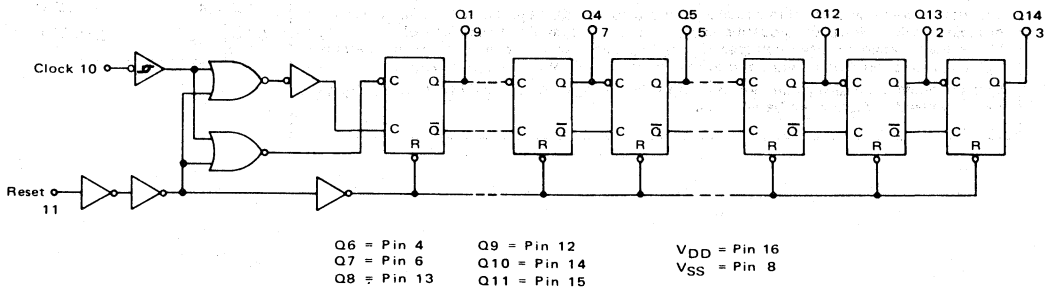
†Temperature Derating: Plastic "P and D/DW" Packages: -7.0 mW/°C From 65°C To 125°C
Ceramic "L" Packages: -12 mW/°C From 100°C To 125°C

TRUTH TABLE

CLOCK	RESET	OUTPUT STATE
	0	No Change
	0	Advance to next state
X	1	All Outputs are low

X = Don't Care

LOGIC DIAGRAM



MC14020B

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V _{DD} Vdc	-55°C		25°C			125°C		Unit
			Min	Max	Min	Typ #	Max	Min	Max	
Output Voltage V _{in} = V _{DD} or 0	V _{OL}	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
		10	—	0.05	—	0	0.05	—	0.05	
		15	—	0.05	—	0	0.05	—	0.05	
V _{in} = 0 or V _{DD}	V _{OH}	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc
		10	9.95	—	9.95	10	—	9.95	—	
		15	14.95	—	14.95	15	—	14.95	—	
Input Voltage (V _O = 4.5 or 0.5 Vdc) (V _O = 9.0 or 1.0 Vdc) (V _O = 13.5 or 1.5 Vdc)	"0" Level V _{IL}	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc
		10	—	3.0	—	4.50	3.0	—	3.0	
		15	—	4.0	—	6.75	4.0	—	4.0	
	"1" Level V _{IH}	5.0	3.5	—	3.5	2.75	—	3.5	—	Vdc
		10	7.0	—	7.0	5.50	—	7.0	—	
		15	11	—	11	8.25	—	11	—	
Output Drive Current (V _{OH} = 2.5 Vdc) (V _{OH} = 4.6 Vdc) (V _{OH} = 9.5 Vdc) (V _{OH} = 13.5 Vdc) (V _{OL} = 0.4 Vdc) (V _{OL} = 0.5 Vdc) (V _{OL} = 1.5 Vdc)	Source I _{OH}	5.0	-3.0	—	-2.4	-4.2	—	-1.7	—	mAdc
		10	-0.64	—	-0.51	-0.88	—	-0.36	—	
		15	-1.6	—	-1.3	-2.25	—	-0.9	—	
	Sink I _{OL}	5.0	0.64	—	0.51	0.88	—	0.36	—	mAdc
		10	1.6	—	1.3	2.25	—	0.9	—	
		15	4.2	—	3.4	8.8	—	2.4	—	
Input Current	I _{in}	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	μAdc
Input Capacitance (V _{in} = 0)	C _{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)	I _{DD}	5.0	—	5.0	—	0.005	5.0	—	150	μAdc
		10	—	10	—	0.010	10	—	300	
		15	—	20	—	0.015	20	—	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C _L = 50 pF on all outputs, all buffers switching)	I _T	5.0	I _T = (0.42 μA/kHz) f + I _{DD}							μAdc
		10	I _T = (0.85 μA/kHz) f + I _{DD}							
		15	I _T = (1.43 μA/kHz) f + I _{DD}							

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C.

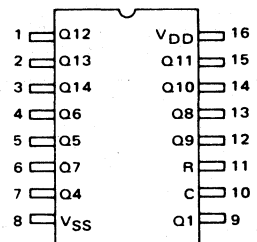
†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) V/k$$

where: I_T is in μA (per package), C_L in pF, V = (V_{DD} - V_{SS}) in volts, f in kHz is input frequency, and k = 0.001.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range V_{SS} ≤ (V_{in} or V_{out}) ≤ V_{DD}. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

PIN ASSIGNMENT



MC14020B

SWITCHING CHARACTERISTICS (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V _{DD} V _{dc}	Min	Typ #	Max	Unit
Output Rise and Fall Time T _{TLH} , T _{THL} = (1.5 ns/pF) C _L + 25 ns T _{TLH} , T _{THL} = (0.75 ns/pF) C _L + 12.5 ns T _{TLH} , T _{THL} = (0.55 ns/pF) C _L + 9.5 ns	t _{TLH} , t _{THL}	5.0 10 15	— — —	100 50 40	200 100 80	ns
Propagation Delay Time Clock to Q1 t _{PHL} , t _{PLH} = (1.7 ns/pF) C _L + 175 ns t _{PHL} , t _{PLH} = (0.66 ns/pF) C _L + 82 ns t _{PHL} , t _{PLH} = (0.5 ns/pF) C _L + 55 ns Clock to Q14 t _{PHL} , t _{PLH} = (1.7 ns/pF) C _L + 1735 ns t _{PHL} , t _{PLH} = (0.66 ns/pF) C _L + 772 ns t _{PHL} , t _{PLH} = (0.5 ns/pF) C _L + 535 ns	t _{PLH} , t _{PHL}	5.0 10 15	— — —	260 115 80	520 230 160	ns
Propagation Delay Time Reset to Q _n t _{PHL} = (1.7 ns/pF) C _L + 285 ns t _{PHL} = (0.66 ns/pF) C _L + 122 ns t _{PHL} = (0.5 ns/pF) C _L + 90 ns	t _{PHL}	5.0 10 15	— — —	370 155 115	740 310 230	ns
Clock Pulse Width	t _{WH}	5.0 10 15	500 165 125	140 55 38	— — —	ns
Clock Pulse Frequency	f _{cl}	5.0 10 15	— — —	2.0 6.0 8.0	1.0 3.0 4.0	MHz
Clock Rise and Fall Time	t _{TLH} , t _{THL}	5.0 10 15	No Limit			—
Reset Pulse Width	t _{WL}	5.0 10 15	3000 550 420	320 120 80	— — —	ns
Reset Removal Time	t _{rem}	5.0 10 15	130 50 30	65 25 15	— — —	ns

*The formulas given are for the typical characteristics only at 25°C.
#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

FIGURE 1 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

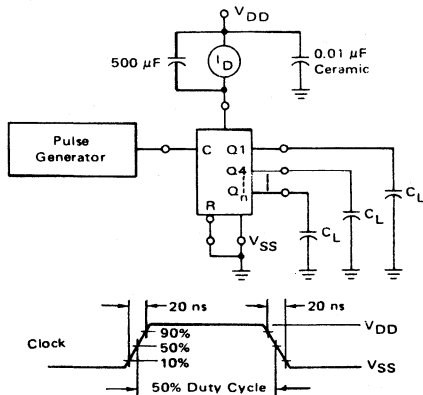
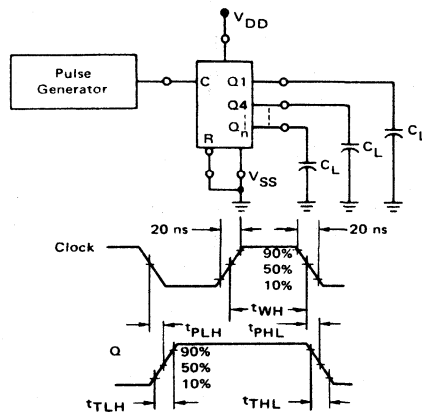
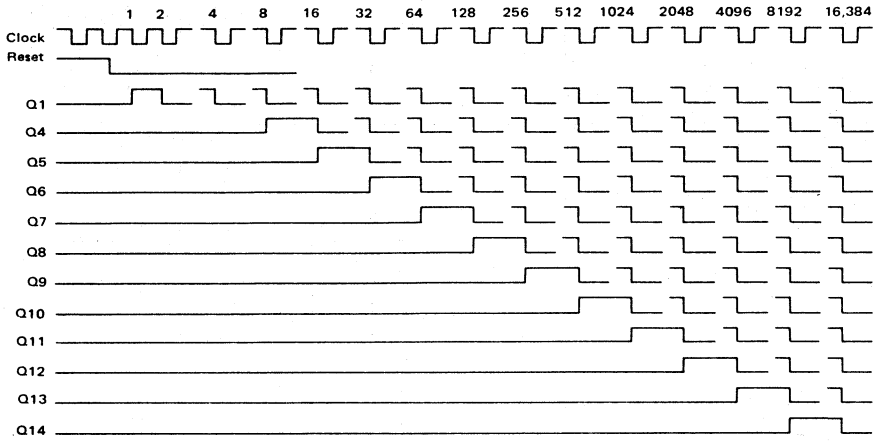


FIGURE 2 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



MC14020B

FIGURE 3 - TIMING DIAGRAM





MOTOROLA

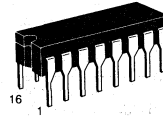
MC14021B
See Page 6-37

MC14022B

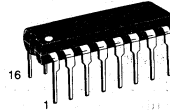
OCTAL COUNTER

The MC14022B is a four-stage Johnson octal counter with built-in code converter. High-speed operation and spike-free outputs are obtained by use of a Johnson octal counter design. The eight decoded outputs are normally low, and go high only at their appropriate octal time period. The output changes occur on the positive-going edge of the clock pulse. This part can be used in frequency division applications as well as octal counter or octal decode display applications.

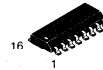
- Fully Static Operation
- DC Clock Input Circuit Allows Slow Rise Times
- Carry Out Output for Cascading
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range
- Pin-for-Pin Replacement for CD4022B
- Triple Diode Protection on All Inputs



L SUFFIX
CERAMIC
CASE 620



P SUFFIX
PLASTIC
CASE 648



D SUFFIX
SOIC
CASE 751B

ORDERING INFORMATION

MC14XXXBCP Plastic
MC14XXXBCL Ceramic
MC14XXXBD SOIC

T_A = -55° to 125°C for all packages.

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V _{DD}	DC Supply Voltage	-0.5 to +18.0	V
V _{in} , V _{out}	Input or Output Voltage (DC or Transient)	-0.5 to V _{DD} + 0.5	V
I _{in} , I _{out}	Input or Output Current (DC or Transient), per Pin	± 10	mA
P _D	Power Dissipation, per Package†	500	mW
T _{stg}	Storage Temperature	-65 to +150	°C
T _L	Lead Temperature (8-Second Soldering)	260	°C

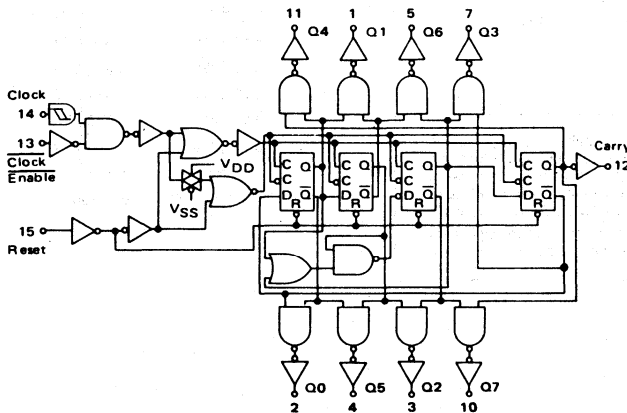
*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P and D/DW" Packages: -7.0 mW/°C From 65°C To 125°C
Ceramic "L" Packages: -12 mW/°C From 100°C To 125°C

FUNCTIONAL TRUTH TABLE
(Positive Logic)

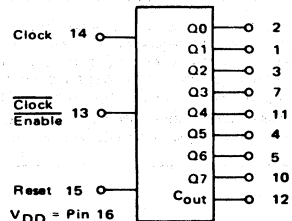
CLOCK	CLOCK ENABLE	RESET	OUTPUT = n
0	X	0	n
X	1	0	n
↘	0	0	n+1
↘	X	0	n
1	↘	0	n+1
X	↘	0	n
X	X	1	Q0

X Don't Care If n < 4 Carry = 1, Otherwise = 0

LOGIC DIAGRAM



BLOCK DIAGRAM



NC = Pin 6,9

6

MC14022B

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	-55°C		25°C			125°C		Unit	
			Min	Max	Min	Typ #	Max	Min	Max		
Output Voltage $V_{in} = V_{DD}$ or 0	V_{OL}	5.0 10 15	—	0.05	—	0	0.05	—	0.05	Vdc	
			—	0.05	—	0	0.05	—	0.05		
—			0.05	—	0	0.05	—	0.05			
$V_{in} = 0$ or V_{DD}	V_{OH}	5.0 10 15	4.95	—	4.95	5.0	—	4.95	—	Vdc	
			9.95	—	9.95	10	—	9.95	—		
			14.95	—	14.95	15	—	14.95	—		
Input Voltage ($V_O = 4.5$ or 0.5 Vdc) ($V_O = 9.0$ or 1.0 Vdc) ($V_O = 13.5$ or 1.5 Vdc)	V_{IL}	5.0 10 15	—	1.5	—	2.25	1.5	—	1.5	Vdc	
			—	3.0	—	4.50	3.0	—	3.0		
—			4.0	—	6.75	4.0	—	4.0			
($V_O = 0.5$ or 4.5 Vdc) ($V_O = 1.0$ or 9.0 Vdc) ($V_O = 1.5$ or 13.5 Vdc)	V_{IH}	5.0 10 15	3.5	—	3.5	2.75	—	3.5	—	Vdc	
			7.0	—	7.0	5.50	—	7.0	—		
			11	—	11	8.25	—	11	—		
Output Drive Current ($V_{OH} = 2.5$ Vdc) ($V_{OH} = 4.6$ Vdc) ($V_{OH} = 9.5$ Vdc) ($V_{OH} = 13.5$ Vdc)	Source	I_{OH}	5.0	-3.0	—	-2.4	-4.2	—	-1.7	—	mAdc
			5.0	-0.64	—	-0.51	-0.88	—	-0.36	—	
($V_{OL} = 0.4$ Vdc) ($V_{OL} = 0.5$ Vdc) ($V_{OL} = 1.5$ Vdc)	Sink	I_{OL}	5.0	0.64	—	0.51	0.88	—	0.36	—	mAdc
			10	1.6	—	1.3	2.25	—	0.9	—	
		15	4.2	—	3.4	8.8	—	2.4	—		
Input Current	I_{in}	15	—	± 0.1	—	± 0.00001	± 0.1	—	± 1.0	μ Adc	
Input Capacitance ($V_{in} = 0$)	C_{in}	—	—	—	—	5.0	7.5	—	—	pF	
Quiescent Current (Per Package)	I_{DD}	5.0	—	5.0	—	0.005	5.0	—	150	μ Adc	
		10	—	10	—	0.010	10	—	300		
		15	—	20	—	0.015	20	—	600		
Total Supply Current**† (Dynamic plus Quiescent, Per Package) ($C_L = 50$ pF on all outputs, all buffers switching)	I_T	5.0	$I_T = (0.28 \mu A/kHz) f + I_{DD}$							μ Adc	
		10	$I_T = (0.56 \mu A/kHz) f + I_{DD}$								
		15	$I_T = (0.85 \mu A/kHz) f + I_{DD}$								

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C.

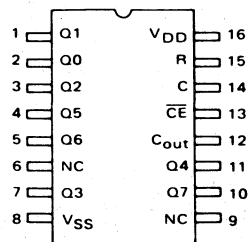
†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) V/k$$

where: I_T is in μA (per package), C_L in pF, $V = (V_{DD} - V_{SS})$ in volts, f in kHz is input frequency, and $k = 0.00125$.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

PIN ASSIGNMENT



NC = No Connection

MC14022B

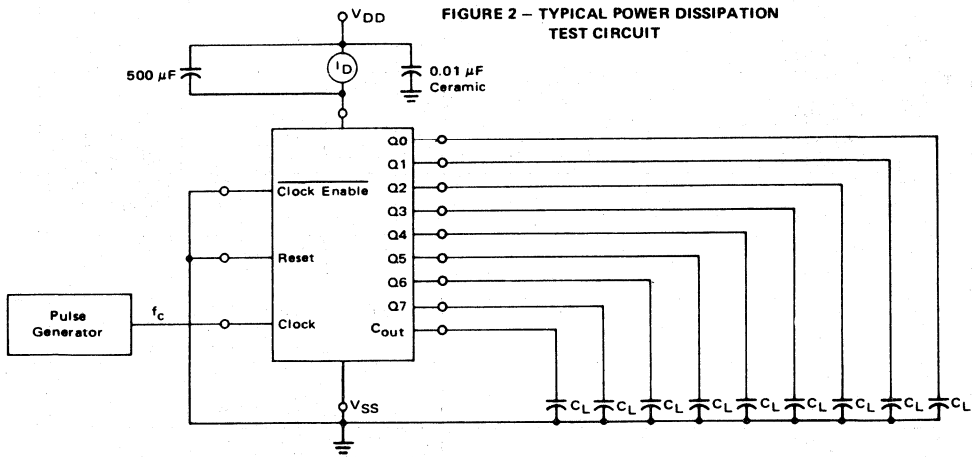
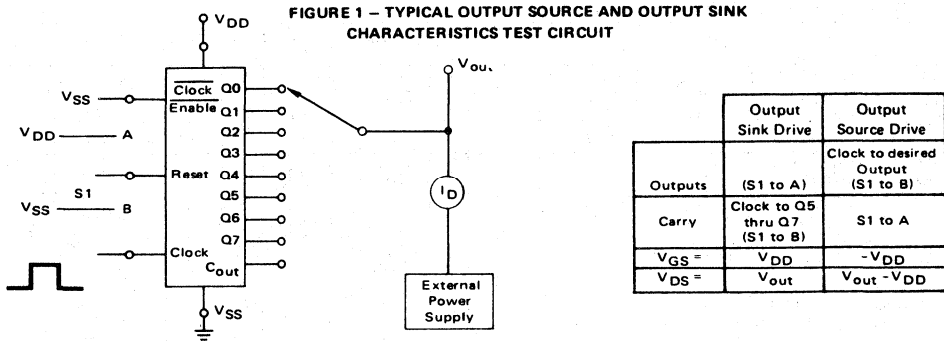
SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V _{DD} V _{dC}	Min	Typ #	Max	Unit
Output Rise and Fall Time t _{TLH} , t _{THL} = (1.5 ns/pF) C _L + 25 ns t _{TLH} , t _{THL} = (0.75 ns/pF) C _L + 12.5 ns t _{TLH} , t _{THL} = (0.55 ns/pF) C _L + 9.5 ns	t _{TLH} , t _{THL}	5.0 10 15	— — —	100 50 40	200 100 80	ns
Propagation Delay Time Reset to Decode Output t _{PLH} , t _{PHL} = (1.7 ns/pF) C _L + 415 ns t _{PLH} , t _{PHL} = (0.66 ns/pF) C _L + 197 ns t _{PLH} , t _{PHL} = (0.5 ns/pF) C _L + 150 ns	t _{PLH} , t _{PHL}	5.0 10 15	— — —	500 230 175	1000 460 350	ns
Propagation Delay Time Clock to C _{out} t _{PLH} , t _{PHL} = (1.7 ns/pF) C _L + 315 ns t _{PLH} , t _{PHL} = (0.66 ns/pF) C _L + 142 ns t _{PLH} , t _{PHL} = (0.5 ns/pF) C _L + 100 ns	t _{PLH} , t _{PHL}	5.0 10 15	— — —	400 175 125	800 350 250	ns
Propagation Delay Time Clock to Decode Output t _{PLH} , t _{PHL} = (1.7 ns/pF) C _L + 415 ns t _{PLH} , t _{PHL} = (0.66 ns/pF) C _L + 197 ns t _{PLH} , t _{PHL} = 0.5 ns/pF C _L + 150 ns	t _{PLH} , t _{PHL}	5.0 10 15	— — —	275 125 95	1000 460 350	ns
Turn-Off Delay Time Reset to C _{out} t _{PLH} = (1.7 ns/pF) C _L + 315 ns t _{PLH} = (0.66 ns/pF) C _L + 142 ns t _{PLH} = (0.5 ns/pF) C _L + 100 ns	t _{PLH}	5.0 10 15	— — —	400 175 125	800 350 250	ns
Clock Pulse Width	t _{WH}	5.0 10 15	250 100 75	125 50 35	— — —	ns
Clock Frequency	f _{cl}	5.0 10 15	— — —	5.0 12 16	2.0 5.0 6.7	MHz
Reset Pulse Width	t _{WH}	5.0 10 15	500 250 190	250 125 95	— — —	ns
Reset Removal Time	t _{rem}	5.0 10 15	750 275 210	375 135 105	— — —	ns
Clock Input Rise and Fall Time	t _{TLH} , t _{THL}	5.0 10 15	No Limit			—
Clock Enable Setup Time	t _{su}	5.0 10 15	350 150 115	175 75 52	— — —	ns
Clock Enable Removal Time	t _{rem}	5.0 10 15	420 200 140	260 100 70	— — —	ns

*The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

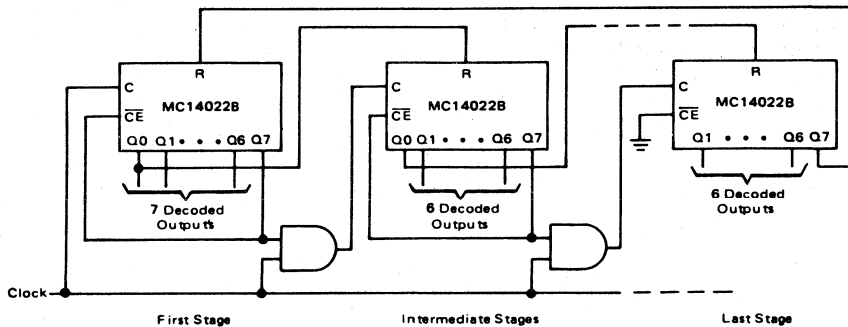
MC14022B



APPLICATIONS INFORMATION

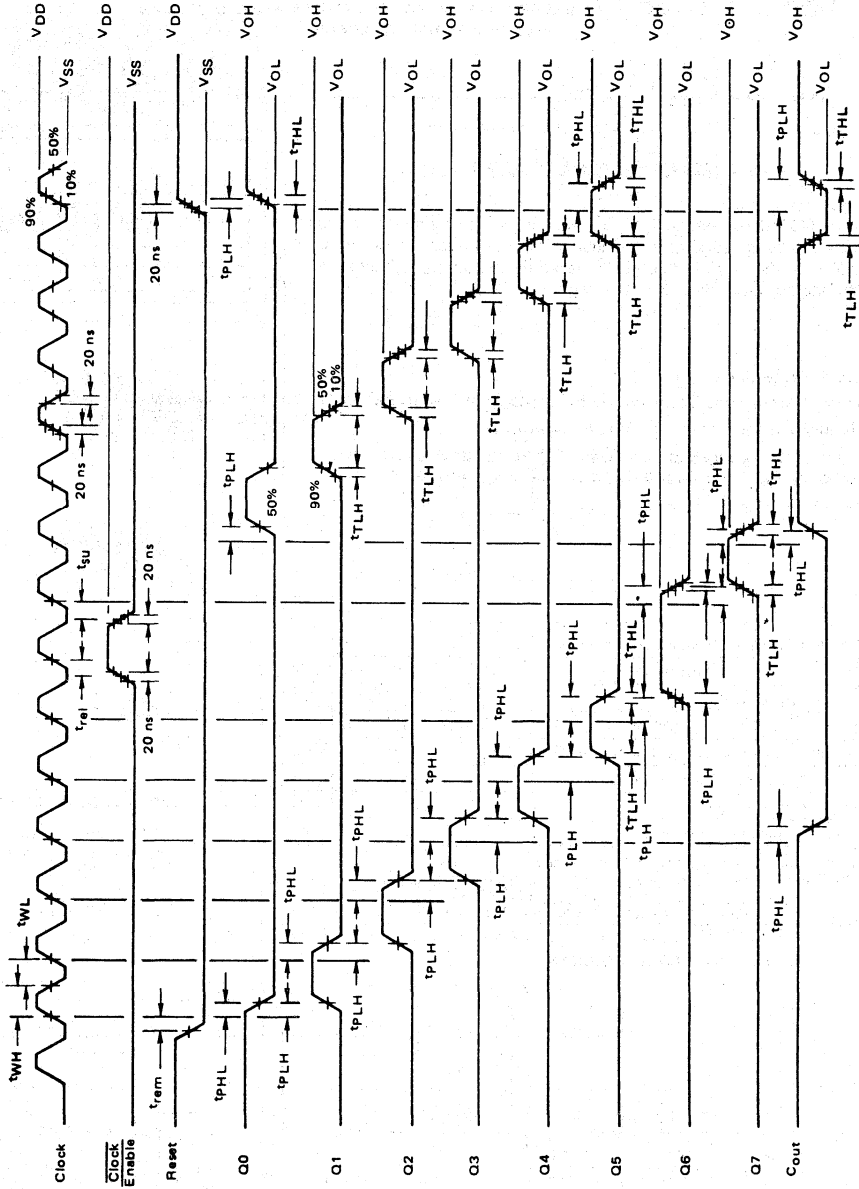
Figure 3 shows a technique for extending the number of decoded output states for the MC14022B. Decoded outputs are sequential within each stage and from stage to stage, with no dead time (except propagation delay).

FIGURE 3 – COUNTER EXPANSION



6

FIGURE 4 - AC MEASUREMENT DEFINITION AND FUNCTIONAL WAVEFORMS





MOTOROLA

MC14023B
See Page 6-5

MC14023UB
See Page 6-14

7-STAGE RIPPLE COUNTER

The MC14024B is a 7-stage ripple counter with short propagation delays and high maximum clock rates. The Reset input has standard noise immunity, however the Clock input has increased noise immunity due to Hysteresis. The output of each counter stage is buffered.

- Diode Protection on All Inputs
- Output Transitions Occur on the Falling Edge of the Clock Pulse
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range
- Pin-for-Pin Replacement for CD4024B

MC14024B



L SUFFIX
CERAMIC
CASE 632



P SUFFIX
PLASTIC
CASE 646



D SUFFIX
SOIC
CASE 751A

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	-0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	-0.5 to $V_{DD} + 0.5$	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	± 10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P and D/DW" Packages: -7.0 mW/°C From 65°C To 125°C
Ceramic "L" Packages: -12 mW/°C From 100°C To 125°C

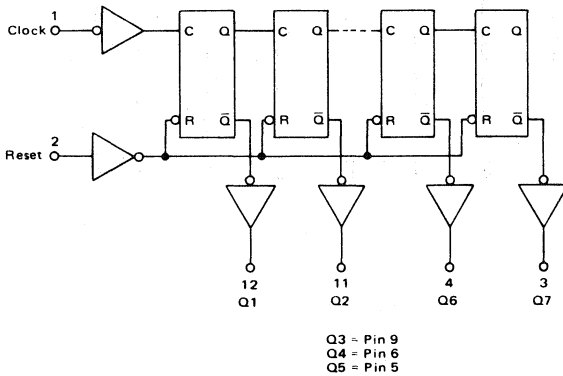
ORDERING INFORMATION

MC14XXXBCP Plastic
MC14XXXBCL Ceramic
MC14XXXBD SOIC

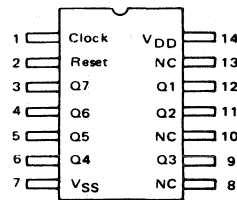
$T_A = -55^\circ$ to 125° C for all packages.

6

LOGIC DIAGRAM



PIN ASSIGNMENT



V_{DD} = Pin 14
 V_{SS} = Pin 7
NC = No Connection

MC14024B

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V _{DD} Vdc	-55°C		25°C			125°C		Unit	
			Min	Max	Min	Typ #	Max	Min	Max		
Output Voltage V _{in} = V _{DD} or 0	V _{OL}	5.0 10 15	—	0.05	—	0	0.05	—	0.05	Vdc	
			—	0.05	—	0	0.05	—	0.05		
—			0.05	—	0	0.05	—	0.05			
V _{in} = 0 or V _{DD}	V _{OH}	5.0 10 15	4.95	—	4.95	5.0	—	4.95	—	Vdc	
			9.95	—	9.95	10	—	9.95	—		
			14.95	—	14.95	15	—	14.95	—		
Input Voltage (V _O = 4.5 or 0.5 Vdc) (V _O = 9.0 or 1.0 Vdc) (V _O = 13.5 or 1.5 Vdc)	V _{IL}	5.0 10 15	—	1.5	—	2.25	1.5	—	1.5	Vdc	
			—	3.0	—	4.50	3.0	—	3.0		
—			4.0	—	6.75	4.0	—	4.0			
(V _O = 0.5 or 4.5 Vdc) (V _O = 1.0 or 9.0 Vdc) (V _O = 1.5 or 13.5 Vdc)	V _{IH}	5.0 10 15	3.5	—	3.5	2.75	—	3.5	—	Vdc	
			7.0	—	7.0	5.50	—	7.0	—		
11			—	11	8.25	—	11	—			
Output Drive Current (V _{OH} = 2.5 Vdc) (V _{OH} = 4.6 Vdc) (V _{OH} = 9.5 Vdc) (V _{OH} = 13.5 Vdc)	Source	I _{OH}	5.0	-3.0	—	-2.4	-4.2	—	-1.7	—	mA _{dc}
			5.0	-0.64	—	-0.51	-0.88	—	-0.36	—	
10			-1.6	—	-1.3	-2.25	—	-0.9	—		
(V _{OL} = 0.4 Vdc) (V _{OL} = 0.5 Vdc) (V _{OL} = 1.5 Vdc)	Sink	I _{OL}	5.0	0.64	—	0.51	0.88	—	0.36	—	mA _{dc}
			10	1.6	—	1.3	2.25	—	0.9	—	
15			4.2	—	3.4	8.8	—	2.4	—		
Input Current	I _{in}	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	μA _{dc}	
Input Capacitance (V _{in} = 0)	C _{in}	—	—	—	—	5.0	7.5	—	—	pF	
Quiescent Current (Per Package)	I _{DD}	5.0	—	5.0	—	0.005	5.0	—	150	μA _{dc}	
		10	—	10	—	0.010	10	—	300		
		15	—	20	—	0.015	20	—	600		
Total Supply Current***† (Dynamic plus Quiescent, Per Package) (C _L = 50 pF on all outputs, all buffers switching)	I _T	5.0	I _T = (0.31 μA/kHz) f + I _{DD}					μA _{dc}			
		10	I _T = (0.60 μA/kHz) f + I _{DD}								
		15	I _T = (1.89 μA/kHz) f + I _{DD}								

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) Vfk$$

where: I_T is in μA (per package), C_L in pF, V = (V_{DD} - V_{SS}) in volts, f in kHz is input frequency, and k = 0.001.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range V_{SS} ≤ (V_{in} or V_{out}) ≤ V_{DD}. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

MC14024B

SWITCHING CHARACTERISTICS* ($C_L = 50 \text{ pF}$, $T_A = 25^\circ\text{C}$)

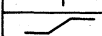
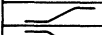
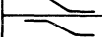
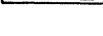
Characteristic	Symbol	V _{DD}	Min	Typ #	Max	Unit
Output Rise and Fall Time $t_{TLH}, t_{THL} = (1.5 \text{ ns/pF}) C_L + 25 \text{ ns}$ $t_{TLH}, t_{THL} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$ $t_{TLH}, t_{THL} = (0.55 \text{ ns/pF}) C_L + 9.5 \text{ ns}$	t_{TLH}, t_{THL}	5.0 10 15	— — —	100 50 40	200 100 80	ns
Propagation Delay Time Clock to Q1 $t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 295 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 117 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 85 \text{ ns}$ Clock to Q7 $t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 915 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 367 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 275 \text{ ns}$ Reset to Q _n $t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 415 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 217 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 155 \text{ ns}$	t_{PLH}, t_{PHL}	5.0 10 15 5.0 10 15 5.0 10 15	— — — — — — — — —	380 150 110 1000 400 300 500 250 180	600 230 175 2000 750 565 800 400 300	ns
Clock Pulse Width	t_{WH}	5.0 10 15	500 165 125	200 60 40	— — —	ns
Reset Pulse Width	t_{WH}	5.0 10 15	600 350 260	375 200 150	— — —	ns
Reset Removal Time	t_{rem}	5.0 10 15	625 190 145	250 75 50	— — —	ns
Clock Input Rise and Fall Times	t_{TLH}, t_{THL}	5.0 10 15	— — —	— — —	1.0 8.0 200	s ms μs
Input Pulse Frequency	f_{cl}	5.0 10 15	— — —	2.5 8.0 12	1.0 3.0 4.0	MHz

*The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

6

TRUTH TABLE

CLOCK	RESET	STATE
0	0	No Change
0	1	All Outputs Low
1	0	No Change
1	1	All Outputs Low
	0	No Change
	1	All Outputs Low
	0	Advance One Count
	1	All Outputs Low

MC14024B

FIGURE 1 – TYPICAL OUTPUT SOURCE CHARACTERISTICS TEST CIRCUIT

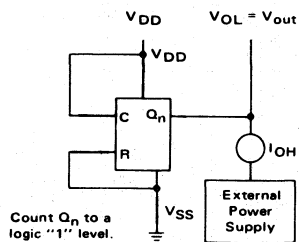


FIGURE 2 – TYPICAL OUTPUT SINK CHARACTERISTICS TEST CIRCUIT

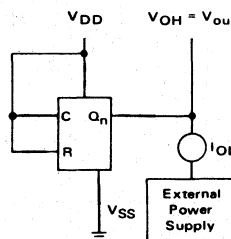


FIGURE 3 – POWER DISSIPATION TEST CIRCUIT

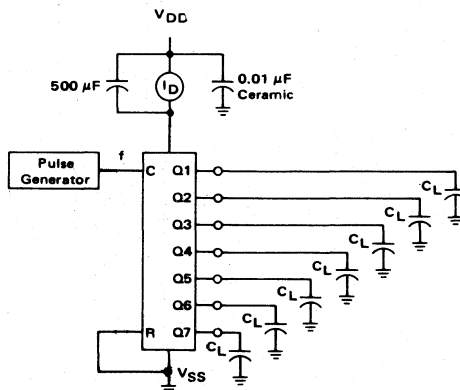
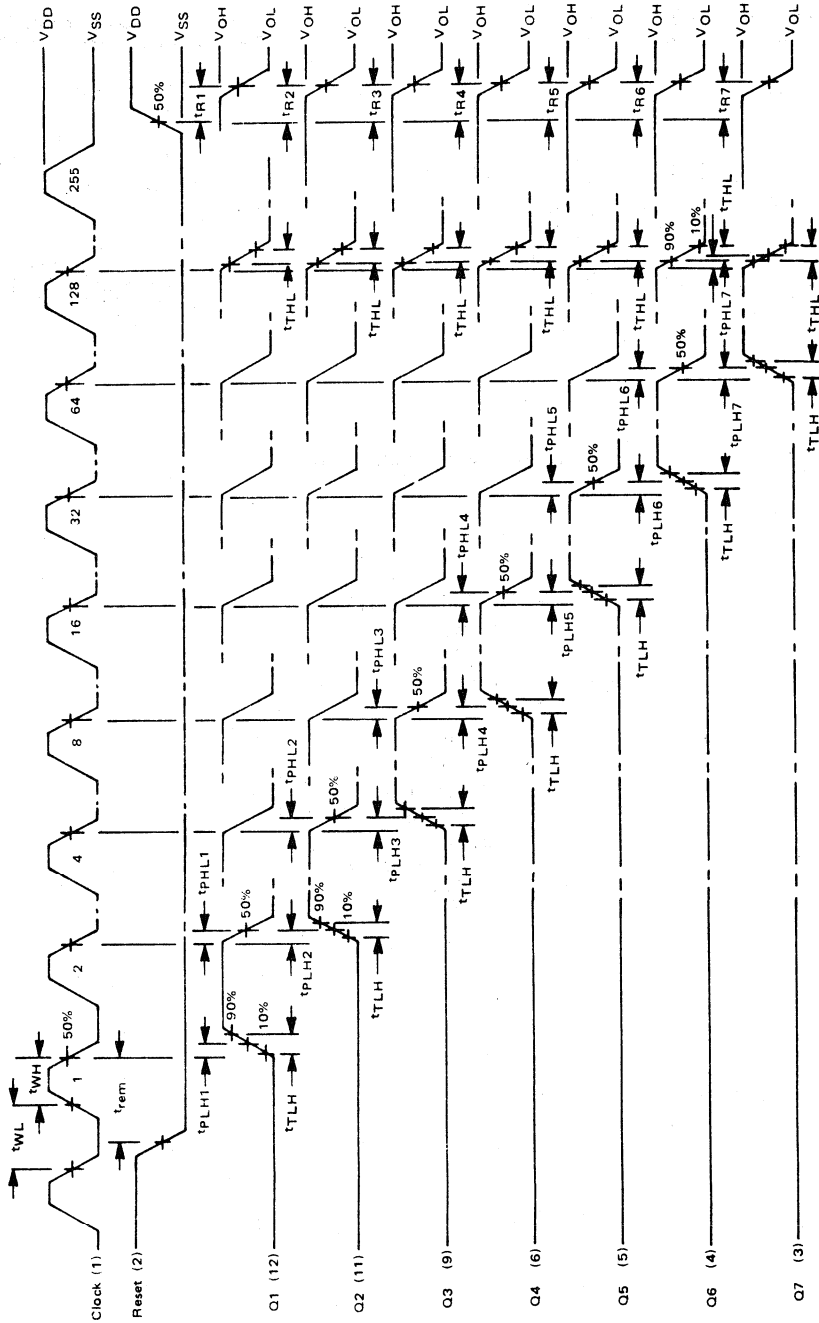


FIGURE 4 - FUNCTIONAL WAVEFORMS





MOTOROLA

DUAL J-K FLIP-FLOP

The MC14027B dual J-K flip-flop has independent J, K, Clock (C), Set (S) and Reset (R) inputs for each flip-flop. These devices may be used in control, register, or toggle functions.

- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Logic Swing Independent of Fanout
- Logic Edge-Clocked Flip-Flop Design –
Logic state is retained indefinitely with clock level either high or low; information is transferred to the output only on the positive-going edge of the clock pulse
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range
- Pin-for-Pin Replacement for CD4027B

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	-0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	-0.5 to $V_{DD} + 0.5$	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	± 10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P and D/DW" Packages: -7.0 mW/°C From 65°C To 125°C
Ceramic "L" Packages: -12 mW/°C From 100°C To 125°C

TRUTH TABLE

C†	INPUTS					OUTPUTS*		
	J	K	S	R	Q_n ‡	Q_{n+1}	\bar{Q}_{n+1}	
1	X	0	0	0	0	1	0	
X	0	0	0	0	1	1	0	
0	X	0	0	0	0	0	1	
X	1	0	0	0	1	0	1	
1	1	0	0	0	Q_0	\bar{Q}_0	Q_0	
X	X	0	0	X	Q_n	\bar{Q}_n	No Change	
X	X	X	1	0	X	1	0	
X	X	X	0	1	X	0	1	
X	X	X	1	1	X	1	1	

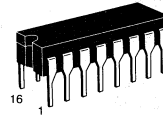
X = Don't Care † = Present State
‡ = Level Change * = Next State

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

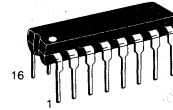
MC14025B
See Page 6-5

MC14025UB
See Page 6-14

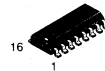
MC14027B



L SUFFIX
CERAMIC
CASE 620



P SUFFIX
PLASTIC
CASE 648



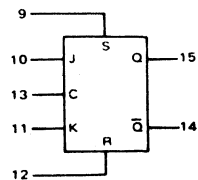
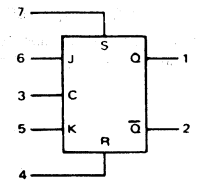
D SUFFIX
SOIC
CASE 751B

ORDERING INFORMATION

- MC14XXXBCP Plastic
- MC14XXXBCL Ceramic
- MC14XXXBD SOIC

$T_A = -55^\circ\text{C}$ to 125°C for all packages.

BLOCK DIAGRAM



$V_{DD} = \text{Pin 16}$
 $V_{SS} = \text{Pin 8}$

MC14027B

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V _{DD} Vdc	-55°C		25°C			125°C		Unit
			Min	Max	Min	Typ #	Max	Min	Max	
Output Voltage V _{in} = V _{DD} or 0	V _{OL}	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
		10	—	0.05	—	0	0.05	—	0.05	
V _{in} = 0 or V _{DD}	V _{OH}	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc
		10	9.95	—	9.95	10	—	9.95	—	
Input Voltage (V _O = 4.5 or 0.5 Vdc) (V _O = 9.0 or 1.0 Vdc) (V _O = 13.5 or 1.5 Vdc)	V _{IL}	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc
		10	—	3.0	—	4.50	3.0	—	3.0	
(V _O = 0.5 or 4.5 Vdc) (V _O = 1.0 or 9.0 Vdc) (V _O = 1.5 or 13.5 Vdc)	V _{IH}	5.0	3.5	—	3.5	2.75	—	3.5	—	Vdc
		10	7.0	—	7.0	5.50	—	7.0	—	
Output Drive Current (V _{OH} = 2.5 Vdc) (V _{OH} = 4.6 Vdc) (V _{OH} = 9.5 Vdc) (V _{OH} = 13.5 Vdc)	I _{OH}	5.0	-3.0	—	-2.4	-4.2	—	-1.7	—	mAdc
		10	-0.64	—	-0.51	-0.88	—	-0.36	—	
(V _{OL} = 0.4 Vdc) (V _{OL} = 0.5 Vdc) (V _{OL} = 1.5 Vdc)	I _{OL}	5.0	0.64	—	0.51	0.88	—	0.36	—	mAdc
		10	1.6	—	1.3	2.25	—	0.9	—	
		15	4.2	—	3.4	8.8	—	2.4	—	
Input Current	I _{in}	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	μAdc
Input Capacitance (V _{in} = 0)	C _{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)	I _{DD}	5.0	—	1.0	—	0.002	1.0	—	30	μAdc
		10	—	2.0	—	0.004	2.0	—	60	
		15	—	4.0	—	0.006	4.0	—	120	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C _L = 50 pF on all outputs, all buffers switching)	I _T	5.0	I _T = (0.8 μA/kHz) f + I _{DD}							μAdc
		10	I _T = (1.6 μA/kHz) f + I _{DD}							
		15	I _T = (2.4 μA/kHz) f + I _{DD}							

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

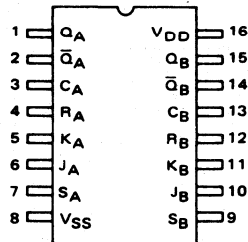
**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) Vfk$$

where: I_T is in μA (per package), C_L in pF, V = (V_{DD} - V_{SS}) in volts, f in kHz is input frequency, and k = 0.002.

PIN ASSIGNMENT



MC14027B

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

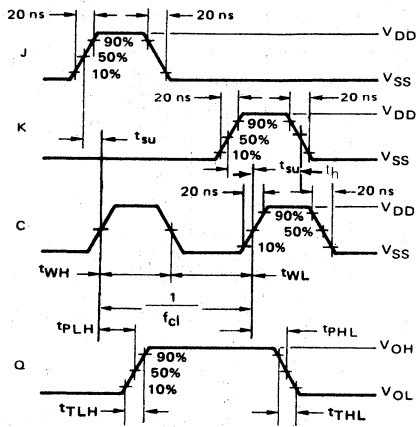
Characteristic	Symbol	V _{DD}	Min	f _{yp} #	Max	Unit
Output Rise and Fall Time t _{TLH} , t _{THL} = (1.5 ns/pF) C _L + 25 ns t _{TLH} , t _{THL} = (0.75 ns/pF) C _L + 12.5 ns t _{TLH} , t _{THL} = (0.55 ns/pF) C _L + 12.5 ns	t _{TLH} , t _{THL}	5.0 10 15	— — —	100 50 40	200 100 80	ns
Propagation Delay Times** Clock to Q, Q t _{PLH} , t _{PHL} = (1.7 ns/pF) C _L + 90 ns t _{PLH} , t _{PHL} = (0.66 ns/pF) C _L + 42 ns t _{PLH} , t _{PHL} = (0.5 ns/pF) C _L + 25 ns Set to Q, Q t _{PLH} , t _{PHL} = (1.7 ns/pF) C _L + 90 ns t _{PLH} , t _{PHL} = (0.66 ns/pF) C _L + 42 ns t _{PLH} , t _{PHL} = (0.5 ns/pF) C _L + 25 ns Reset to Q, Q t _{PLH} , t _{PHL} = (1.7 ns/pF) C _L + 265 ns t _{PLH} , t _{PHL} = (0.66 ns/pF) C _L + 67 ns t _{PLH} , t _{PHL} = (0.5 ns/pF) C _L + 50 ns	t _{PLH} , t _{PHL}	5.0 10 15 5.0 10 15 5.0 10 15	— — — — — — — — —	175 75 50 175 75 50 350 100 75	350 150 100 350 150 100 450 200 150	ns
Setup Times	t _{su}	5.0 10 15	140 50 35	70 25 17	— — —	ns
Hold Times	t _h	5.0 10 15	140 50 35	70 25 17	— — —	ns
Clock Pulse Width	t _{WH} , t _{WL}	5.0 10 15	330 110 75	165 55 38	— — —	ns
Clock Pulse Frequency	f _{cl}	5.0 10 15	— — —	3.0 9.0 13	1.5 4.5 6.5	MHz
Clock Pulse Rise and Fall Time	t _{TLH} , t _{THL}	5.0 10 15	— — —	— — —	15 5.0 4.0	μs
Removal Times Set Reset	t _{rem}	5 10 15 5 10 15	90 45 35 50 25 20	10 5 3 -30 -15 -10	— — — — — —	ns
Set and Reset Pulse Width	t _{WH}	5.0 10 15	250 100 70	125 50 35	— — —	ns

*The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

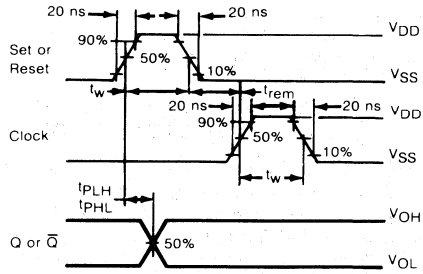
MC14027B

FIGURE 1 — DYNAMIC SIGNAL WAVEFORMS
(J, K, Clock, and Output)

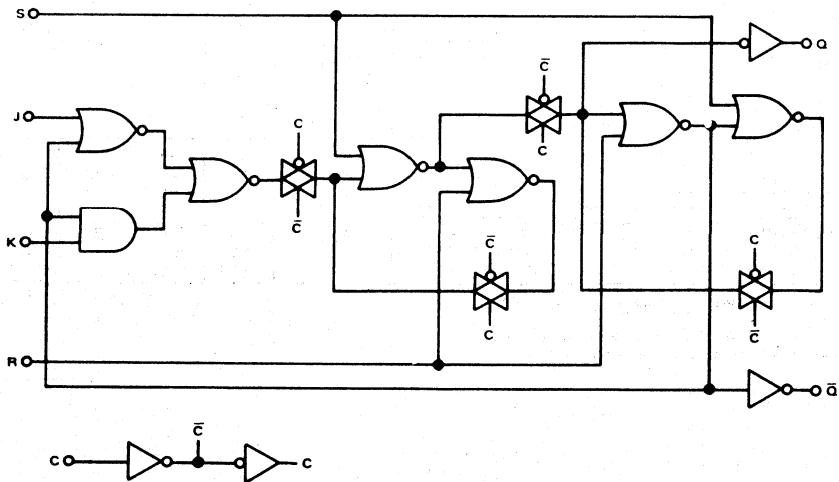


Inputs R and S low.
For the measurement of t_{WH} , $1/f_{cl}$, and P_D
the Inputs J and K are kept high.

FIGURE 2 — DYNAMIC SIGNAL WAVEFORMS
(Set, Reset, Clock, and Output)



LOGIC DIAGRAM
(1/2 of Device Shown)



6



MOTOROLA

MC14028B

**BCD-TO-DECIMAL DECODER
BINARY-TO-OCTAL DECODER**

The MC14028B decoder is constructed so that an 8421 BCD code on the four inputs provides a decimal (one-of-ten) decoded output, while a 3-bit binary input provides a decoded octal (one-of-eight) code output with D forced to a logic "0". Expanded decoding such as binary-to-hexadecimal (one-of-16), etc., can be achieved by using other MC14028B devices. The part is useful for code conversion, address decoding, memory selection control, demultiplexing, or read-out decoding.

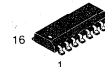
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range
- Positive Logic Design
- Low Outputs on All Illegal Input Combinations
- Similar to CD4028B.



L SUFFIX
CERAMIC
CASE 620



P SUFFIX
PLASTIC
CASE 648



D SUFFIX
SOIC
CASE 751B

ORDERING INFORMATION

- MC14XXXBCP Plastic
- MC14XXXBCL Ceramic
- MC14XXXBD SOIC

T_A = -55° to 125°C for all packages.

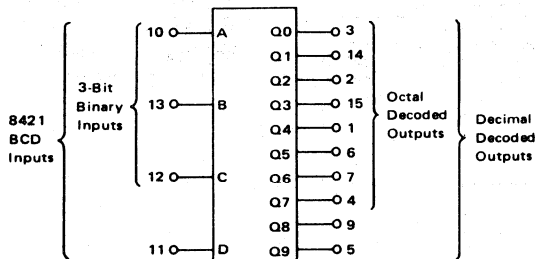
MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V _{DD}	DC Supply Voltage	-0.5 to +18.0	V
V _{in} , V _{out}	Input or Output Voltage (DC or Transient)	-0.5 to V _{DD} + 0.5	V
I _{in} , I _{out}	Input or Output Current (DC or Transient), per Pin	± 10	mA
P _D	Power Dissipation, per Package†	500	mW
T _{stg}	Storage Temperature	-65 to +150	°C
T _L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.

†Temperature Derating: Plastic "P and D/DW" Packages: -7.0 mW/°C From 65°C To 125°C
Ceramic "L" Packages: -12 mW/°C From 100°C To 125°C

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

TRUTH TABLE

INPUT				OUTPUT									
D	C	B	A	Q9	Q8	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0
0	0	0	0	0	0	0	0	0	0	0	0	0	1
0	0	0	1	0	0	0	0	0	0	0	0	1	0
0	0	1	0	0	0	0	0	0	0	0	1	0	0
0	0	1	1	0	0	0	0	0	0	1	0	0	0
0	1	0	0	0	0	0	0	0	1	0	0	0	0
0	1	0	1	0	0	0	0	0	1	0	0	0	0
0	1	1	0	0	0	0	1	0	0	0	0	0	0
0	1	1	1	0	0	1	0	0	0	0	0	0	0
1	0	0	0	0	1	0	0	0	0	0	0	0	0
1	0	0	1	1	0	0	0	0	0	0	0	0	0
1	0	1	0	0	0	0	0	0	0	0	0	0	0
1	0	1	1	0	0	0	0	0	0	0	0	0	0
1	1	0	0	0	0	0	0	0	0	0	0	0	0
1	1	0	1	0	0	0	0	0	0	0	0	0	0
1	1	1	0	0	0	0	0	0	0	0	0	0	0
1	1	1	1	0	0	0	0	0	0	0	0	0	0

6

MC14028B

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V _{DD} Vdc	-55°C		25°C			125°C		Unit
			Min	Max	Min	Typ #	Max	Min	Max	
Output Voltage V _{in} = V _{DD} or 0	V _{OL}	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
		10	—	0.05	—	0	0.05	—	0.05	
		15	—	0.05	—	0	0.05	—	0.05	
V _{in} = 0 or V _{DD}	V _{OH}	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc
		10	9.95	—	9.95	10	—	9.95	—	
		15	14.95	—	14.95	15	—	14.95	—	
Input Voltage (V _O = 4.5 or 0.5 Vdc) (V _O = 9.0 or 1.0 Vdc) (V _O = 13.5 or 1.5 Vdc)	V _{IL}	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc
		10	—	3.0	—	4.50	3.0	—	3.0	
		15	—	4.0	—	6.75	4.0	—	4.0	
	V _{IH}	5.0	3.5	—	3.5	2.75	—	3.5	—	Vdc
		10	7.0	—	7.0	5.50	—	7.0	—	
		15	11	—	11	8.25	—	11	—	
Output Drive Current (V _{OH} = 2.5 Vdc) (V _{OH} = 4.6 Vdc) (V _{OH} = 9.5 Vdc) (V _{OH} = 13.5 Vdc)	Source I _{OH}	5.0	-3.0	—	-2.4	-4.2	—	-1.7	—	mA _{dc}
		5.0	-0.64	—	-0.51	-0.88	—	-0.36	—	
		10	-1.6	—	-1.3	-2.25	—	-0.9	—	
	Sink I _{OL}	5.0	0.64	—	0.51	0.88	—	0.36	—	mA _{dc}
		10	1.6	—	1.3	2.25	—	0.9	—	
		15	4.2	—	3.4	8.8	—	2.4	—	
Input Current	I _{in}	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	μA _{dc}
Input Capacitance (V _{in} = 0)	C _{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)	I _{DD}	5.0	—	5.0	—	0.005	5.0	—	150	μA _{dc}
		10	—	10	—	0.010	10	—	300	
		15	—	20	—	0.015	20	—	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C _L = 50 pF on all outputs, all buffers switching)	I _T	5.0	I _T = (0.3 μA/kHz) f + I _{DD}						μA _{dc}	
		10	I _T = (0.6 μA/kHz) f + I _{DD}							
		15	I _T = (0.9 μA/kHz) f + I _{DD}							

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

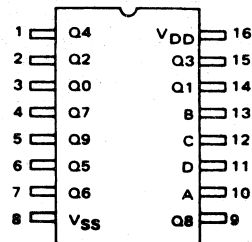
**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) V/k$$

where: I_T is in μA (per package), C_L in pF, V = (V_{DD} - V_{SS}) in volts, f in kHz is input frequency, and k = 0.001.

PIN ASSIGNMENT



This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range V_{SS} ≤ (V_{in} or V_{out}) ≤ V_{DD}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

MC14028B

SWITCHING CHARACTERISTICS* ($C_L = 50 \text{ pF}$, $T_A = 25^\circ\text{C}$)

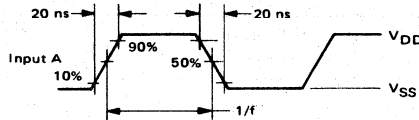
Characteristic	Symbol	V _{DD}	Min	Typ #	Max	Unit
Output Rise and Fall Time	t_{TLH} , t_{THL}	5.0 10 15	— — —	100 50 40	200 100 80	ns
t_{TLH} , $t_{THL} = (1.5 \text{ ns/pF}) C_L + 25 \text{ ns}$						
t_{TLH} , $t_{THL} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$						
t_{TLH} , $t_{THL} = (0.55 \text{ ns/pF}) C_L + 9.5 \text{ ns}$						
Propagation Delay Time	t_{PLH} , t_{PHL}	5.0 10 15	— — —	300 130 90	600 260 180	ns
t_{PLH} , $t_{PHL} = (1.7 \text{ ns/pF}) C_L + 215 \text{ ns}$						
t_{PLH} , $t_{PHL} = (0.66 \text{ ns/pF}) C_L + 97 \text{ ns}$						
t_{PLH} , $t_{PHL} = (0.5 \text{ ns/pF}) C_L + 65 \text{ ns}$						

*The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

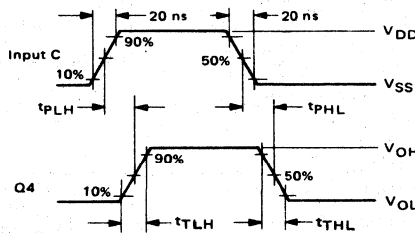
FIGURE 1 – DYNAMIC SIGNAL WAVEFORMS

Inputs B, C, and D switching in respect to a BCD code.



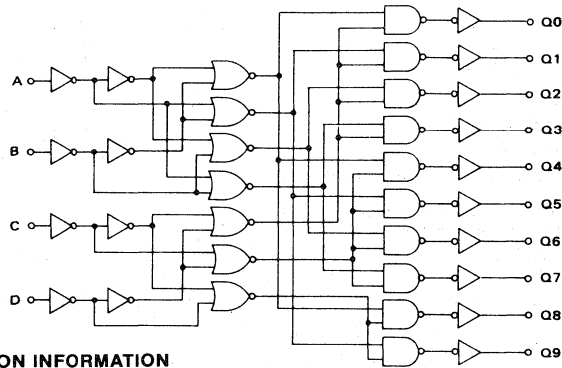
All outputs connected to respective C_L loads. f in respect to a system clock.

Inputs A, B, and D low.



MC14028B

LOGIC DIAGRAM

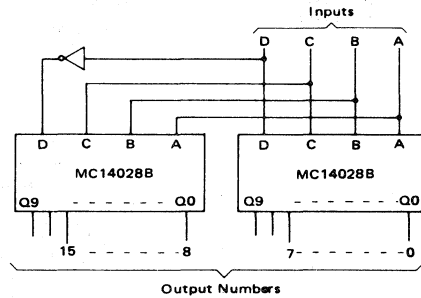


APPLICATION INFORMATION

Expanded decoding can be performed by using the MC14028B and other CMOS Integrated Circuits. The circuit in Figure 2 converts any 4-bit code to a decimal or hexadecimal code. The accompanying table shows the input binary combinations, the associated "output numbers" that go "high" when selected, and the "redefined output numbers" needed for the proper code. For example: For the combination DCBA = 0111 the output number 7 is redefined for the 4-bit binary, 4-bit gray, excess-3, or excess-3 gray codes as 7, 5, 4, or 2, respectively. Figure 3 shows a 6-bit binary 1-of-64 decoder using nine MC14028B circuits and two MC14069UB inverters.

The MC14028B can be used in decimal digit displays, such as, neon readouts or incandescent projection indicators as shown in Figure 4.

FIGURE 2 - CODE CONVERSION CIRCUIT AND TRUTH TABLE



INPUTS																CODE AND REDEFINED OUTPUT NUMBERS									
																Hexadecimal			Decimal						
D	C	B	A	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	4-Bit Binary	4-Bit Gray	Excess-3	Excess-3 Gray	Aiken	4221
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	
0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	0	0	1	
0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	2	3	0	2	2	
0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	3	2	3	3	2	
0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	4	7	1	4	4	
0	1	0	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	5	6	2	4	3	
0	1	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	6	4	3	1	3	
0	1	1	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	7	5	4	2	4	
1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	8	15	5		5	
1	0	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	9	14	6		5	
1	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	10	12	7	9	6	
1	0	1	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	11	13	8		5	
1	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	12	8	9	5	6	
1	1	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	13	9		6	7	
1	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	14	11		8	8	
1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	15	10		7	9	

MC14028B

FIGURE 3 – SIX-BIT BINARY 1-OF-64 DECODER

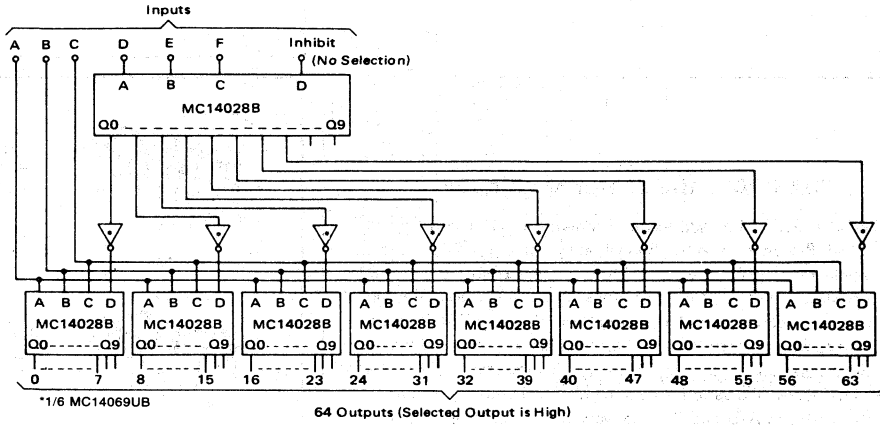
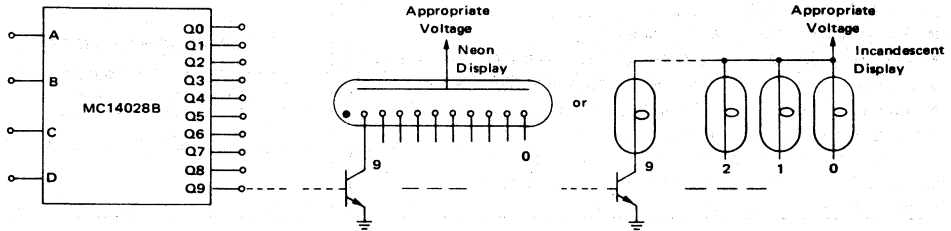


FIGURE 4 – DECIMAL DIGIT DISPLAY APPLICATION





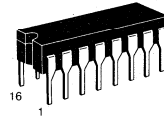
MOTOROLA

MC14029B

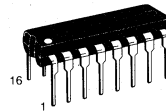
BINARY/DECADE UP/DOWN COUNTER

The MC14029B Binary/Decade up/down counter is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. The counter consists of type D flip-flop stages with a gating structure to provide toggle flip-flop capability. The counter can be used in either Binary or BCD operation. This complementary MOS counter finds primary use in up/down and difference counting and frequency synthesizer applications where low power dissipation and/or high noise immunity is desired. It is also useful in A/D and D/A conversion and for magnitude and sign generation.

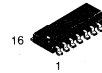
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Internally Synchronous for High Speed
- Logic Edge-Clocked Design – Count Occurs on Positive Going Edge of Clock
- Asynchronous Preset Enable Operation
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range
- Pin for Pin Replacement for CD4029B



**L SUFFIX
CERAMIC
CASE 620**



**P SUFFIX
PLASTIC
CASE 648**



**D SUFFIX
SOIC
CASE 751B**

ORDERING INFORMATION

MC14XXXBCP Plastic
MC14XXXBCL Ceramic
MC14XXXBD SOIC

T_A = -55° to 125°C for all packages.

6

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V _{DD}	DC Supply Voltage	-0.5 to +18.0	V
V _{in} , V _{out}	Input or Output Voltage (DC or Transient)	-0.5 to V _{DD} + 0.5	V
I _{in} , I _{out}	Input or Output Current (DC or Transient), per Pin	± 10	mA
P _D	Power Dissipation, per Package†	500	mW
T _{stg}	Storage Temperature	-65 to +150	°C
T _L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.

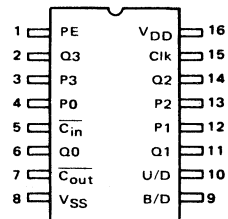
†Temperature Derating: Plastic "P and D/DW" Packages: -7.0 mW/°C From 65°C To 125°C
Ceramic "L" Packages: -12 mW/°C From 100°C To 125°C

TRUTH TABLE

Carry In	Up/Down	Preset Enable	Action
1	X	0	No Count
0	1	0	Count Up
0	0	0	Count Down
X	X	1	Preset

X = Don't Care

PIN ASSIGNMENT



MC14029B

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V _{DD} Vdc	-55°C		25°C			125°C		Unit	
			Min	Max	Min	Typ #	Max	Min	Max		
Output Voltage V _{in} = V _{DD} or 0	VOL	5.0	—	0.05	—	0	0.05	—	0.05	Vdc	
		10	—	0.05	—	0	0.05	—	0.05		
15		—	0.05	—	0	0.05	—	0.05			
V _{in} = 0 or V _{DD}	VOH	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc	
		10	9.95	—	9.95	10	—	9.95	—		
		15	14.95	—	14.95	15	—	14.95	—		
Input Voltage (V _O = 4.5 or 0.5 Vdc) (V _O = 9.0 or 1.0 Vdc) (V _O = 13.5 or 1.5 Vdc)	VIL	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc	
		10	—	3.0	—	4.50	3.0	—	3.0		
15		—	4.0	—	6.75	4.0	—	4.0			
(V _O = 0.5 or 4.5 Vdc) (V _O = 1.0 or 9.0 Vdc) (V _O = 1.5 or 13.5 Vdc)	VIH	5.0	3.5	—	3.5	2.75	—	3.5	—	Vdc	
		10	7.0	—	7.0	5.50	—	7.0	—		
		15	11	—	11	8.25	—	11	—		
Output Drive Current (V _{OH} = 2.5 Vdc) (V _{OH} = 4.6 Vdc) (V _{OH} = 9.5 Vdc) (V _{OH} = 13.5 Vdc)	Source	IOH	5.0	-3.0	—	-2.4	-4.2	—	-1.7	—	mAdc
			10	-0.64	—	-0.51	-0.88	—	-0.36	—	
			10	-1.6	—	-1.3	-2.25	—	-0.9	—	
			15	-4.2	—	-3.4	-8.8	—	-2.4	—	
	Sink	IOL	5.0	0.64	—	0.51	0.88	—	0.36	—	mAdc
			10	1.6	—	1.3	2.25	—	0.9	—	
15	4.2	—	3.4	8.8	—	2.4	—	—			
Input Current	I _{in}	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	μAdc	
Input Capacitance (V _{in} = 0)	C _{in}	—	—	—	—	5.0	7.5	—	—	pF	
Quiescent Current (Per Package)	I _{DD}	5.0	—	5.0	—	0.005	5.0	—	150	μAdc	
		10	—	10	—	0.010	10	—	300		
		15	—	20	—	0.015	20	—	600		
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C _L = 50 pF on all outputs, all buffers switching)	I _T	5.0	I _T = (0.58 μA/kHz) f + I _{DD} I _T = (1.20 μA/kHz) f + I _{DD} I _T = (1.70 μA/kHz) f + I _{DD}							μAdc	
10											
15											

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) V/k$$

where: I_T is in μA (per package), C_L in pF, V = (V_{DD} - V_{SS}) in volts, f in kHz is input frequency, and k = 0.001.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range V_{SS} ≤ (V_{in} or V_{out}) ≤ V_{DD}. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

MC14029B

SWITCHING CHARACTERISTICS * ($C_L = 50 \text{ pF}$, $T_A = 25^\circ\text{C}$)

Characteristic	Symbol	V_{DD}	All Types			Unit
			Min	Typ #	Max	
Output Rise and Fall Time $t_{TLH}, t_{THL} = (1.5 \text{ ns/pF}) C_L + 25 \text{ ns}$ $t_{TLH}, t_{THL} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$ $t_{TLH}, t_{THL} = (0.55 \text{ ns/pF}) C_L + 9.5 \text{ ns}$	t_{TLH} , t_{THL}	5.0 10 15	— — —	100 50 40	200 100 80	ns
Propagation Delay Time Clk to Q $t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 230 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 97 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 75 \text{ ns}$ Clk to $\overline{C_{out}}$ $t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 230 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 97 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 75 \text{ ns}$ C_{in} to $\overline{C_{out}}$ $t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 95 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 47 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 35 \text{ ns}$ PE to Q $t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 230 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 97 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 75 \text{ ns}$ PE to $\overline{C_{out}}$ $t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 465 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 192 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 125 \text{ ns}$	t_{PLH} , t_{PHL}	5.0 10 15	— — —	200 100 90	400 200 180	ns
	t_{PLH} , t_{PHL}	5.0 10 15	— — —	250 130 85	500 260 190	ns
	t_{PLH} , t_{PHL}	5.0 10 15	— — —	175 50 50	360 120 100	ns
	t_{PLH} , t_{PHL}	5.0 10 15	— — —	235 100 80	470 200 160	ns
	t_{PLH} , t_{PHL}	5.0 10 15	— — —	320 145 105	640 290 210	ns
Clock Pulse Width	$t_W(\text{cl})$	5.0 10 15	180 80 60	90 40 30	— — —	ns
Clock Pulse Frequency	f_{cl}	5.0 10 15	— — —	4.0 8.0 10	2.0 4.0 5.0	MHz
Preset Removal Time The Preset Signal must be low prior to a positive-going transition of the clock.	t_{rem}	5.0 10 15	160 80 60	80 40 30	— — —	ns
Clock Rise and Fall Time	$t_r(\text{cl})$ $t_f(\text{cl})$	5.0 10 15	— — —	— — —	15 5 4	μs
Carry In Setup Time	t_{su}	5.0 10 15	150 60 40	75 30 20	— — —	ns
Up/Down Setup Time		5.0 10 15	340 140 100	170 70 50	— — —	ns
Binary/Decade Setup Time		5.0 10 15	320 140 100	160 70 50	— — —	ns
Preset Enable Pulse Width	t_W	5.0 10 15	130 70 50	65 35 25	— — —	ns

*The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

MC14029B

FIGURE 1 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

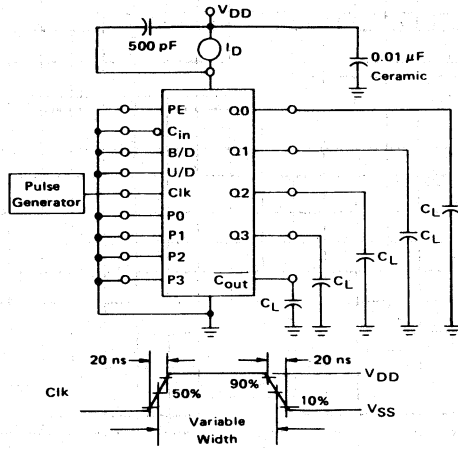
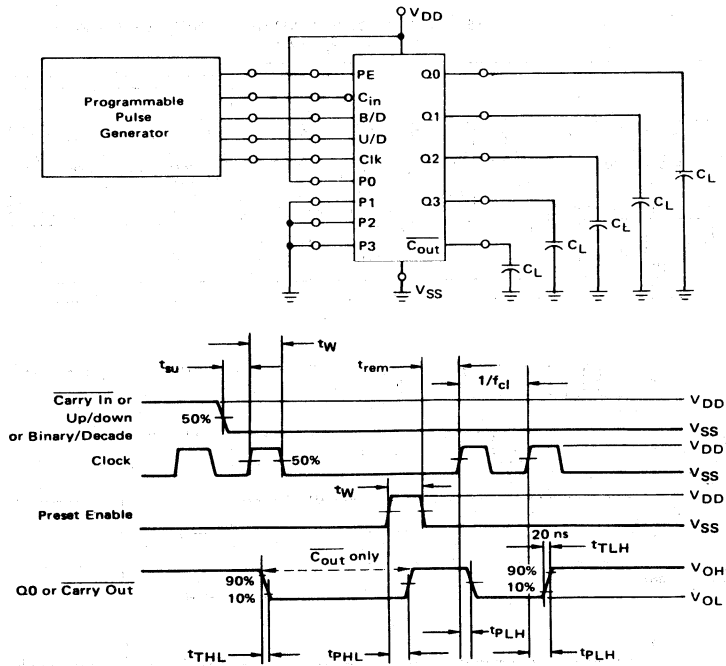


FIGURE 2 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



6

MC14029B

TIMING DIAGRAM

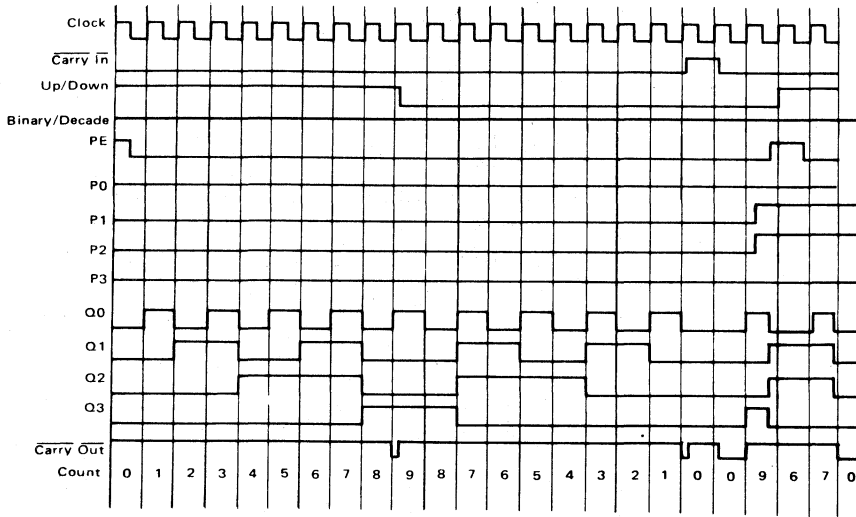
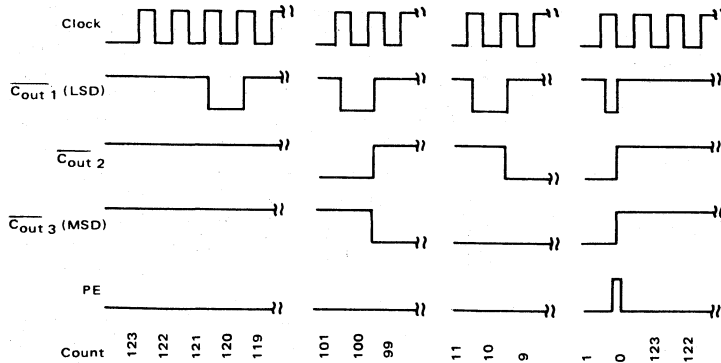
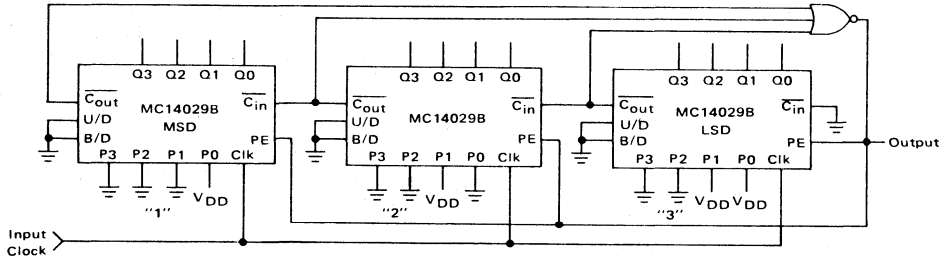


FIGURE 3 – DIVIDE BY N BCD DOWN COUNTER and TIMING DIAGRAM
(Shown for N = 123)

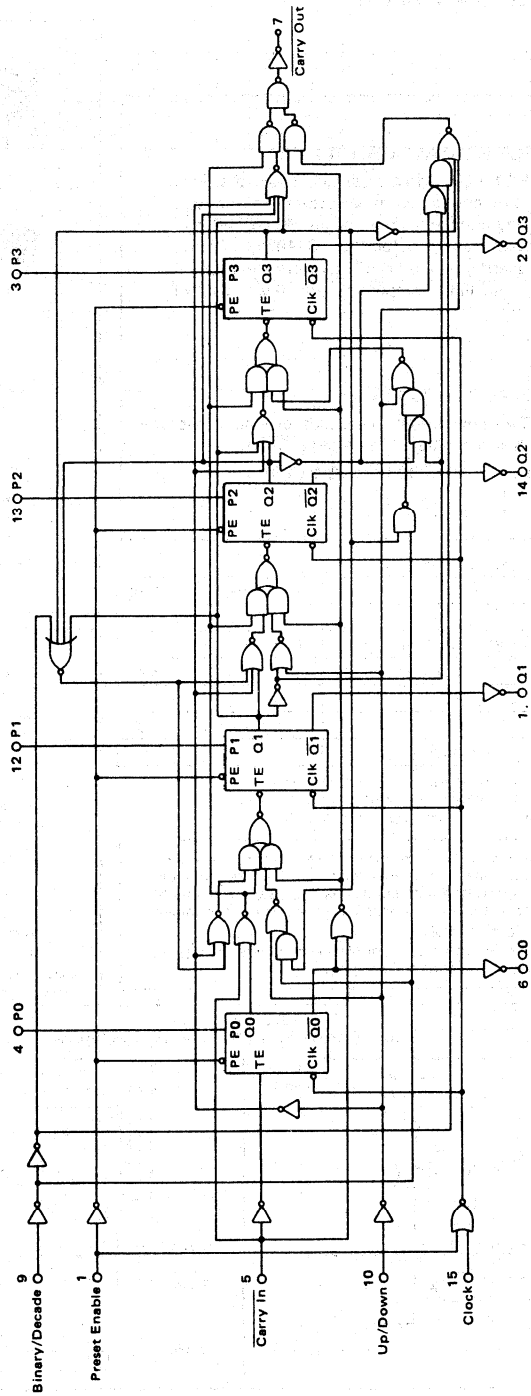


* $t_W \approx 900 \text{ ns}$ @ $V_{DD} = 5 \text{ V}$

6

MC14029B

LOGIC DIAGRAM





MOTOROLA

TRIPLE SERIAL ADDERS

The MC14032B and MC14038B triple serial adders have the clock and carry reset inputs common to all three adders. The carry is added on the positive-going clock transition for the MC14032B, and on the negative-going clock transition for the MC14038B. Typical applications include serial arithmetic units, digital correlators, digital servo control systems, datalink computers, and flight control computers.

- Buffered Outputs
- Single-Phase Clocking
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range.
- Pin-for-Pin Replacement for CD4032B and CD4038B.

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	-0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	-0.5 to $V_{DD} + 0.5$	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	± 10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

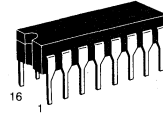
*Maximum Ratings are those values beyond which damage to the device may occur.

†Temperature Derating: Plastic "P and D/DW" Packages: -7.0 mW/°C From 65°C To 125°C
Ceramic "L" Packages: -12 mW/°C From 100°C To 125°C

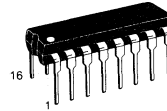
This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

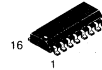
**MC14032B
MC14038B**



L SUFFIX
CERAMIC
CASE 620



P SUFFIX
PLASTIC
CASE 648



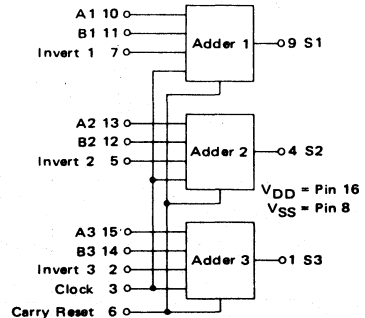
D SUFFIX
SOIC
CASE 751B

ORDERING INFORMATION

MC14XXXBCP Plastic
MC14XXXBCL Ceramic
MC14XXXBD SOIC

$T_A = -55^\circ \text{ to } 125^\circ \text{C}$ for all packages.

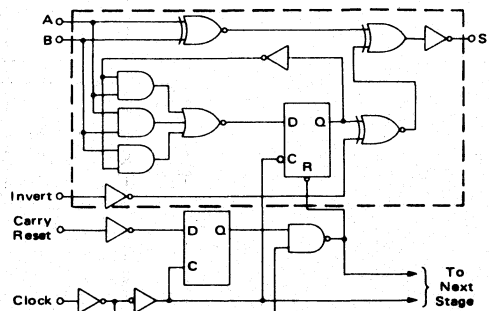
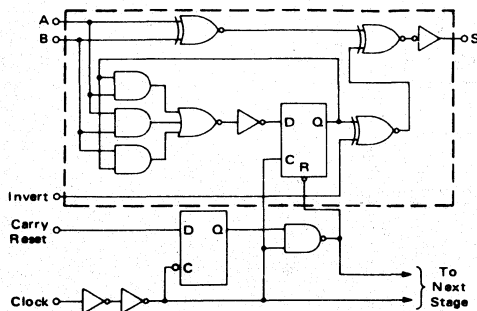
BLOCK DIAGRAM



MC14032B

**LOGIC DIAGRAMS
(ONE SECTION AND COMMON INPUTS SHOWN)**

MC14038B



MC14032B•MC14038B

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V _{DD} Vdc	-55°C		25°C			125°C		Unit	
			Min	Max	Min	Typ #	Max	Min	Max		
Output Voltage V _{in} = V _{DD} or 0	V _{OL}	5.0	—	0.05	—	0	0.05	—	0.05	Vdc	
		10	—	0.05	—	0	0.05	—	0.05		
		15	—	0.05	—	0	0.05	—	0.05		
	V _{in} = 0 or V _{DD}	V _{OH}	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc
			10	9.95	—	9.95	10	—	9.95	—	
			15	14.95	—	14.95	15	—	14.95	—	
Input Voltage (V _O = 4.5 or 0.5 Vdc) (V _O = 9.0 or 1.0 Vdc) (V _O = 13.5 or 1.5 Vdc)	V _{IL}	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc	
		10	—	3.0	—	4.50	3.0	—	3.0		
		15	—	4.0	—	6.75	4.0	—	4.0		
	V _{in} = 0 or V _{DD}	V _{IH}	5.0	3.5	—	3.5	2.75	—	3.5	—	Vdc
			10	7.0	—	7.0	5.50	—	7.0	—	
			15	11	—	11	8.25	—	11	—	
Output Drive Current (V _{OH} = 2.5 Vdc) (V _{OH} = 4.6 Vdc) (V _{OH} = 9.5 Vdc) (V _{OH} = 13.5 Vdc)	Source	I _{OH}	5.0	-3.0	—	-2.4	-4.2	—	-1.7	—	mAdc
			10	-0.64	—	-0.51	-0.88	—	-0.36	—	
			15	-1.6	—	-1.3	-2.25	—	-0.9	—	
	Sink	I _{OL}	5.0	0.64	—	0.51	0.88	—	0.36	—	mAdc
			10	1.6	—	1.3	2.25	—	0.9	—	
			15	4.2	—	3.4	8.8	—	2.4	—	
Input Current	I _{in}	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	μAdc	
Input Capacitance (V _{in} = 0)	C _{in}	—	—	—	—	5.0	7.5	—	—	pF	
Quiescent Current (Per Package)	I _{DD}	5.0	—	5.0	—	0.005	5.0	—	150	μAdc	
		10	—	10	—	0.010	10	—	300		
		15	—	20	—	0.015	20	—	600		
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C _L = 50 pF on all outputs, all buffers switching)	I _T	5.0	I _T = (0.96 μA/kHz) f + I _{DD}							μAdc	
		10	I _T = (1.93 μA/kHz) f + I _{DD}								
		15	I _T = (2.80 μA/kHz) f + I _{DD}								

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

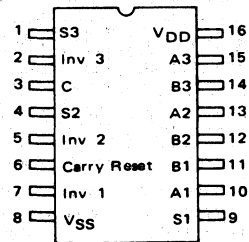
**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) \text{ Vfk}$$

where: I_T is in μA (per package), C_L in pF, V = (V_{DD} - V_{SS}) in volts, f in kHz is input frequency, and k = 0.003.

PIN ASSIGNMENT



MC14032B•MC14038B

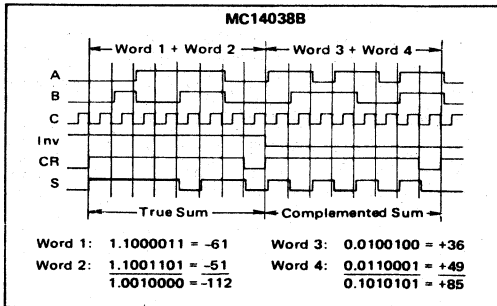
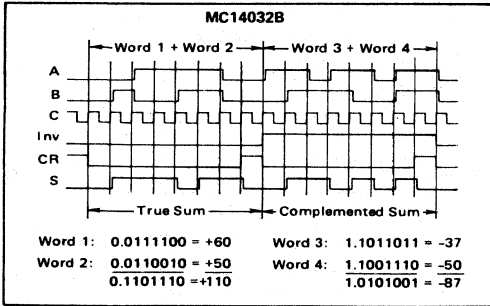
SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V _{DD} V _{dC}	Min	Typ #	Max	Unit
Output Rise and Fall Time t _{TLH} , t _{THL} = (1.5 ns/pF) C _L + 25 ns t _{TLH} , t _{THL} = (0.75 ns/pF) C _L + 12.5 ns t _{TLH} , t _{THL} = (0.55 ns/pF) C _L + 9.5 ns	t _{TLH} , t _{THL}	5.0 10 15	— — —	100 50 40	200 100 80	ns
Propagation Delay Time A, B or Invert to Sum t _{PLH} , t _{PHL} = (1.7 ns/pF) C _L + 195 ns t _{PLH} , t _{PHL} = (0.66 ns/pF) C _L + 87 ns t _{PLH} , t _{PHL} = (0.5 ns/pF) C _L + 65 ns Clock to Sum t _{PLH} , t _{PHL} = (1.7 ns/pF) C _L + 415 ns t _{PLH} , t _{PHL} = (0.66 ns/pF) C _L + 147 ns t _{PLH} , t _{PHL} = (0.5 ns/pF) C _L + 110 ns	t _{PLH} , t _{PHL}	5.0 10 15	— — —	280 120 90	1400 300 230	ns
Input Setup Time	t _{su}	5.0 10 15	10 10 10	-10 0 0	— — —	ns
Clock Pulse Frequency	f _{cl}	5.0 10 15	— — —	4.0 10 12	1.0 2.5 4.0	MHz
Clock Rise and Fall Times	t _{THL} , t _{TLH}	5.0 10 15	— — —	— — —	15 5 4	μs

*The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

TIMING DIAGRAMS



Note: Unused input pins must be connected to either V_{DD} or V_{SS}.

MC14032B•MC14038B

FIGURE 1 – TYPICAL OUTPUT SOURCE TEST CIRCUIT

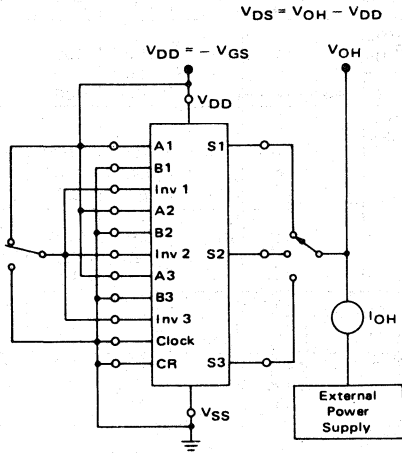


FIGURE 2 – TYPICAL OUTPUT SINK TEST CIRCUIT

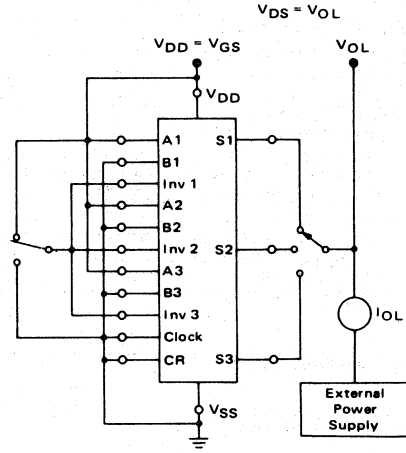
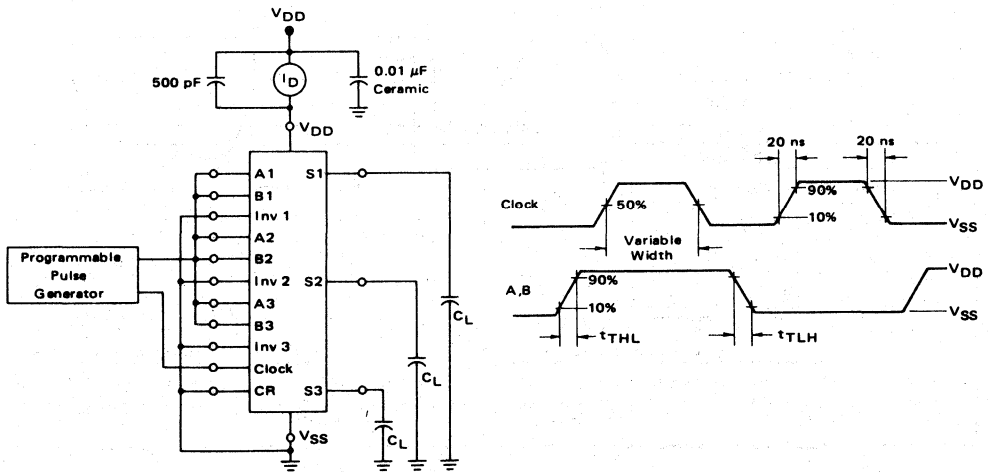
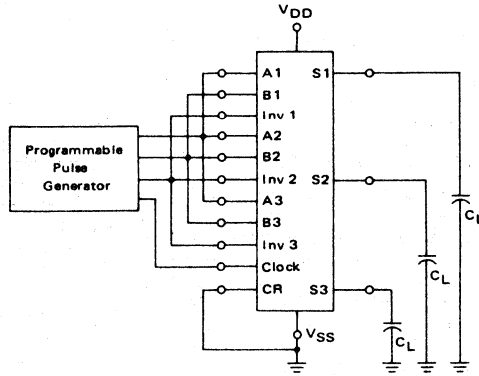


FIGURE 3 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORMS

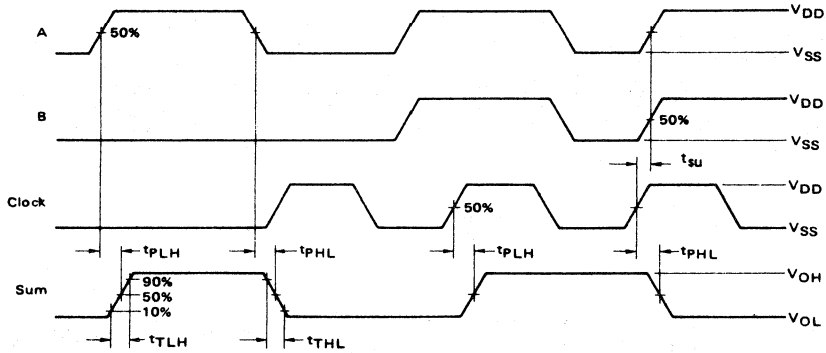


MC14032B•MC14038B

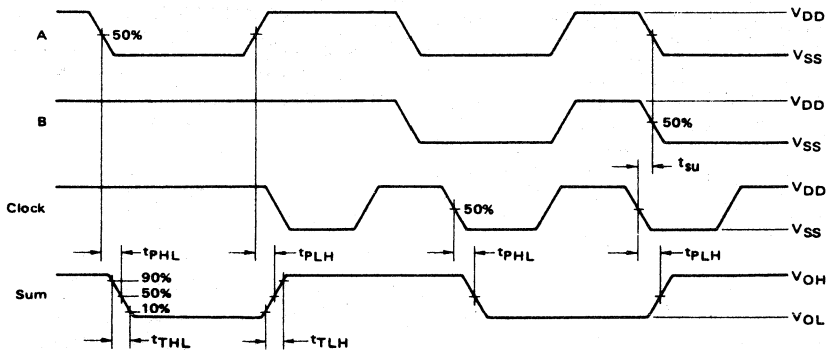
FIGURE 4 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



MC14032B



MC14038B





MOTOROLA

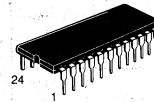
MC14034B

8-BIT UNIVERSAL BUS REGISTER

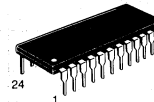
The MC14034B is a bidirectional 8-bit static parallel/serial, input/output bus register. The device contains two sets of input/output lines which allows the bidirectional transfer of data between two buses; the conversion of serial data to parallel form, or the conversion of parallel data to serial form. Additionally the serial data input allows data to be entered shift/right, while shift/left can be accomplished by hard-wiring each parallel output to the previous parallel bit input.

Other useful applications for this device include pseudo-random code generation, sample and hold register, frequency and phase-comparator, address or buffer register, and serial/parallel input/output conversions.

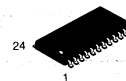
- Bidirectional Parallel Data Input
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range.
- Pin-for-Pin Replacement for CD4034B.



L SUFFIX
CERAMIC
CASE 623



P SUFFIX
PLASTIC
CASE 709



DW SUFFIX
SOIC
CASE 751E

ORDERING INFORMATION

MC14XXXBCP. Plastic
MC14XXXBCL. Ceramic
MC14XXXBDW. SOIC

T_A = -55° to 125°C for all packages.

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V _{DD}	DC Supply Voltage	-0.5 to +18.0	V
V _{in} , V _{out}	Input or Output Voltage (DC or Transient)	-0.5 to V _{DD} + 0.5	V
I _{in} , I _{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
P _D	Power Dissipation, per Package†	500	mW
T _{stg}	Storage Temperature	-65 to +150	°C
T _L	Lead Temperature (8-Second Soldering)	260	°C

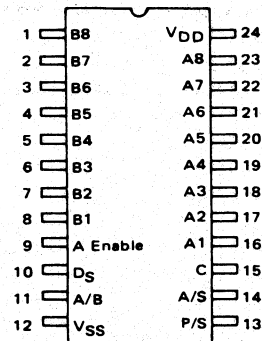
*Maximum Ratings are those values beyond which damage to the device may occur.

†Temperature Derating: Plastic "P and D/DW" Packages: -7.0 mW/°C From 65°C To 125°C
Ceramic "L" Packages: -12 mW/°C From 100°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range V_{SS} ≤ (V_{in} or V_{out}) ≤ V_{DD}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

PIN ASSIGNMENT



MC14034B

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V _{DD} Vdc	-55°C		25°C			125°C		Unit	
			Min	Max	Min	Typ #	Max	Min	Max		
Output Voltage V _{in} = V _{DD} or 0	V _{OL}	5.0	—	0.05	—	0	0.05	—	0.05	Vdc	
		10	—	0.05	—	0	0.05	—	0.05		
15		—	0.05	—	—	0	0.05	—	0.05		
V _{in} = 0 or V _{DD}	V _{OH}	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc	
		10	9.95	—	9.95	10	—	9.95	—		
		15	14.95	—	14.95	15	—	14.95	—		
Input Voltage (V _O = 4.5 or 0.5 Vdc) (V _O = 9.0 or 1.0 Vdc) (V _O = 13.5 or 1.5 Vdc)	V _{IL}	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc	
		10	—	3.0	—	4.50	3.0	—	3.0		
		15	—	4.0	—	6.75	4.0	—	4.0		
(V _O = 0.5 or 4.5 Vdc) (V _O = 1.0 or 9.0 Vdc) (V _O = 1.5 or 13.5 Vdc)	V _{IH}	5.0	3.5	—	3.5	2.75	—	3.5	—	Vdc	
		10	7.0	—	7.0	5.50	—	7.0	—		
		15	11	—	11	8.25	—	11	—		
Output Drive Current (V _{OH} = 2.5 Vdc) (V _{OH} = 4.6 Vdc) (V _{OH} = 9.5 Vdc) (V _{OH} = 13.5 Vdc)	Source	I _{OH}	5.0	-1.2	—	-1.0	-1.7	—	-0.7	—	mAdc
			5.0	-0.25	—	-0.2	-0.36	—	-0.14	—	
			10	-0.62	—	-0.5	-0.9	—	-0.35	—	
			15	-1.8	—	-1.5	-3.5	—	-1.1	—	
	Sink	I _{OL}	5.0	0.64	—	0.51	0.88	—	0.36	—	mAdc
			10	1.6	—	1.3	2.25	—	0.9	—	
15	4.2	—	3.4	8.8	—	2.4	—	—			
Input Current	I _{in}	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	μAdc	
Input Capacitance (V _{in} = 0)	C _{in}	—	—	—	—	5.0	7.5	—	—	pF	
Quiescent Current (Per Package)	I _{DD}	5.0	—	5.0	—	0.010	5.0	—	150	μAdc	
		10	—	10	—	0.020	10	—	300		
		15	—	20	—	0.030	20	—	600		
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C _L = 50 pF on all outputs, all buffers switching)	I _T	5.0	I _T = (2.2 μA/kHz) f + I _{DD}							μAdc	
		10	I _T = (4.4 μA/kHz) f + I _{DD}								
		15	I _T = (6.6 μA/kHz) f + I _{DD}								
3-State Output Leakage Current	I _{TL}	15	—	±0.1	—	±0.0001	±0.1	—	±3.0	μAdc	

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) V/k$$

where: I_T is in μA (per package), C_L in pF, V = (V_{DD} - V_{SS}) in volts, f in kHz is input frequency, and k = 0.004.

MC14034B

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V _{DD} V _{dC}	Min	Typ #	Max	Unit
Output Rise Time A or B t _{TLH} = (3.0 ns/pF) C _L + 30 ns t _{TLH} = (1.5 ns/pF) C _L + 15 ns t _{TLH} = (1.1 ns/pF) C _L + 10 ns	t _{TLH}	5.0 10 15	— — —	180 90 65	360 180 130	ns
Output Fall Time A or B t _{THL} = (1.5 ns/pF) C _L + 25 ns t _{THL} = (0.75 ns/pF) C _L + 12.5 ns t _{THL} = (0.55 ns/pF) C _L + 9.5 ns	t _{THL}	5.0 10 15	— — —	100 50 40	200 100 80	ns
Propagation Delay Time A (B) Synchronous Parallel Data Input, B (A) Parallel Data Output t _{PLH} , t _{PHL} = (1.7 ns/pF) C _L + 440 ns t _{PHL} , t _{PHL} = (0.66 ns/pF) C _L + 172 ns t _{PLH} , t _{PHL} = (0.5 ns/pF) C _L + 120 ns	t _{PLH} , t _{PHL}	5.0 10 15	— — —	525 205 145	1050 410 290	ns
Propagation Delay Time A (B) Asynchronous Parallel Data Input B (A) Parallel Data Output t _{PLH} , t _{PHL} = (1.7 ns/pF) C _L + 420 ns t _{PLH} , t _{PHL} = (0.66 ns/pF) C _L + 147 ns t _{PLH} , t _{PHL} = (0.5 ns/pF) C _L + 105 ns	t _{PLH} , t _{PHL}	5.0 10 15	— — —	505 180 130	1010 360 260	ns
Clock Pulse Width	t _{WH}	5.0 10 15	340 140 110	170 70 55	— — —	ns
Clock Pulse Frequency	f _{cl}	5.0 10 15	— — —	2.5 6.0 8.0	1.2 3.0 4.0	MHz
Clock Pulse Rise	t _{TLH} , t _{THL}	5.0 10 15	— — —	— — —	15 5 4	μs
A, B Input Setup Time	t _{su}	5.0 10 15	100 45 35	35 15 12	— — —	ns
High Level SE, P/S, A/S Pulse Width	t _{WH}	5.0 10 15	600 270 200	200 90 80	— — —	ns

*The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

6

TRUTH TABLE

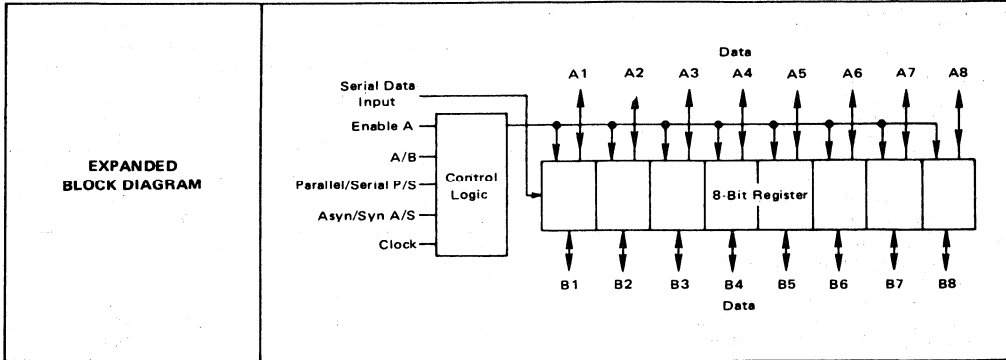
"A" Enable	P/S	A/B	A/S	MODE	OPERATION†
0	0	0	X	Serial	Synchronous Serial data input, A and B parallel data outputs disabled.
0	0	1	X	Serial	Synchronous Serial data input, B-Parallel data output.
0	1	0	0	Parallel	B Synchronous Parallel data inputs, A-Parallel data outputs disabled.
0	1	0	1	Parallel	B Asynchronous Parallel data inputs, A-Parallel data outputs disabled.
0	1	1	0	Parallel	A-Parallel data inputs disabled, B-Parallel data outputs.
0	1	1	1	Parallel	A-Parallel data inputs disabled, B-Parallel data outputs.
1	0	0	X	Serial	Synchronous serial data input, A-Parallel data output.
1	0	1	X	Serial	Synchronous serial data input, B-Parallel data output.
1	1	0	0	Parallel	B-Synchronous Parallel data input, A-Parallel data output.
1	1	0	1	Parallel	B-Asynchronous Parallel data input, A-Parallel data output.
1	1	1	0	Parallel	A-Synchronous Parallel data input, B-Parallel data output.
1	1	1	1	Parallel	A-Asynchronous Parallel data input, B-Parallel data output.

X = Don't Care

†Outputs change at positive transition of clock in the serial mode and when the A/S input is low in the parallel mode.

During transfer from parallel to serial operation, A/S should remain low in order to prevent D_S transfer into flip-flops.

MC14034B



OPERATING CHARACTERISTICS

The MC14034B is composed of eight register cells connected in cascade with additional control logic. Each register cell is composed of one "D" master-slave flip-flop with separate internal clocks, and two data transfer gates allowing the data to be transferred bidirectionally from bus A to bus B and from bus B to bus A, and to be memorized. Besides the single phase clock and the serial data inputs, the control logic provides four other features:

A Enable Input — When high, this input enables the bus A data lines.

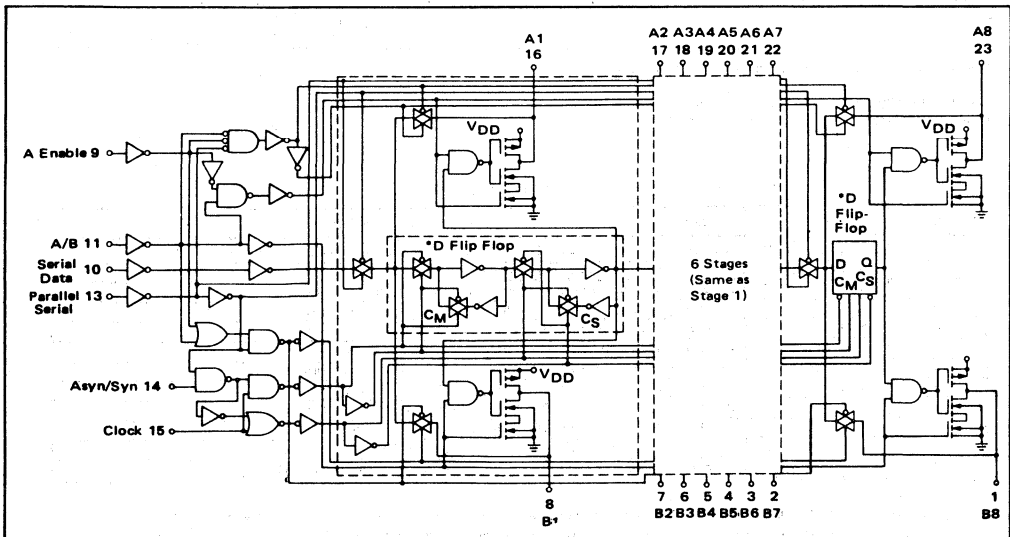
A/B Input (Data A or B) — This input controls the direction of data flow: when high, the data flows from

bus A to bus B; when low, the data flows from bus B to bus A.

P/S Input (Parallel/Serial) — This input controls the data input mode (parallel or serial). When high, the data is transferred to the register in a parallel asynchronous mode or a parallel synchronous mode (positive clock transition). When low, the data is entered into the register in a serial synchronous mode (positive clock transition).

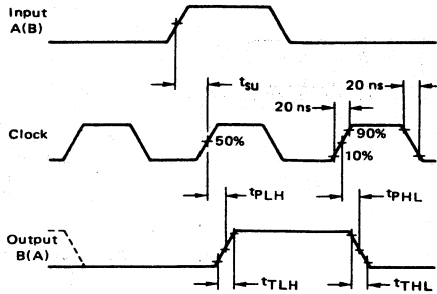
A/S Input (Asynchronous/Synchronous to the Clock) — When this input is high, the data is transferred independently from the clock rate; when low, the clock is enabled and the data is transferred synchronously.

LOGIC DIAGRAM



MC14034B

FIGURE 1 – PROPAGATION DELAY AND TRANSITION TIMES WAVEFORMS



PROPAGATION AND TRANSITION TIME TEST CIRCUITS

FIGURE 2 – A SYNCHRONOUS DATA INPUT, B PARALLEL DATA OUTPUT AND SETUP TIME

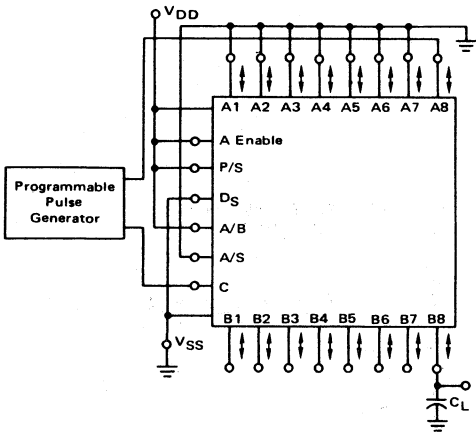
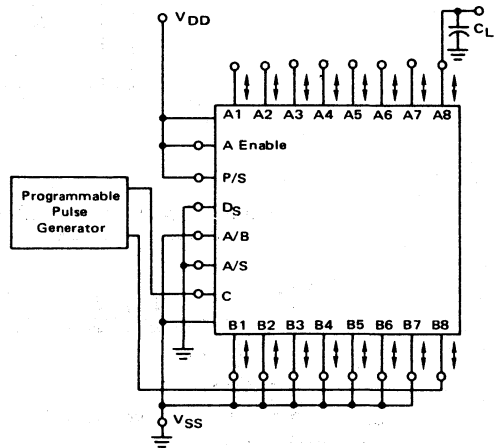


FIGURE 3 – B SYNCHRONOUS DATA INPUT, A PARALLEL DATA OUTPUT AND SETUP TIME



MC14034B

FIGURE 4 - POWER DISSIPATION TEST CIRCUIT AND WAVEFORMS

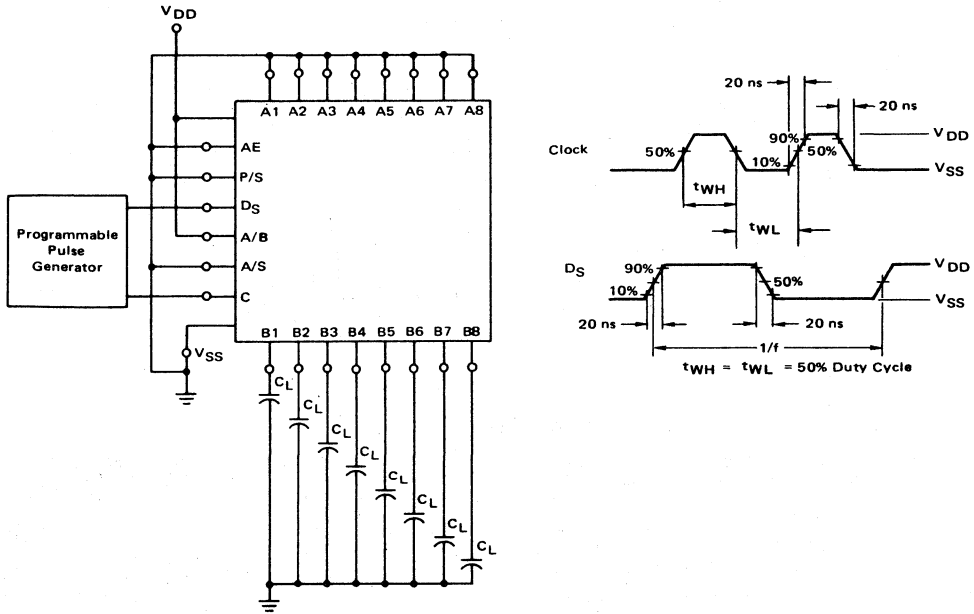
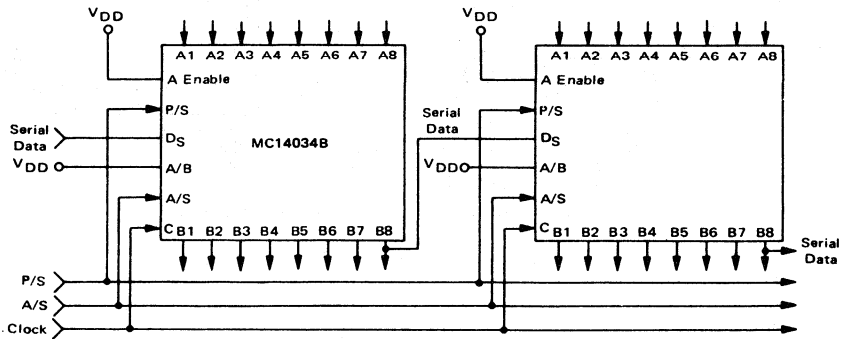


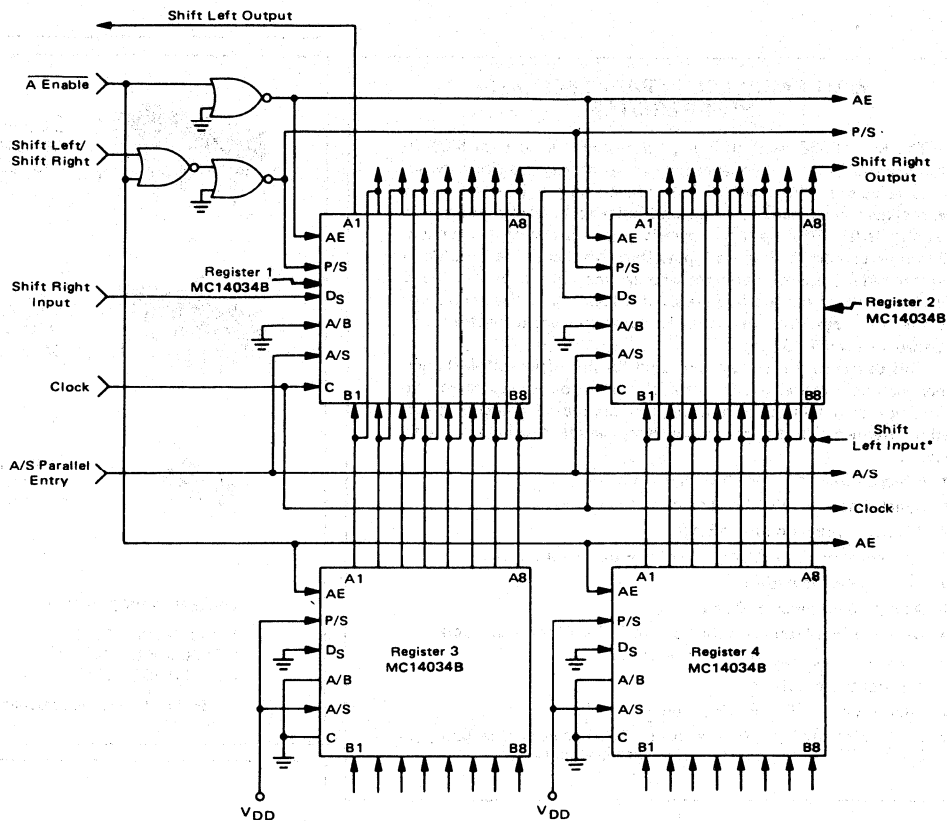
FIGURE 5 - 16-BIT PARALLEL IN/PARALLEL OUT, PARALLEL IN/SERIAL OUT, SERIAL IN/PARALLEL OUT, SERIAL IN/SERIAL OUT REGISTER



6

MC14034B

FIGURE 6 – SHIFT RIGHT/SHIFT LEFT WITH PARALLEL INPUTS



A "High" ("Low") on the Shift Left/Shift Right input allows serial data on the Shift Left Input (Shift Right Input) to enter the register on the positive transition of the clock signal. A "high" on the "A" Enable Input disables the "A" parallel data lines on Reg. 1 and 2 and enables the "A" data lines on registers 3 and 4 and allows parallel data into registers 1 and 2. Other logic schemes may be used in place of registers 3 and 4 for parallel loading.

When parallel inputs are not used Reg. 3 and 4 and associated logic are not required.

*Shift left input must be disabled during parallel entry.



MOTOROLA

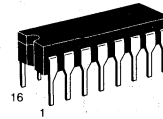
MC14035B

**4-BIT PARALLEL-IN/PARALLEL-OUT
SHIFT REGISTER**

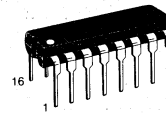
The MC14035B 4-bit shift register is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. It consists of a 4-stage clocked serial-shift register with synchronous parallel inputs and buffered parallel outputs. The Parallel/Serial (P/S) input allows serial-right shifting of data or synchronous parallel loading via inputs Dp₃ thru Dp₀. The True/Complement (T/C) input determines whether the outputs display the Q or \bar{Q} outputs of the flip-flop stages. J-K logic forms the serial input to the first stage. With the J and K inputs connected together they operate as a serial "D" input.

This device may be effectively used for shift-right/shift-left registers, parallel-to-serial/serial-to-parallel conversion, sequence generation, up/down Johnson or ring counters, pseudo-random code generation, frequency and phase comparators, sample and hold registers, etc. . . .

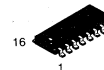
- 4-Stage Clocked Serial-Shift Operation
- Synchronous Parallel Loading of all Four Stages
- J-K Serial Inputs on First Stage
- Asynchronous True/Complement Control of all Outputs
- Fully Static Operation
- Asynchronous Master Reset
- Data Transfer Occurs on the Positive-Going Clock Transition
- No Limit on Clock Rise and Fall Times
- All Inputs are Buffered
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range



**L SUFFIX
CERAMIC
CASE 620**



**P SUFFIX
PLASTIC
CASE 648**



**D SUFFIX
SOIC
CASE 751B**

ORDERING INFORMATION

MC14XXXBCP Plastic
MC14XXXBCL Ceramic
MC14XXXBD SOIC

T_A = -55° to 125°C for all packages.

6

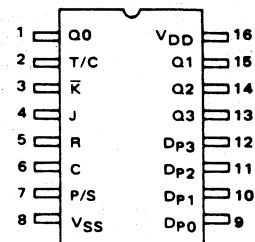
MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V _{DD}	DC Supply Voltage	-0.5 to +18.0	V
V _{in, Vout}	Input or Output Voltage (DC or Transient)	-0.5 to V _{DD} + 0.5	V
I _{in, Iout}	Input or Output Current (DC or Transient), per Pin	± 10	mA
P _D	Power Dissipation, per Package†	500	mW
T _{stg}	Storage Temperature	-65 to +150	°C
T _L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.

†Temperature Derating: Plastic "P and D/DW" Packages: -7.0 mW/°C From 65°C To 125°C
Ceramic "L" Packages: -12 mW/°C From 100°C To 125°C

PIN ASSIGNMENT



TRUTH TABLE

INPUTS				t _n OUTPUT
C	J	K	R	Q0
0	0	0	0	0
0	1	0	0	Q0 (n-1)
0	1	0	0	$\bar{Q}0$ (n-1)
1	1	0	0	1
x	x	x	0	Q0 (n-1)
x	x	x	1	0

x = Don't Care
P/S = 0 = Serial Mode
T/C = 1 = True Outputs

MC14035B

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V _{DD} Vdc	-55°C		25°C			125°C		Unit
			Min	Max	Min	Typ #	Max	Min	Max	
Output Voltage V _{in} = V _{DD} or 0	V _{OL}	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
		10	—	0.05	—	0	0.05	—	0.05	
V _{in} = 0 or V _{DD}	V _{OH}	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc
		10	9.95	—	9.95	10	—	9.95	—	
Input Voltage (V _O = 4.5 or 0.5 Vdc) (V _O = 9.0 or 1.0 Vdc) (V _O = 13.5 or 1.5 Vdc)	V _{IL}	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc
		10	—	3.0	—	4.50	3.0	—	3.0	
(V _O = 0.5 or 4.5 Vdc) (V _O = 1.0 or 9.0 Vdc) (V _O = 1.5 or 13.5 Vdc)	V _{IH}	5.0	3.5	—	3.5	2.75	—	3.5	—	Vdc
		10	7.0	—	7.0	5.50	—	7.0	—	
Output Drive Current (V _{OH} = 2.5 Vdc) (V _{OH} = 4.6 Vdc) (V _{OH} = 9.5 Vdc) (V _{OH} = 13.5 Vdc)	Source I _{OH}	5.0	-3.0	—	-2.4	-4.2	—	-1.7	—	mAdc
		10	-0.64	—	-0.51	-0.88	—	-0.36	—	
(V _{OL} = 0.4 Vdc) (V _{OL} = 0.5 Vdc) (V _{OL} = 1.5 Vdc)	Sink I _{OL}	5.0	0.64	—	0.51	0.88	—	0.36	—	mAdc
		10	1.6	—	1.3	2.25	—	0.9	—	
		15	4.2	—	3.4	8.8	—	2.4	—	
Input Current	I _{in}	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	μAdc
Input Capacitance (V _{in} = 0)	C _{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)	I _{DD}	5.0	—	5.0	—	0.005	5.0	—	150	μAdc
		10	—	10	—	0.010	10	—	300	
		15	—	20	—	0.015	20	—	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C _L = 50 pF on all outputs, all buffers switching)	I _T	5.0				I _T = (1.0 μA/kHz) f + I _{DD}			μAdc	
10				I _T = (2.0 μA/kHz) f + I _{DD}						
15				I _T = (3.0 μA/kHz) f + I _{DD}						

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) V_{ik}$$

where: I_T is in μA (per package), C_L in pF, V = (V_{DD} - V_{SS}) in volts, f in kHz is input frequency, and k = 0.001.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range V_{SS} ≤ (V_{in} or V_{out}) ≤ V_{DD}. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

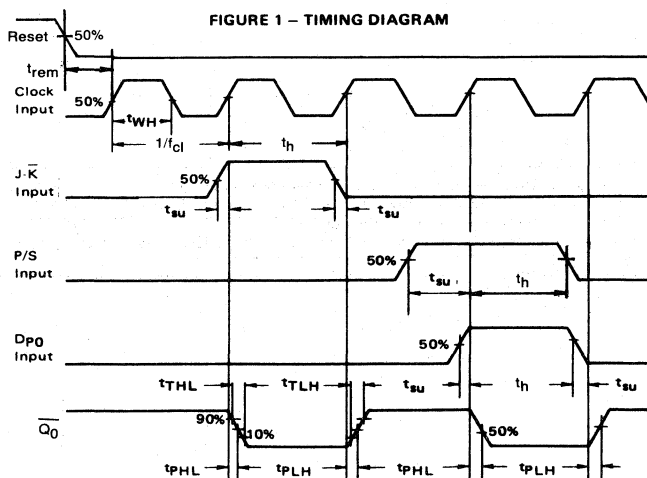
MC14035B

SWITCHING CHARACTERISTICS (C_L = 50 pF, T_A = 25°C, See Figure 1)

Characteristic	Symbol	V _{DD} V _{dC}	Min	Typ #	Max	Unit
Output Rise and Fall Time T _{TLH} , T _{THL} = (1.5 ns/pF) C _L + 25 ns T _{TLH} , T _{THL} = (0.75 ns/pF) C _L + 12.5 ns T _{TLH} , T _{THL} = (0.55 ns/pF) C _L + 12.5 ns	t _{TLH} , t _{THL}	5.0 10 15	—	100 50 40	200 100 80	ns
Propagation Delay Time, Clock or Reset to Q T _{PLH} , T _{PHL} = (1.75 ns/pF) C _L + 223 ns T _{PLH} , T _{PHL} = (0.70 ns/pF) C _L + 89 ns T _{PLH} , T _{PHL} = (0.53 ns/pF) C _L + 67 ns	t _{PLH} , t _{PHL}	5.0 10 15	—	300 130 95	600 260 190	ns
Clock Pulse Width	t _{WH}	5.0 10 15	335 165 125	135 45 40	— — —	ns
Reset Pulse Width	t _{WH}	5.0 10 15	400 175 130	80 40 35	— — —	ns
Reset Removal Time	t _{rem}	5.0 10 15	80 30 25	40 15 10	— — —	ns
Clock Pulse Rise and Fall Time	t _{TLH} , t _{THL}	5.0 10 15	No Limit			—
Clock Pulse Frequency	f _{cl}	5.0 10 15	— — —	2.5 6.0 10	1.2 2.0 3.0	MHz
J-K̄ to Clock Setup Time	t _{su}	5.0 10 15	500 200 150	120 50 30	— — —	ns
Clock to J-K̄ Hold Time	t _h	5.0 10 15	40 30 25	-40 -5 0	— — —	ns
P/S to Clock Setup Time	t _{su}	5.0 10 15	500 200 150	25 10 7.5	— — —	ns
Clock to P/S Hold Time	t _h	5.0 10 15	30 20 20	-70 -20 -10	— — —	ns
D _p to Clock Setup Time	t _{su}	5.0 10 15	500 200 150	90 20 15	— — —	ns
Clock to D _p Hold Time	t _h	5.0 10 15	90 40 40	-25 0 5	— — —	ns

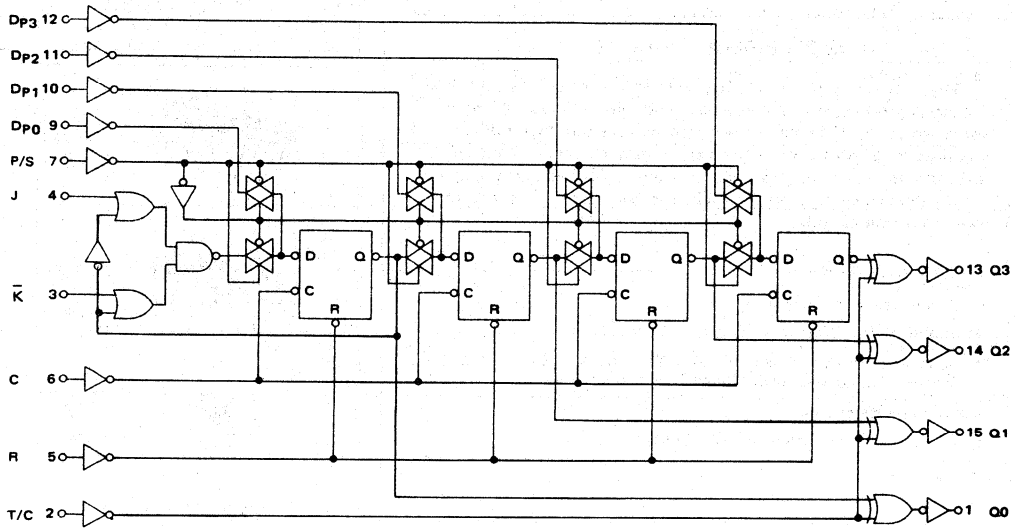
*The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

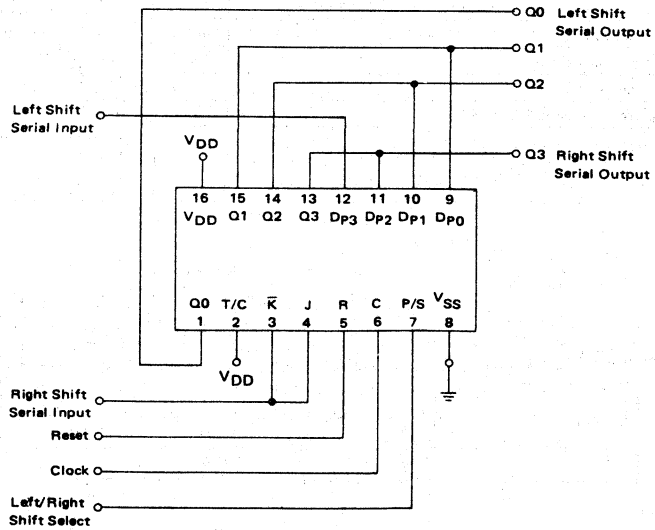


MC14035B

LOGIC DIAGRAM



APPLICATION DIAGRAM Shift Left/Shift Right Register





MOTOROLA

MC14038B
See Page 6-92

MC14040B

12-BIT BINARY COUNTER

The MC14040B 12-stage binary counter is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. This part is designed with an input wave shaping circuit and 12 stages of ripple-carry binary counter. The device advances the count on the negative-going edge of the clock pulse. Applications include time delay circuits, counter controls, and frequency-driving circuits.

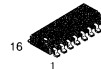
- Fully Static Operation
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range
- Common Reset Line
- Pin-for-Pin Replacement for CD4040B



L SUFFIX
CERAMIC
CASE 620



P SUFFIX
PLASTIC
CASE 648



D SUFFIX
SOIC
CASE 751B

ORDERING INFORMATION

MC14XXXBCP Plastic
MC14XXXBCL Ceramic
MC14XXXBD SOIC

T_A = -55° to 125°C for all packages.

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V _{DD}	DC Supply Voltage	-0.5 to +18.0	V
V _{in} , V _{out}	Input or Output Voltage (DC or Transient)	-0.5 to V _{DD} + 0.5	V
I _{in} , I _{out}	Input or Output Current (DC or Transient), per Pin	± 10	mA
P _D	Power Dissipation, per Package†	500	mW
T _{stg}	Storage Temperature	-65 to +150	°C
T _L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.

†Temperature Derating: Plastic "P and D/DW" Packages: -7.0 mW/°C From 65°C To 125°C
Ceramic "L" Packages: -12 mW/°C From 100°C To 125°C

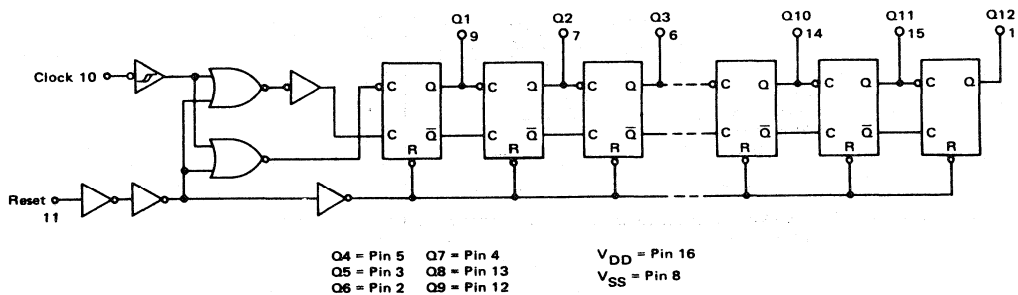
TRUTH TABLE

CLOCK	RESET	OUTPUT STATE
	0	No Change
	0	Advance to next state
X	1	All Outputs are low

X = Don't Care

6

LOGIC DIAGRAM



MC14040B

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V _{DD} Vdc	-55°C		25°C			125°C		Unit
			Min	Max	Min	Typ #	Max	Min	Max	
Output Voltage V _{in} = V _{DD} or 0 V _{in} = 0 or V _{DD}	"0" Level V _{OL}	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
		10	—	0.05	—	0	0.05	—	0.05	
		15	—	0.05	—	0	0.05	—	0.05	
	"1" Level V _{OH}	5.0	4.95	—	4.95	5.0	—	4.95	—	
		10	9.95	—	9.95	10	—	9.95	—	
		15	14.95	—	14.95	15	—	14.95	—	
Input Voltage (V _O = 4.5 or 0.5 Vdc) (V _O = 9.0 or 1.0 Vdc) (V _O = 13.5 or 1.5 Vdc) (V _O = 0.5 or 4.5 Vdc) (V _O = 1.0 or 9.0 Vdc) (V _O = 1.5 or 13.5 Vdc)	"0" Level V _{IL}	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc
		10	—	3.0	—	4.50	3.0	—	3.0	
		15	—	4.0	—	6.75	4.0	—	4.0	
	"1" Level V _{IH}	5.0	3.5	—	3.5	2.75	—	3.5	—	
		10	7.0	—	7.0	5.50	—	7.0	—	
		15	11	—	11	8.25	—	11	—	
Output Drive Current (V _{OH} = 2.5 Vdc) (V _{OH} = 4.6 Vdc) (V _{OH} = 9.5 Vdc) (V _{OH} = 13.5 Vdc) (V _{OL} = 0.4 Vdc) (V _{OL} = 0.5 Vdc) (V _{OL} = 1.5 Vdc)	Source I _{OH}	5.0	-3.0	—	-2.4	-4.2	—	-1.7	—	mAdc
		5.0	-0.64	—	-0.51	-0.88	—	-0.36	—	
		10	-1.6	—	-1.3	-2.25	—	-0.9	—	
		15	-4.2	—	-3.4	-8.8	—	-2.4	—	
	Sink I _{OL}	5.0	0.64	—	0.51	0.88	—	0.36	—	
		10	1.6	—	1.3	2.25	—	0.9	—	
15	4.2	—	3.4	8.8	—	2.4	—	—		
Input Current	I _{in}	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	μAdc
Input Capacitance (V _{in} = 0)	C _{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)	I _{DD}	5.0	—	5.0	—	0.005	5.0	—	150	μAdc
		10	—	10	—	0.010	10	—	300	
		15	—	20	—	0.015	20	—	600	
Total Supply Current**†† (Dynamic plus Quiescent, Per Package) (C _L = 50 pF on all outputs, all buffers switching)	I _T	5.0	I _T = (0.42 μA/kHz) f + I _{DD}						μAdc	
		10	I _T = (0.85 μA/kHz) f + I _{DD}							
		15	I _T = (1.43 μA/kHz) f + I _{DD}							

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

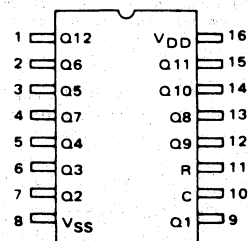
$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) Vfk$$

where: I_T is in μA (per package), C_L in pF, V = (V_{DD} - V_{SS}) in volts, f in kHz is input frequency, and k = 0.001.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range V_{SS} ≤ (V_{in} or V_{out}) ≤ V_{DD}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

PIN ASSIGNMENT



MC14040B

SWITCHING CHARACTERISTICS (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V _{DD} V _{dc}	Min	Typ #	Max	Unit
Output Rise and Fall Time T _{TLH} , T _{THL} = (1.5 ns/pF) C _L + 25 ns T _{TLH} , T _{THL} = (0.75 ns/pF) C _L + 12.5 ns T _{TLH} , T _{THL} = (0.55 ns/pF) C _L + 9.5 ns	t _{TLH} , t _{THL}	5.0 10 15	— — —	100 50 40	200 100 80	ns
Propagation Delay Time Clock to Q1 t _{PHL} , t _{PLH} = (1.7 ns/pF) C _L + 315 ns t _{PHL} , t _{PLH} = (0.66 ns/pF) C _L + 137 ns t _{PHL} , t _{PLH} = (0.5 ns/pF) C _L + 95 ns Clock to Q12 t _{PHL} , t _{PLH} = (1.7 ns/pF) C _L + 2415 ns t _{PHL} , t _{PLH} = (0.66 ns/pF) C _L + 867 ns t _{PHL} , t _{PLH} = (0.5 ns/pF) C _L + 475 ns	t _{PLH} , t _{PHL}	5.0 10 15	— — —	260 115 80	520 230 160	ns
Propagation Delay Time Reset to Q _n t _{PHL} = (1.7 ns/pF) C _L + 485 ns t _{PHL} = (0.66 ns/pF) C _L + 182 ns t _{PHL} = (0.5 ns/pF) C _L + 145 ns	t _{PHL}	5.0 10 15	— — —	370 155 115	740 310 230	ns
Clock Pulse Width	t _{WH}	5.0 10 15	385 150 115	140 55 38	— — —	ns
Clock Pulse Frequency	f _{cl}	5.0 10 15	— — —	2.1 7.0 10.0	1.5 3.5 4.5	MHz
Clock Rise and Fall Time	t _{TLH} , t _{THL}	5.0 10 15	No Limit			ns
Reset Pulse Width	t _{WH}	5.0 10 15	960 360 270	320 120 80	— — —	ns
Reset Removal Time	t _{rem}	5.0 10 15	130 50 30	65 25 15	— — —	ns

*The formulas given are for the typical characteristics only at 25°C.
#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

FIGURE 1 – POWER DISSIPATION TEST
CIRCUIT AND WAVEFORM

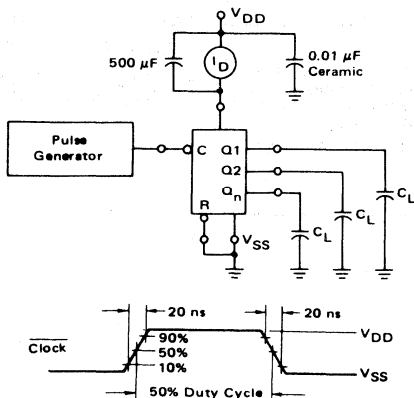
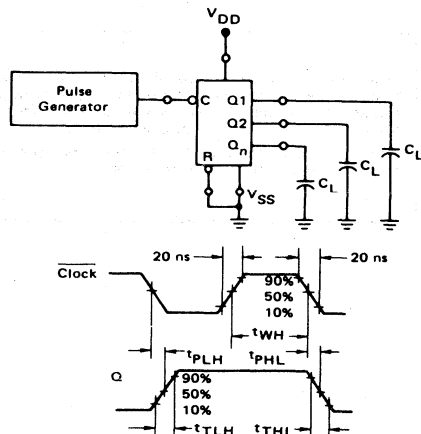
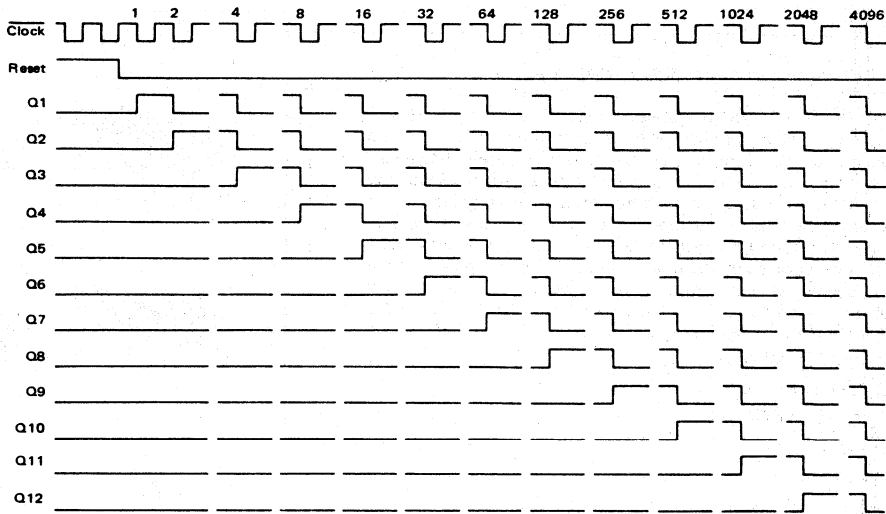


FIGURE 2 – SWITCHING TIME TEST
CIRCUIT AND WAVEFORMS



MC14040B

FIGURE 3 – TIMING DIAGRAM

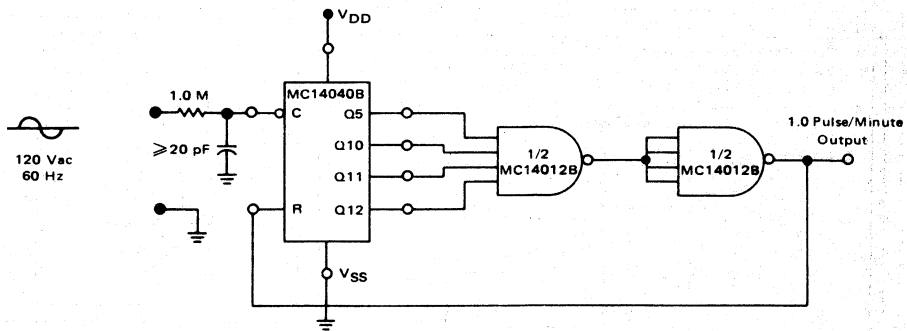


APPLICATIONS INFORMATION

TIME-BASE GENERATOR

A 60 Hz sinewave obtained through a 1.0 Megohm resistor connected directly to a standard 120 Vac power line is applied to the clock input of the MC14040B. By selecting outputs Q5, Q10, Q11, and Q12 division by

3600 is accomplished. The MC14012B decodes the counter outputs, produces a single output pulse, and resets the binary counter. The resulting output frequency is 1.0 pulse/minute.





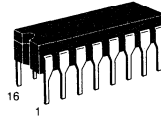
MOTOROLA

MC14042B

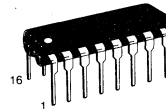
QUAD TRANSPARENT LATCH

The MC14042B Quad Transparent Latch is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. Each latch has a separate data input, but all four latches share a common clock. The clock polarity (high or low) used to strobe data through the latches can be reversed using the polarity input. Information present at the data input is transferred to outputs Q and \bar{Q} during the clock level which is determined by the polarity input. When the polarity input is in the logic "0" state, data is transferred during the low clock level, and when the polarity input is in the logic "1" state the transfer occurs during the high clock level.

- Buffered Data Inputs
- Common Clock
- Clock Polarity Control
- Q and \bar{Q} Outputs
- Double Diode Input Protection
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range



L SUFFIX
CERAMIC
CASE 620



P SUFFIX
PLASTIC
CASE 648



D SUFFIX
SOIC
CASE 751B

ORDERING INFORMATION

MC14XXXBCP Plastic
MC14XXXBCL Ceramic
MC14XXXBD SOIC

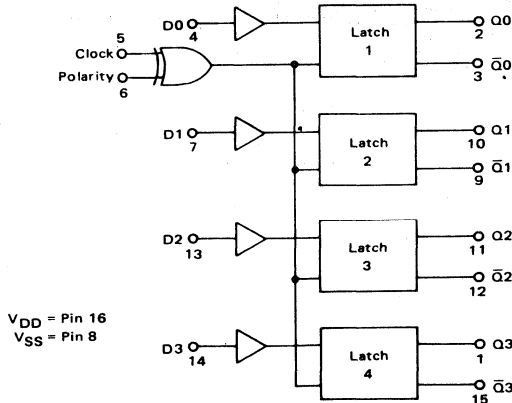
T_A = -55° to 125°C for all packages.

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

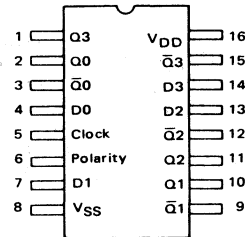
Symbol	Parameter	Value	Unit
V _{DD}	DC Supply Voltage	-0.5 to +18.0	V
V _{in} , V _{out}	Input or Output Voltage (DC or Transient)	-0.5 to V _{DD} + 0.5	V
I _{in} , I _{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
P _D	Power Dissipation, per Package†	500	mW
T _{stg}	Storage Temperature	-65 to +150	°C
T _L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P and D/DW" Packages: -7.0 mW/°C From 65°C To 125°C
Ceramic "L" Packages: -12 mW/°C From 100°C To 125°C

LOGIC DIAGRAM



PIN ASSIGNMENT



TRUTH TABLE

CLOCK	POLARITY	Q
0	0	Data
1	0	Latch
1	1	Data
0	1	Latch

MC14042B

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V _{DD} Vdc	-55°C		25°C			125°C		Unit
			Min	Max	Min	Typ #	Max	Min	Max	
Output Voltage V _{in} = V _{DD} or 0 V _{in} = 0 or V _{DD}	V _{OL}	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
		10	—	0.05	—	0	0.05	—	0.05	
		15	—	0.05	—	0	0.05	—	0.05	
	V _{OH}	5.0	4.95	—	4.95	5.0	—	4.95	—	
		10	9.95	—	9.95	10	—	9.95	—	
		15	14.95	—	14.95	15	—	14.95	—	
Input Voltage (V _O = 4.5 or 0.5 Vdc) (V _O = 9.0 or 1.0 Vdc) (V _O = 13.5 or 1.5 Vdc) (V _O = 0.5 or 4.5 Vdc) (V _O = 1.0 or 9.0 Vdc) (V _O = 1.5 or 13.5 Vdc)	V _{IL}	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc
		10	—	3.0	—	4.50	3.0	—	3.0	
		15	—	4.0	—	6.75	4.0	—	4.0	
	V _{IH}	5.0	3.5	—	3.5	2.75	—	3.5	—	
		10	7.0	—	7.0	5.50	—	7.0	—	
		15	11	—	11	8.25	—	11	—	
Output Drive Current (V _{OH} = 2.5 Vdc) (V _{OH} = 4.6 Vdc) (V _{OH} = 9.5 Vdc) (V _{OH} = 13.5 Vdc) (V _{OL} = 0.4 Vdc) (V _{OL} = 0.5 Vdc) (V _{OL} = 1.5 Vdc)	Source I _{OH}	5.0	-3.0	—	-2.4	-4.2	—	-1.7	—	mAdc
		5.0	-0.64	—	-0.51	-0.88	—	-0.36	—	
		10	-1.6	—	-1.3	-2.25	—	-0.9	—	
	Sink I _{OL}	5.0	0.64	—	0.51	0.88	—	0.36	—	
		10	1.6	—	1.3	2.25	—	0.9	—	
		15	4.2	—	3.4	8.8	—	2.4	—	
Input Current	I _{in}	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	μAdc
Input Capacitance (V _{in} = 0)	C _{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)	I _{DD}	5.0	—	1.0	—	0.002	1.0	—	30	μAdc
		10	—	2.0	—	0.004	2.0	—	60	
		15	—	4.0	—	0.006	4.0	—	120	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C _L = 50 pF on all outputs, all buffers switching)	I _T	5.0	I _T = (1.0 μA/kHz) f + I _{DD} I _T = (2.0 μA/kHz) f + I _{DD} I _T = (3.0 μA/kHz) f + I _{DD}						15	μAdc

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) V/k$$

where: I_T is in μA (per package), C_L in pF, V = (V_{DD} - V_{SS}) in volts, f in kHz is input frequency, and k = 0.004.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range V_{SS} ≤ (V_{in} or V_{out}) ≤ V_{DD}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

MC14042B

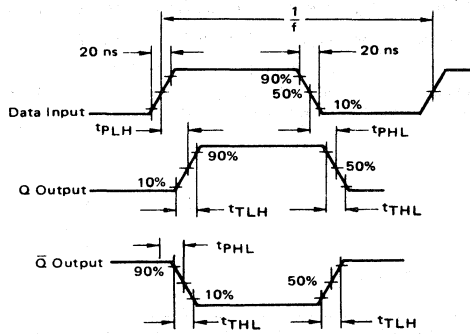
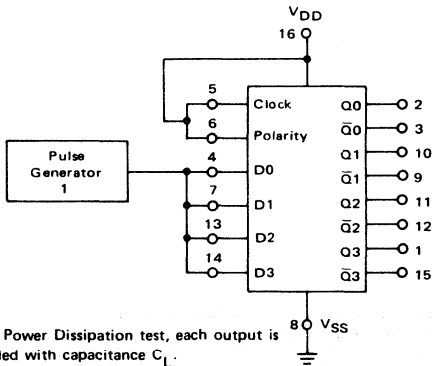
SWITCHING CHARACTERISTICS* ($C_L = 50 \text{ pF}$, $T_A = 25^\circ\text{C}$)

Characteristic	Symbol	V _{DD}	Min	Typ #	Max	Unit
Output Rise and Fall Time $t_{TLH}, t_{THL} = (1.5 \text{ ns/pF}) C_L + 25 \text{ ns}$ $t_{TLH}, t_{THL} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$ $t_{TLH}, t_{THL} = (0.55 \text{ ns/pF}) C_L + 9.5 \text{ ns}$	t_{TLH}, t_{THL}	5.0 10 15	— — —	100 50 40	200 100 80	ns
Propagation Delay Time, D to Q, \bar{Q} $t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 135 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 57 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 35 \text{ ns}$	t_{PLH}, t_{PHL}	5.0 10 15	— — —	220 90 60	440 180 120	ns
Propagation Delay Time, Clock to Q, \bar{Q} $t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 135 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 57 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 35 \text{ ns}$	t_{PLH}, t_{PHL}	5.0 10 15	— — —	220 90 60	440 180 120	ns
Clock Pulse Width	t_{WH}	5.0 10 15	300 100 80	150 50 40	— — —	ns
Clock Pulse Rise and Fall Time	t_{TLH}, t_{THL}	5.0 10 15	— — —	— — —	15 5.0 4.0	μs
Hold Time	t_h	5.0 10 15	100 50 40	50 25 20	— — —	ns
Setup Time	t_{su}	5.0 10 15	50 30 25	0 0 0	— — —	ns

*The formulas given are for the typical characteristics only at 25°C.

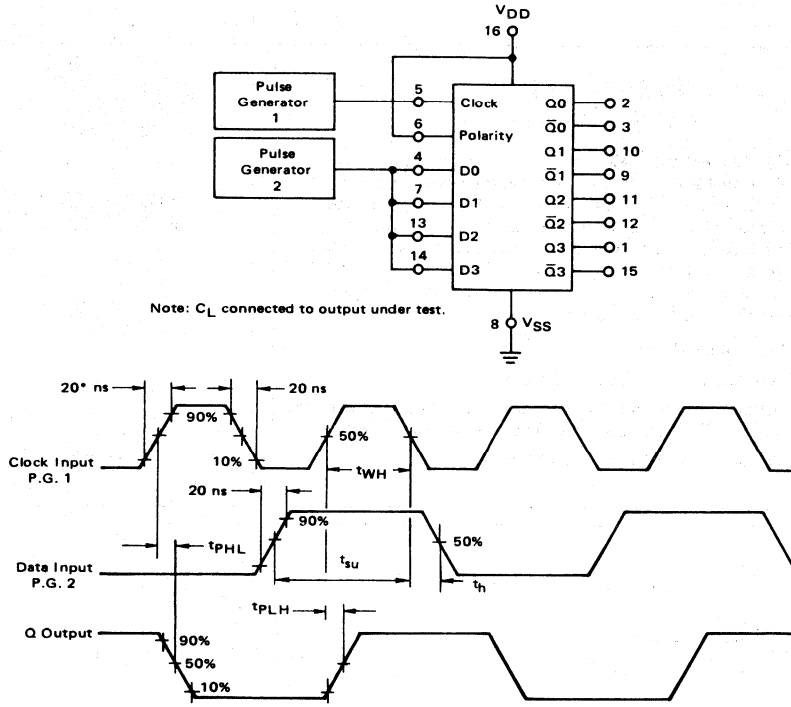
#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

FIGURE 1 – AC AND POWER DISSIPATION TEST CIRCUIT AND TIMING DIAGRAM (Data to Output)



MC14042B

**FIGURE 2 – AC TEST CIRCUIT AND TIMING DIAGRAM
(Clock to Output)**



*Input clock rise time is 20 ns except for maximum rise time test.



MOTOROLA

MC14043B

MC14044B

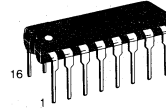
**CMOS MSI
QUAD R-S LATCHES**

The MC14043B and MC14044B quad R-S latches are constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. Each latch has an independent Q output and set and reset inputs. The Q outputs are gated through three-state buffers having a common enable input. The outputs are enabled with a logical "1" or high on the enable input; a logical "0" or low disconnects the latch from the Q outputs, resulting in an open circuit at the Q outputs.

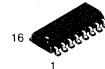
- Double Diode Input Protection
- Three-State Outputs with Common Enable
- Outputs Capable of Driving Two Low-power TTL Loads or One Low-Power Schottky TTL Load Over the Rated Temperature Range
- Supply Voltage Range = 3.0 Vdc to 18 Vdc



**L SUFFIX
CERAMIC
CASE 620**



**P SUFFIX
PLASTIC
CASE 648**



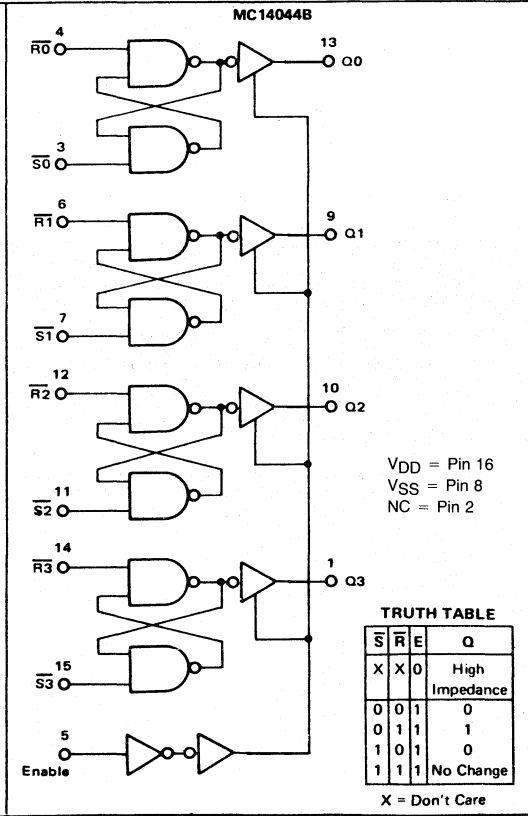
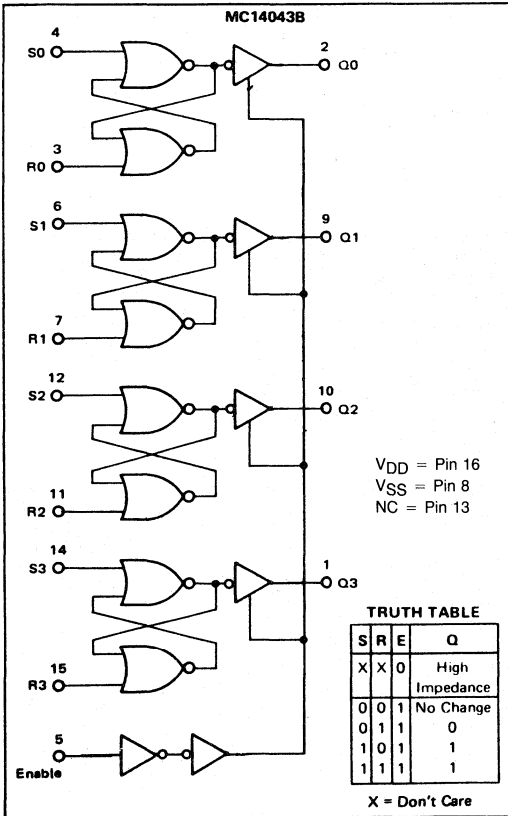
**D SUFFIX
SOIC
CASE 751B**

ORDERING INFORMATION

MC14XXXBCP Plastic
MC14XXXBCL Ceramic
MC14XXXBD SOIC

T_A = -55° to 125°C for all packages.

6



MC14043B•MC14044B

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V _{DD} Vdc	-55°C		25°C			125°C		Unit	
			Min	Max	Min	Typ #	Max	Min	Max		
Output Voltage V _{in} = V _{DD} or 0	V _{OL}	5.0	—	0.05	—	0	0.05	—	0.05	Vdc	
		10	—	0.05	—	0	0.05	—	0.05		
		15	—	0.05	—	0	0.05	—	0.05		
	V _{in} = 0 or V _{DD}	V _{OH}	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc
			10	9.95	—	9.95	10	—	9.95	—	
			15	14.95	—	14.95	15	—	14.95	—	
Input Voltage (V _O = 4.5 or 0.5 Vdc) (V _O = 9.0 or 1.0 Vdc) (V _O = 13.5 or 1.5 Vdc)	V _{IL}	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc	
		10	—	3.0	—	4.50	3.0	—	3.0		
		15	—	4.0	—	6.75	4.0	—	4.0		
	V _O = 0.5 or 4.5 Vdc) (V _O = 1.0 or 9.0 Vdc) (V _O = 1.5 or 13.5 Vdc)	V _{IH}	5.0	3.5	—	3.5	2.75	—	3.5	—	Vdc
			10	7.0	—	7.0	5.50	—	7.0	—	
			15	11	—	11	8.25	—	11	—	
Output Drive Current (V _{OH} = 2.5 Vdc) (V _{OH} = 4.6 Vdc) (V _{OH} = 9.5 Vdc) (V _{OH} = 13.5 Vdc)	Source I _{OH}	5.0	-3.0	—	-2.4	-4.2	—	-1.7	—	mAdc	
		5.0	-0.64	—	-0.51	-0.88	—	-0.36	—		
		10	-1.6	—	-1.3	-2.25	—	-0.9	—		
	Sink I _{OL}	5.0	0.64	—	0.51	0.88	—	0.36	—	mAdc	
		10	1.6	—	1.3	2.25	—	0.9	—		
		15	4.2	—	3.4	8.8	—	2.4	—		
Input Current	I _{in}	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	μAdc	
Input Capacitance (V _{in} = 0)	C _{in}	—	—	—	—	5.0	7.5	—	—	pF	
Quiescent Current (Per Package)	I _{DD}	5.0	—	1.0	—	0.002	1.0	—	30	μAdc	
		10	—	2.0	—	0.004	2.0	—	60		
		15	—	4.0	—	0.006	4.0	—	120		
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C _L = 50 pF on all outputs, all buffers switching)	I _T	5.0	I _T = (0.58 μA/kHz) f + I _{DD}							μAdc	
		10	I _T = (1.15 μA/kHz) f + I _{DD}								
		15	I _T = (1.73 μA/kHz) f + I _{DD}								
Three-State Output Leakage Current	I _{TL}	15	—	±0.1	—	±0.0001	±0.1	—	±3.0	μAdc	

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) \text{ Vfk}$$

where: I_T is in μA (per package), C_L in pF, V = (V_{DD} - V_{SS}) in volts, f in kHz is input frequency, and k = 0.004.

*Maximum Ratings are those values beyond which damage to the device may occur.

†Temperature Derating: Plastic "P and D/DW" Packages: -7.0 mW/°C From 65°C To 125°C
Ceramic "L" Packages: -12 mW/°C From 100°C To 125°C

MC14043B•MC14044B

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V _{DD}	DC Supply Voltage	-0.5 to +18.0	V
V _{in} , V _{out}	Input or Output Voltage (DC or Transient)	-0.5 to V _{DD} + 0.5	V
I _{in} , I _{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
P _D	Power Dissipation, per Package†	500	mW
T _{stg}	Storage Temperature	-65 to +150	°C
T _L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.

†Temperature Derating: Plastic "P and D/DW" Packages: -7.0 mW/°C From 65°C To 125°C

Ceramic "L" Packages: -12 mW/°C From 100°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range V_{SS} ≤ (V_{in} or V_{out}) ≤ V_{DD}. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

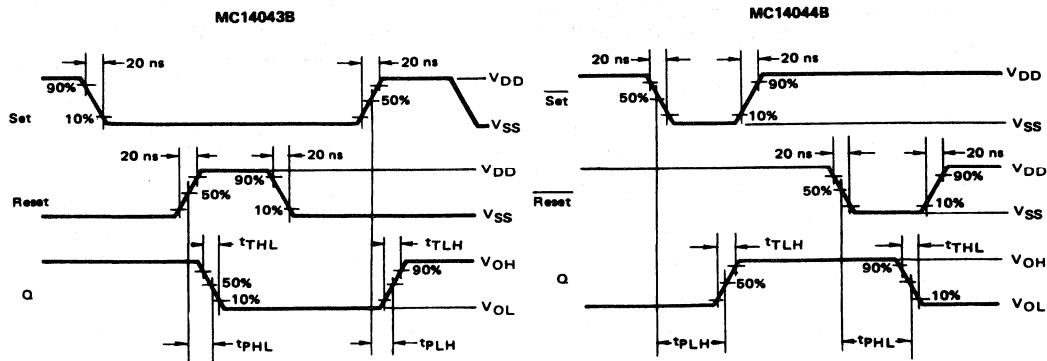
SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V _{DD} V _{dC}	Min	Typ #	Max	Unit
Output Rise Time t _{TLH} = (1.35 ns/pF) C _L + 32.5 ns t _{TLH} = (0.60 ns/pF) C _L + 20 ns t _{TLH} = (0.40 ns/pF) C _L + 20 ns	t _{TLH}	5.0 10 15	- - -	100 50 40	200 100 80	ns
Output Fall Time t _{THL} = (1.35 ns/pF) C _L + 32.5 ns t _{THL} = (0.60 ns/pF) C _L + 20 ns t _{THL} = (0.40 ns/pF) C _L + 20 ns	t _{THL}	5.0 10 15	- - -	100 50 40	200 100 80	ns
Propagation Delay Time t _{PLH} = (0.90 ns/pF) C _L + 130 ns t _{PLH} = (0.36 ns/pF) C _L + 57 ns t _{PLH} = (0.26 ns/pF) C _L + 47 ns t _{PHL} = (0.90 ns/pF) C _L + 130 ns t _{PHL} = (0.90 ns/pF) C _L + 57 ns t _{PHL} = (0.26 ns/pF) C _L + 47 ns	t _{PLH} t _{PHL}	5.0 10 15	- - -	175 75 60	350 175 120	ns
Set, Set Pulse Width	t _w	5.0 10 15	200 100 70	80 40 30	- - -	ns
Reset, Reset Pulse Width	t _w	5.0 10 15	200 100 70	80 40 30	- - -	ns
Three-State Enable/Disable Delay	t _{PLZ} t _{PHZ} t _{PZL} t _{PZH}	5.0 10 15	- - -	150 80 55	300 160 110	ns

*The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

AC WAVEFORMS

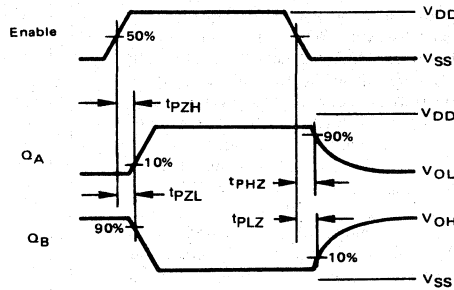
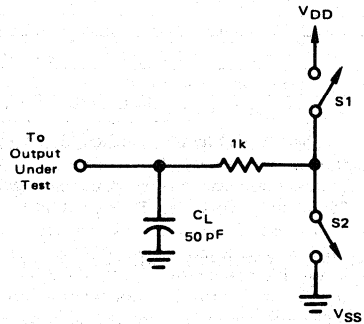


MC14043B•MC14044B

THREE-STATE ENABLE/DISABLE DELAYS

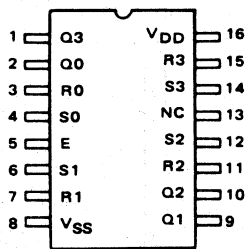
Set, Reset, Enable, and Switch Conditions for 3-State Tests.

TEST	ENABLE	S1	S2	Q	MC14043B		MC14044B	
					S	R	\overline{S}	\overline{R}
t _{pZH}		Open	Closed	A	V _{DD}	V _{SS}	V _{SS}	V _{DD}
t _{pZL}		Closed	Open	B	V _{SS}	V _{DD}	V _{DD}	V _{SS}
t _{pHZ}		Open	Closed	A	V _{DD}	V _{SS}	V _{SS}	V _{DD}
t _{pLZ}		Closed	Open	B	V _{SS}	V _{DD}	V _{DD}	V _{SS}

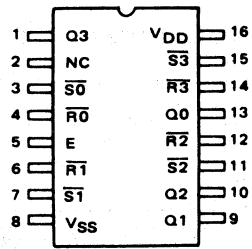


PIN ASSIGNMENT

MC14043B



MC14044B



NC = No Connection



MOTOROLA

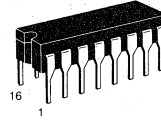
MC14046B

PHASE LOCKED LOOP

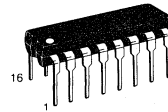
The MC14046B phase locked loop contains two phase comparators, a voltage-controlled oscillator (VCO), source follower, and zener diode. The comparators have two common signal inputs, PCA_{in} and PCB_{in} . Input PCA_{in} can be used directly coupled to large voltage signals, or indirectly coupled (with a series capacitor) to small voltage signals. The self-bias circuit adjusts small voltage signals in the linear region of the amplifier. Phase comparator 1 (an exclusive OR gate) provides a digital error signal $PC1_{out}$, and maintains 90° phase shift at the center frequency between PCA_{in} and PCB_{in} signals (both at 50% duty cycle). Phase comparator 2 (with leading edge sensing logic) provides digital error signals, $PC2_{out}$ and LD, and maintains a 0° phase shift between PCA_{in} and PCB_{in} signals (duty cycle is immaterial). The linear VCO produces an output signal VCO_{out} whose frequency is determined by the voltage of input VCO_{in} and the capacitor and resistors connected to pins $C1A$, $C1B$, $R1$, and $R2$. The source-follower output SF_{out} with an external resistor is used where the VCO_{in} signal is needed but no loading can be tolerated. The inhibit input Inh , when high, disables the VCO and source follower to minimize standby power consumption. The zener diode can be used to assist in power supply regulation.

Applications include FM and FSK modulation and demodulation, frequency synthesis and multiplication, frequency discrimination, tone decoding, data synchronization and conditioning, voltage-to-frequency conversion and motor speed control.

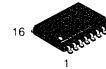
- Buffered Outputs Compatible with MHTL and Low-Power TTL
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 to 18 V
- Pin-for-Pin Replacement for CD4046B
- Phase Comparator 1 is an Exclusive Or Gate and is Duty Cycle Limited
- Phase Comparator 2 switches on Rising Edges and is not Duty Cycle Limited



L SUFFIX
CERAMIC
CASE 620



P SUFFIX
PLASTIC
CASE 648



DW SUFFIX
SOIC
CASE 751G

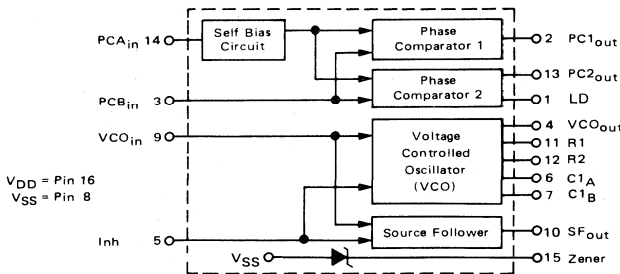
ORDERING INFORMATION

MC14XXXBCP Plastic
MC14XXXBCL Ceramic
MC14XXXBDW SOIC

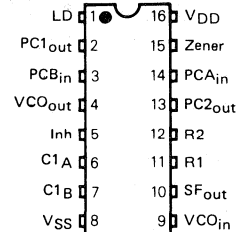
$T_A = -55^\circ$ to 125°C for all packages.

6

BLOCK DIAGRAM



PIN ASSIGNMENT



MC14046B

MAXIMUM RATINGS* (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V _{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V _{in}	-0.5 to V _{DD} +0.5	Vdc
DC Input Current, per Pin	I _{in}	±10	mAdc
Power Dissipation, per Package†	P _D	500	mW
Operating Temperature Range	T _A	-55 to +125	°C
Storage Temperature Range	T _{stg}	-65 to +150	°C

*Maximum Ratings are those values beyond which damage to the device may occur.

†Temperature Derating: Plastic "P and D/DW" Packages: -7.0 mW/°C From 65°C To 125°C
Ceramic "L" Packages: -12 mW/°C From 100°C To 125°C

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V _{DD} Vdc	-55°C		25°C			125°C		Unit
			Min	Max	Min	Typ	Max	Min	Max	
Output Voltage V _{in} = V _{DD} or 0 V _{in} = 0 or V _{DD}	V _{OL}	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
		10	—	0.05	—	0	0.05	—	0.05	
		15	—	0.05	—	0	0.05	—	0.05	
	V _{OH}	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc
		10	9.95	—	9.95	10	—	9.95	—	
		15	14.95	—	14.95	15	—	14.95	—	
Input Voltage # (V _O = 4.5 or 0.5 Vdc) (V _O = 9.0 or 1.0 Vdc) (V _O = 13.5 or 1.5 Vdc) (V _O = 0.5 or 4.5 Vdc) (V _O = 1.0 or 9.0 Vdc) (V _O = 1.5 or 13.5 Vdc)	V _{IL}	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc
		10	—	3.0	—	4.50	3.0	—	3.0	
		15	—	4.0	—	6.75	4.0	—	4.0	
	V _{IH}	5.0	3.5	—	3.5	2.75	—	3.5	—	Vdc
		10	7.0	—	7.0	5.50	—	7.0	—	
		15	11	—	11	8.25	—	11	—	
Output Drive Current (V _{OH} = 2.5 Vdc) (V _{OH} = 4.6 Vdc) (V _{OH} = 9.5 Vdc) (V _{OH} = 13.5 Vdc) (V _{OL} = 0.4 Vdc) (V _{OL} = 0.5 Vdc) (V _{OL} = 1.5 Vdc)	Source I _{OH}	5.0	-1.2	—	-1.0	-1.7	—	-0.7	—	mAdc
		10	-0.25	—	-0.2	-0.36	—	-0.14	—	
		15	-0.62	—	-0.5	-0.9	—	-0.35	—	
	Sink I _{OL}	5.0	0.64	—	0.51	0.88	—	0.36	—	mAdc
		10	1.6	—	1.3	2.25	—	0.9	—	
		15	4.2	—	3.4	8.8	—	2.4	—	
Input Current	I _{in}	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	μAdc
Input Capacitance	C _{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package) I _{nh} = PCA _{in} = V _{DD} . Zener = VCO _{in} = 0 V, PCB _{in} = V _{DD} . or 0 V, I _{out} = 0 μA	I _{DD}	5.0	—	5.0	—	0.005	5.0	—	150	μAdc
		10	—	10	—	0.010	10	—	300	
		15	—	20	—	0.015	20	—	600	
Total Supply Current† (I _{nh} = "0", f _o = 10 kHz, C _L = 50 pF, R1 = 1.0 MΩ, R2 = ∞, R _{SF} = ∞, and 50% Duty Cycle)	I _T	5.0	I _T = (1.46 μA/kHz) f + I _{DD}						μAdc	
		10	I _T = (2.91 μA/kHz) f + I _{DD}							
		15	I _T = (4.37 μA/kHz) f + I _{DD}							

#Noise immunity specified for worst-case input combination.

Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc

†To Calculate Total Current in General:

$$I_T \approx 2.2 \times V_{DD} \left(\frac{V_{COin} - 1.65}{R1} + \frac{V_{DD} - 1.35}{R2} \right)^{3/4} + 1.6 \times \left(\frac{V_{COin} - 1.65}{R_{SF}} \right)^{3/4} + 1 \times 10^{-3} (C_L + 9) V_{DD} f +$$

$$1 \times 10^{-1} V_{DD}^2 \left(\frac{100\% \text{ Duty Cycle of PCA}_{in}}{100} \right) + I_Q \quad \text{where: } I_T \text{ in } \mu\text{A}, C_L \text{ in pF, } V_{COin}, V_{DD} \text{ in Vdc, } f \text{ in kHz, and}$$

R1, R2, R_{SF} in MΩ, C_L on VCO_{out}.

MC14046B

ELECTRICAL CHARACTERISTICS* ($C_L = 50 \text{ pF}$, $T_A = 25^\circ\text{C}$)

Characteristic	Symbol	VDD Vdc	Minimum	Typical	Maximum	Units
			Device		Device	
Output Rise Time $t_{\text{TLH}} = (3.0 \text{ ns/pF}) C_L + 30 \text{ ns}$ $t_{\text{TLH}} = (1.5 \text{ ns/pF}) C_L + 15 \text{ ns}$ $t_{\text{TLH}} = (1.1 \text{ ns/pF}) C_L + 10 \text{ ns}$	t_{TLH}	5.0 10 15	— — —	180 90 65	350 150 110	ns
Output Fall Time $t_{\text{THL}} = (1.5 \text{ ns/pF}) C_L + 25 \text{ ns}$ $t_{\text{THL}} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$ $t_{\text{THL}} = (0.55 \text{ ns/pF}) C_L + 9.5 \text{ ns}$	t_{THL}	5.0 10 15	— — —	100 50 37	175 75 55	ns

PHASE COMPARATORS 1 and 2

Input Resistance — PCA_{in}	R_{in}	5.0	1.0	2.0	—	$\text{M}\Omega$
		10	0.2	0.4	—	
		15	0.1	0.2	—	
— PCB_{in}	R_{in}	15	150	1500	—	$\text{M}\Omega$
Minimum Input Sensitivity AC Coupled — PCA_{in} C series = 1000 pF, $f = 50 \text{ kHz}$	V_{in}	5.0	—	200	300	mV p-p
		10	—	400	600	
		15	—	700	1050	
DC Coupled — PCA_{in} , PCB_{in}	—	5 to 15	See Noise Immunity			

VOLTAGE CONTROLLED OSCILLATOR (VCO)

Maximum Frequency ($\text{VCO}_{\text{in}} = \text{V}_{\text{DD}}$, $C_1 = 50 \text{ pF}$ $R_1 = 5.0 \text{ k}\Omega$, and $R_2 = \infty$)	f_{max}	5.0	0.5	0.7	—	MHz
		10	1.0	1.4	—	
		15	1.4	1.9	—	
Temperature — Frequency Stability ($R_2 = \infty$)	—	5.0	—	0.12	—	%/°C
		10	—	0.04	—	
		15	—	0.015	—	
Linearity ($R_2 = \infty$) ($\text{VCO}_{\text{in}} = 2.5 \text{ V} \pm 0.3 \text{ V}$, $R_1 > 10 \text{ k}\Omega$) ($\text{VCO}_{\text{in}} = 5.0 \text{ V} \pm 2.5 \text{ V}$, $R_1 > 400 \text{ k}\Omega$) ($\text{VCO}_{\text{in}} = 7.5 \text{ V} \pm 5.0 \text{ V}$, $R_1 \geq 1000 \text{ k}\Omega$)	—	5.0	—	1.0	—	%
		10	—	1.0	—	
		15	—	1.0	—	
Output Duty Cycle	—	5 to 15	—	50	—	%
Input Resistance — VCO_{in}	R_{in}	15	150	1500	—	$\text{M}\Omega$

SOURCE-FOLLOWER

Offset Voltage (VCO_{in} minus SF_{out} , $R_{\text{SF}} > 500 \text{ k}\Omega$)	—	5.0	—	1.65	2.2	V
		10	—	1.65	2.2	
		15	—	1.65	2.2	
Linearity ($\text{VCO}_{\text{in}} = 2.5 \text{ V} \pm 0.3 \text{ V}$, $R_{\text{SF}} > 50 \text{ k}\Omega$) ($\text{VCO}_{\text{in}} = 5.0 \text{ V} \pm 2.5 \text{ V}$, $R_{\text{SF}} > 50 \text{ k}\Omega$) ($\text{VCO}_{\text{in}} = 7.5 \text{ V} \pm 5.0 \text{ V}$, $R_{\text{SF}} > 50 \text{ k}\Omega$)	—	5.0	—	0.1	—	%
		10	—	0.6	—	
		15	—	0.8	—	

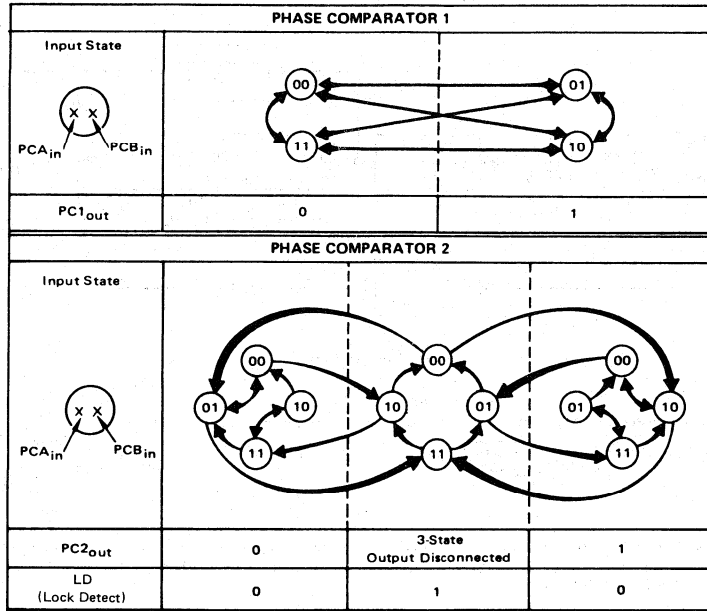
ZENER DIODE

Zener Voltage ($I_z = 50 \mu\text{A}$)	V_Z	—	6.7	7.0	7.3	V
Dynamic Resistance ($I_z = 1.0 \text{ mA}$)	R_Z	—	—	100	—	Ω

*The formula given is for the typical characteristics only.

MC14046B

FIGURE 1 – PHASE COMPARATORS STATE DIAGRAMS



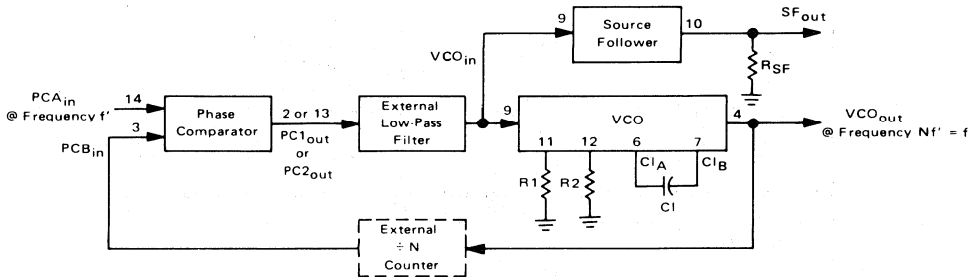
Refer to Waveforms in Figure 3.

FIGURE 2 – DESIGN INFORMATION

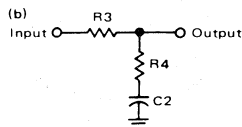
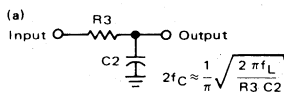
Characteristic	Using Phase Comparator 1	Using Phase Comparator 2
No signal on input PCA _{in} .	VCO in PLL system adjusts to center frequency (f _q).	VCO in PLL system adjusts to minimum frequency (f _{min}).
Phase angle between PCA _{in} and PCB _{in} .	90° at center frequency (f _q), approaching 0° and 180° at ends of lock range (2f _L).	Always 0° in lock (positive rising edges).
Locks on harmonics of center frequency.	Yes	No
Signal input noise rejection.	High	Low
Lock frequency range (2f _L).	The frequency range of the input signal on which the loop will stay locked if it was initially in lock. 2f _L = full VCO frequency range = f _{max} - f _{min} .	
Capture frequency range (2f _C).	The frequency range of the input signal on which the loop will lock if it was initially out of lock.	
	Depends on low-pass filter characteristics (see Figure 3). f _C < f _L	f _C = f _L
Center frequency (f _q).	The frequency of VCO _{out} when VCO _{in} = 1/2 VDD	
VCO output frequency (f).	$f_{min} = \frac{1}{R_2(C_1 + 32 \text{ pF})} \quad (\text{VCO input} = V_{SS})$ $f_{max} = \frac{1}{R_1(C_1 + 32 \text{ pF})} + f_{min} \quad (\text{VCO input} = V_{DD})$ <p>Note: These equations are intended to be a design guide. Since calculated component values may be in error by as much as a factor of 4, laboratory experimentation may be required for fixed designs. Part to part frequency variation with identical passive components is typically less than ±20%.</p> <p>Where: 10K < R₁ < 1M 10K < R₂ < 1M 100pF < C₁ < .01 μF</p>	

MC14046B

FIGURE 3 – GENERAL PHASE-LOCKED LOOP CONNECTIONS AND WAVEFORMS



Typical Low-Pass Filters



Typically:

$$R_4 C_2 = \frac{6N}{f_{\max}} - \frac{N}{2\pi \Delta f}$$

$$(R_3 + 3,000\Omega) C_2 = \frac{100N\Delta f}{f_{\max}^2} - R_4 C_2$$

$$\Delta f = f_{\max} - f_{\min}$$

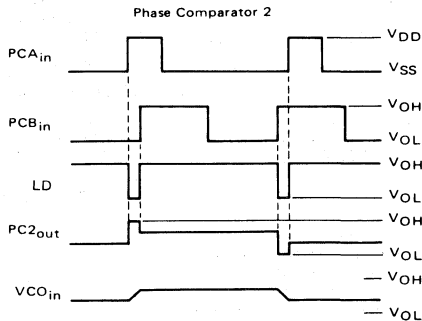
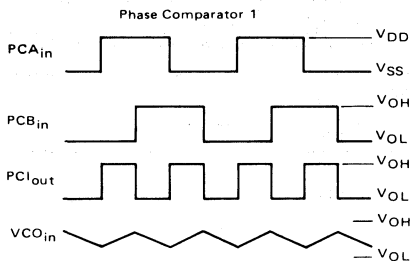
Note: Sometimes R_3 is split into two series resistors each $R_3 \div 2$. A capacitor C_C is then placed from the midpoint to ground. The value for C_C should be such that the corner frequency of this network does not significantly affect ω_n . In Figure B, the ratio of R_3 to R_4 sets the damping, $R_4 \cong (0.1)(R_3)$ for optimum results.

Definitions: N = Total division ratio in feedback loop
 $K_\phi = V_{DD}/\pi$ for Phase Comparator 1
 $K_\phi = V_{DD}/4\pi$ for Phase Comparator 2
 $K_{VCO} = \frac{2\pi \Delta f_{VCO}}{V_{DD} - 2V}$
 for a typical design $\omega_n \cong \frac{2\pi f_r}{10}$ (at phase detector input)
 $\zeta \cong 0.707$

LOW-PASS FILTER

Filter A	Filter B
$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NR_3 C_2}}$	$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NC_2(R_3 + R_4)}}$
$\zeta = \frac{N\omega_n}{2K_\phi K_{VCO}}$	$\zeta = 0.5 \omega_n (R_3 C_2 + \frac{N}{K_\phi K_{VCO}})$
$F(s) = \frac{1}{R_3 C_2 S + 1}$	$F(s) = \frac{R_3 C_2 S + 1}{S(R_3 C_2 + R_4 C_2) + 1}$

Waveforms



Note: for further information, see:

- (1) F. Gardner, "Phase-Lock Techniques", John Wiley and Son, New York, 1966.
- (2) G. S. Moschytz, "Miniature RC Filters Using Phase-Locked Loop", BSTJ, May, 1965.
- (3) Garth Nash, "Phase-Lock Loop Design Fundamentals", AN-535, Motorola Inc.
- (4) A. B. Przedpelski, "Phase-Locked Loop Design Articles", AR254, reprinted by Motorola Inc.



MOTOROLA

**MC14049B
MC14050B**

HEX BUFFER

The MC14049B Hex Inverter/Buffer and MC14050B Noninverting Hex Buffer are constructed with MOS P-Channel and N-Channel enhancement mode devices in a single monolithic structure. These complementary MOS devices find primary use where low power dissipation and/or high noise immunity is desired. These devices provide logic level conversion using only one supply voltage, V_{DD} .

The input-signal high level (V_{IH}) can exceed the V_{DD} supply voltage for logic level conversions. Two TTL/DTL loads can be driven when the devices are used as a CMOS-to-TTL/DTL converter ($V_{DD} = 5.0$ V, $V_{OL} \leq 0.4$ V, $I_{OL} \geq 3.2$ mA).

Note that pins 13 and 16 are not connected internally on these devices; consequently connections to these terminals will not affect circuit operation.

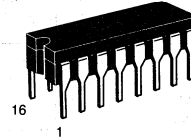
- High Source and Sink Currents
- High-to-Low Level Converter
- Supply Voltage Range = 3.0 V to 18 V
- V_{IH} can exceed V_{DD}
- Meets JEDEC B Specifications
- Improved ESD Protection On All Inputs

MAXIMUM RATINGS¹ (Voltages referenced to V_{SS})

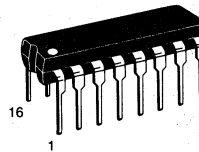
Characteristic	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage (DC or Transient)	V_{IN}	-0.5 to +18	Vdc
Output Voltage (DC or Transient)	V_{out}	-0.5 to $V_{DD} + 0.5$	Vdc
Input Current (DC or Transient), per pin	I_{in}	± 10	mA
Output Current (DC or Transient), per pin	I_{out}	+45	mA
Power Dissipation, per Package ² (Plastic/Ceramic) (SOIC)	P_D	825 740	mW
Storage Temperature	T_{stg}	-65 to +150	°C
Lead Temperature (8-Second Soldering)	T_L	260	°C

¹Maximum Ratings are those values beyond which damage to the device may occur.

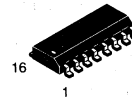
²Temperature Derating: See Figure 3.



**L SUFFIX
CERAMIC
CASE 620**



**P SUFFIX
PLASTIC
CASE 648**



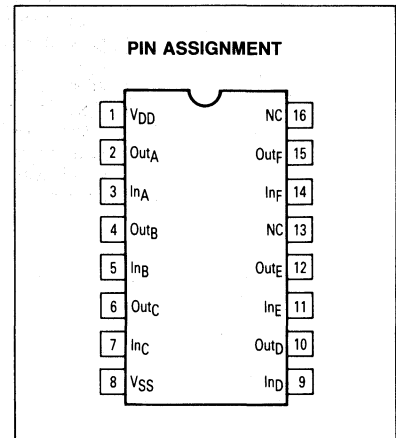
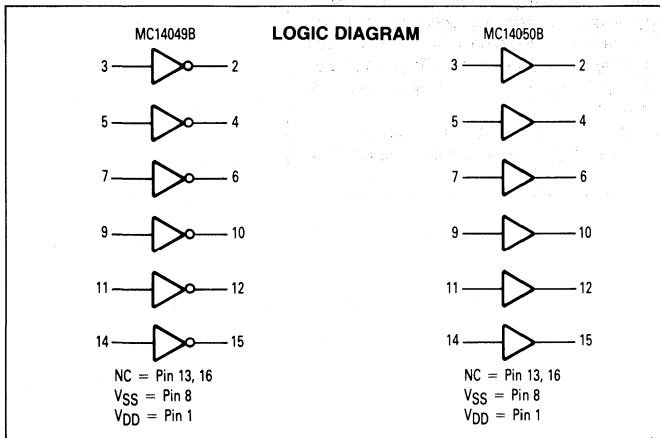
**D SUFFIX
SOIC
CASE 751B**

ORDERING INFORMATION

MC14XXXBCL Ceramic
MC14XXXBCP Plastic
MC14XXXBD SOIC

$T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$ for all packages

6



MC14049B • MC14050B

ELECTRICAL CHARACTERISTICS (Voltages referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	-55°C		+25°C			+125°C		Unit
			Min	Max	Min	Typ ¹	Max	Min	Max	
Output Voltage $V_{in} = V_{DD}$ $V_{in} = 0$	"0" Level V_{OL}	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
		10	—	0.05	—	0	0.05	—	0.05	
		15	—	0.05	—	0	0.05	—	0.05	
	"1" Level V_{OH}	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc
		10	9.95	—	9.95	10	—	9.95	—	
		15	14.95	—	14.95	15	—	14.95	—	
Input Voltage ($V_O = 4.5$ Vdc) ($V_O = 9.0$ Vdc) ($V_O = 13.5$ Vdc) ($V_O = 0.5$ Vdc) ($V_O = 1.0$ Vdc) ($V_O = 1.5$ Vdc)	"0" Level V_{IL}	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc
		10	—	3.0	—	4.50	3.0	—	3.0	
		15	—	4.0	—	6.75	4.0	—	4.0	
	"1" Level V_{IH}	5.0	3.5	—	3.5	2.75	—	3.5	—	Vdc
		10	7.0	—	7.0	5.50	—	7.0	—	
		15	11	—	11	8.25	—	11	—	
Output Drive Current ($V_{OH} = 2.5$ Vdc) ($V_{OH} = 9.5$ Vdc) ($V_{OH} = 13.5$ Vdc) ($V_{OL} = 0.4$ Vdc) ($V_{OL} = 0.5$ Vdc) ($V_{OL} = 1.5$ Vdc)	Source I_{OH}	5.0	-1.6	—	-1.25	-2.5	—	-1.0	—	mAdc
		10	-1.6	—	-1.30	-2.6	—	-1.0	—	
		15	-4.7	—	-3.75	-10	—	-3.0	—	
	Sink I_{OL}	5.0	3.75	—	3.2	6.0	—	2.6	—	mAdc
		10	10	—	8.0	16	—	6.6	—	
		15	30	—	24	40	—	19	—	
Input Current	I_{in}	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	μAdc
Input Capacitance ($V_{in} = 0$)	C_{in}	—	—	—	—	10	20	—	—	pF
Quiescent Current (Per Package)	I_{DD}	5.0	—	1.0	—	0.002	1.0	—	30	μAdc
		10	—	2.0	—	0.004	2.0	—	60	
		15	—	4.0	—	0.006	4.0	—	120	
Total Supply Current ^{2,3} (Dynamic plus Quiescent, per package) ($C_L = 50$ pF on all outputs, all buffers switching)	I_T	5.0	$I_T = (1.8 \mu A/kHz) f + I_{DD}$ $I_T = (3.5 \mu A/kHz) f + I_{DD}$ $I_T = (5.3 \mu A/kHz) f + I_{DD}$							μAdc
		10								
		15								

¹ Data labeled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

² The formulas given are for the typical characteristics only at +25°C

³ To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) V/k$$

Where: I_T is in μA (per Package), C_L in pF, $V = (V_{DD} - V_{SS})$ in volts, f in kHz is input frequency and $k = 0.002$.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields **referenced to the V_{SS} pin only**. Extra precautions must be taken to avoid applications of any voltage higher than the maximum rated voltages to this high-impedance circuit. For proper operation, the ranges $V_{SS} \leq V_{in} \leq 18$ V and $V_{SS} \leq V_{out} \leq V_{DD}$ are recommended.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

MC14049B • MC14050B

AC SWITCHING CHARACTERISTICS¹ ($C_L = 50$ pF, $T_A = +25^\circ\text{C}$)

Characteristic	Symbol	V _{DD} Vdc	Min	Typ ²	Max	Unit
Output Rise Time $t_{TLH} = (0.7 \text{ ns/pF}) C_L + 65 \text{ ns}$ $t_{TLH} = (0.25 \text{ ns/pF}) C_L + 37.5 \text{ ns}$ $t_{TLH} = (0.2 \text{ ns/pF}) C_L + 30 \text{ ns}$	t_{TLH}	5.0 10 15	— — —	100 50 40	160 80 60	ns
Output Fall Time $t_{THL} = (0.2 \text{ ns/pF}) C_L + 30 \text{ ns}$ $t_{THL} = (0.06 \text{ ns/pF}) C_L + 17 \text{ ns}$ $t_{THL} = (0.04 \text{ ns/pF}) C_L + 13 \text{ ns}$	t_{THL}	5.0 10 15	— — —	40 20 15	60 40 30	ns
Propagation Delay Time $t_{PLH} = (0.33 \text{ ns/pF}) C_L + 63.5 \text{ ns}$ $t_{PLH} = (0.19 \text{ ns/pF}) C_L + 30.5 \text{ ns}$ $t_{PLH} = (0.06 \text{ ns/pF}) C_L + 27 \text{ ns}$	t_{PLH}	5.0 10 15	— — —	80 40 30	140 80 60	ns
Propagation Delay Time $t_{PHL} = (0.2 \text{ ns/pF}) C_L + 30 \text{ ns}$ $t_{PHL} = (0.1 \text{ ns/pF}) C_L + 15 \text{ ns}$ $t_{PHL} = (0.05 \text{ ns/pF}) C_L + 12.5 \text{ ns}$	t_{PHL}	5.0 10 15	— — —	40 20 15	80 40 30	ns

¹ The formulas given are for the typical characteristics only at 25°C.

² Data labeled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

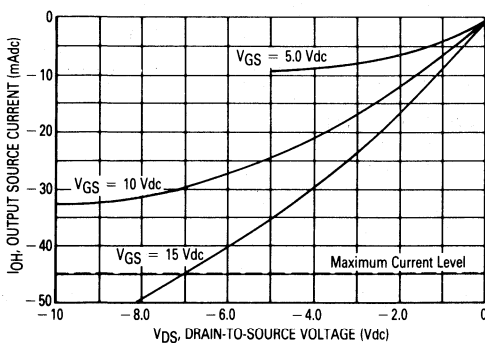
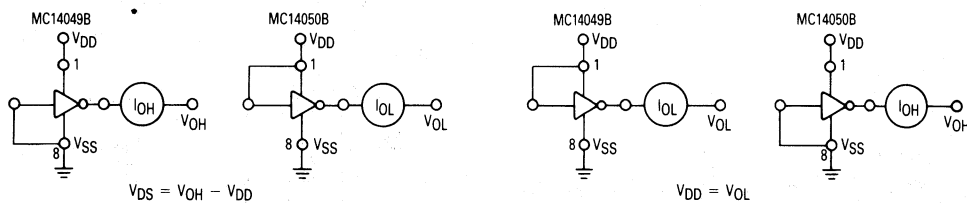


FIGURE 1 — TYPICAL OUTPUT SOURCE CHARACTERISTICS

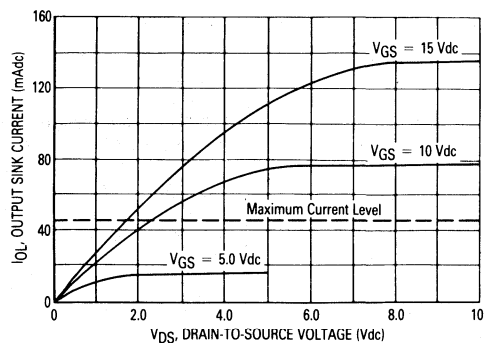


FIGURE 2 — TYPICAL OUTPUT SINK CHARACTERISTICS

MC14049B • MC14050B

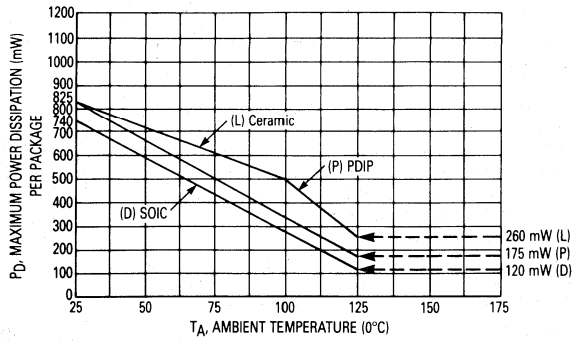


FIGURE 3 — AMBIENT TEMPERATURE POWER DERATING

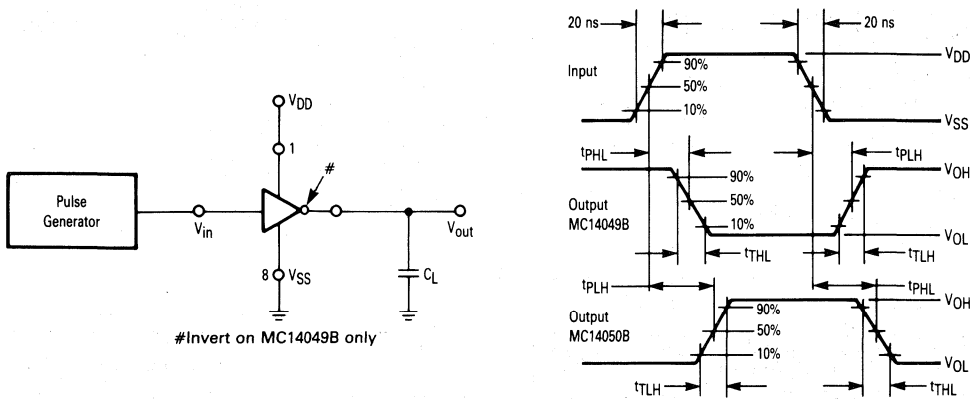


FIGURE 4 — SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



MOTOROLA

MC14049UB

HEX BUFFERS

The MC14049UB hex inverter/buffer is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. This complementary MOS device finds primary use where low power dissipation and/or high noise immunity is desired. This device provides logic-level conversion using only one supply voltage, V_{DD} . The input-signal high level (V_{IH}) can exceed the V_{DD} supply voltage for logic-level conversions. Two TTL/DTL Loads can be driven when the device is used as CMOS-to-TTL/DTL converters ($V_{DD} = 5.0\text{ V}$, $V_{OL} \leq 0.4\text{ V}$, $I_{OL} \geq 3.2\text{ mA}$). Note that pins 13 and 16 are not connected internally on this device; consequently connections to these terminals will not affect circuit operation.

- High Source and Sink Currents
- High-to-Low Level Converter
- Supply Voltage Range = 3.0 V to 18 V
- Meets JEDEC UB Specifications
- V_{IH} can exceed V_{DD}
- Improved ESD Protection on All Inputs

MAXIMUM RATINGS* (Voltages referenced to V_{SS})

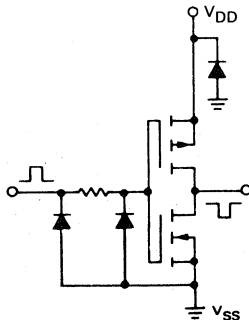
Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	V
Input Voltage (DC or Transient)	V_{IH}	-0.5 to +18	V
Output Voltage (DC or Transient)	V_{out}	-0.5 to $V_{DD} + 0.5$	V
Input Current (DC or Transient), per Pin	I_{in}	± 10	mA
Output Current (DC or Transient), per Pin	I_{out}	+45	mA
Power Dissipation, per Package† Plastic/Ceramic SOIC	P_D	825	mW
		740	
Storage Temperature	T_{stg}	-65 to +150	°C
Lead Temperature (8-Second Soldering)	T_L	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.

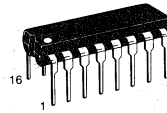
† Temperature Derating: All Packages: See Figure 4.

CIRCUIT SCHEMATIC (1/6 OF CIRCUIT SHOWN)

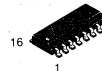
MC14049UB



L SUFFIX
CERAMIC
CASE 620



P SUFFIX
PLASTIC
CASE 648



D SUFFIX
SOIC
CASE 751B

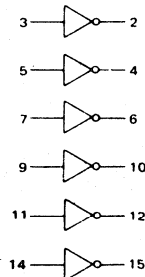
ORDERING INFORMATION

MC14XXXBCP Plastic
MC14XXXBCL Ceramic
MC14XXXBD SOIC

$T_A = -55^\circ$ to 125°C for all packages.

LOGIC DIAGRAM

MC14049UB



NC = Pin 13, 16
 V_{SS} = Pin 8
 V_{DD} = Pin 1

MC14049UB

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V _{DD} Vdc	-55°C		25°C			125°C		Unit
			Min	Max	Min	Typ	Max	Min	Max	
Output Voltage V _{in} = V _{DD} or 0	V _{OL}	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
		10	—	0.05	—	0	0.05	—	0.05	
V _{in} = 0 or V _{DD}	V _{OH}	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc
		10	9.95	—	9.95	10	—	9.95	—	
Input Voltage (V _O = 4.5 Vdc) (V _O = 9.0 Vdc) (V _O = 13.5 Vdc)	V _{IL}	5.0	—	1.0	—	2.25	1.0	—	1.0	Vdc
		10	—	2.0	—	4.50	2.0	—	2.0	
(V _O = 0.5 Vdc) (V _O = 1.0 Vdc) (V _O = 1.5 Vdc)	V _{IH}	5.0	4.0	—	4.0	2.75	—	4.0	—	Vdc
		10	8.0	—	8.0	5.50	—	8.0	—	
Output Drive Current (V _{OH} = 2.5 Vdc) (V _{OH} = 9.5 Vdc) (V _{OH} = 13.5 Vdc)	Source I _{OH}	5.0	-1.6	—	-1.25	-2.5	—	-1.0	—	mAdc
		10	-1.6	—	-1.3	-2.6	—	-1.0	—	
(V _{OL} = 0.4 Vdc) (V _{OL} = 0.5 Vdc) (V _{OL} = 1.5 Vdc)	Sink I _{OL}	5.0	3.75	—	3.2	6.0	—	2.6	—	mAdc
		10	10	—	8.0	16	—	6.6	—	
		15	30	—	24	40	—	19	—	
Input Current	I _{in}	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	μAdc
Input Capacitance (V _{in} = 0)	C _{in}	—	—	—	—	10	20	—	—	pF
Quiescent Current (Per Package)	I _{DD}	5.0	—	1.0	—	0.002	1.0	—	30	μAdc
		10	—	2.0	—	0.004	2.0	—	60	
		15	—	4.0	—	0.006	4.0	—	120	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C _L = 50 pF on all outputs, all buffers switching)	I _T	5.0	I _T = (1.8 μA/kHz) f + I _{DD}							μAdc
10	I _T = (3.5 μA/kHz) f + I _{DD}									
15	I _T = (5.3 μA/kHz) f + I _{DD}									

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) Vfk$$

where: I_T is in μA (per package), C_L in pF, V = (V_{DD} - V_{SS}) in volts, f in kHz is input frequency, and k = 0.002.

MC14049UB

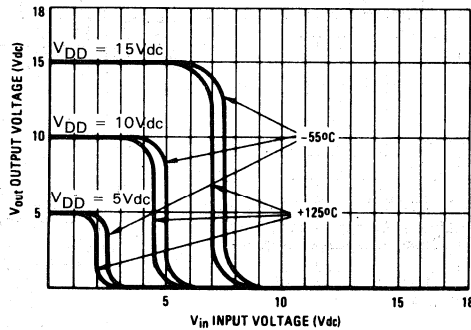
SWITCHING CHARACTERISTICS* ($C_L = 50 \text{ pF}$, $T_A = 25^\circ\text{C}$)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ #	Max	Unit
Output Rise Time $t_{TLH} = (0.8 \text{ ns/pF}) C_L + 60 \text{ ns}$ $t_{TLH} = (0.3 \text{ ns/pF}) C_L + 35 \text{ ns}$ $t_{TLH} = (0.27 \text{ ns/pF}) C_L + 26.5 \text{ ns}$	t_{TLH}	5.0 10 15	— — —	100 50 40	160 100 60	ns
Output Fall Time $t_{THL} = (0.3 \text{ ns/pF}) C_L + 25 \text{ ns}$ $t_{THL} = (0.12 \text{ ns/pF}) C_L + 14 \text{ ns}$ $t_{THL} = (0.1 \text{ ns/pF}) C_L + 10 \text{ ns}$	t_{THL}	5.0 10 15	— — —	40 20 15	60 40 30	ns
Propagation Delay Time $t_{PLH} = (0.38 \text{ ns/pF}) C_L + 61 \text{ ns}$ $t_{PLH} = (0.20 \text{ ns/pF}) C_L + 30 \text{ ns}$ $t_{PLH} = (0.11 \text{ ns/pF}) C_L + 24.5 \text{ ns}$	t_{PLH}	5.0 10 15	— — —	80 40 30	120 65 50	ns
Propagation Delay Time $t_{PHL} = (0.38 \text{ ns/pF}) C_L + 11 \text{ ns}$ $t_{PHL} = (0.12 \text{ ns/pF}) C_L + 9 \text{ ns}$ $t_{PHL} = (0.11 \text{ ns/pF}) C_L + 4.5 \text{ ns}$	t_{PHL}	5.0 10 15	— — —	30 15 10	60 30 20	ns

*The formulas given are for the typical characteristics only at 25°C .

#Data labeled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

FIGURE 1 – TYPICAL VOLTAGE TRANSFER CHARACTERISTICS versus TEMPERATURE



MC14049UB

FIGURE 2 – TYPICAL OUTPUT SOURCE CHARACTERISTICS

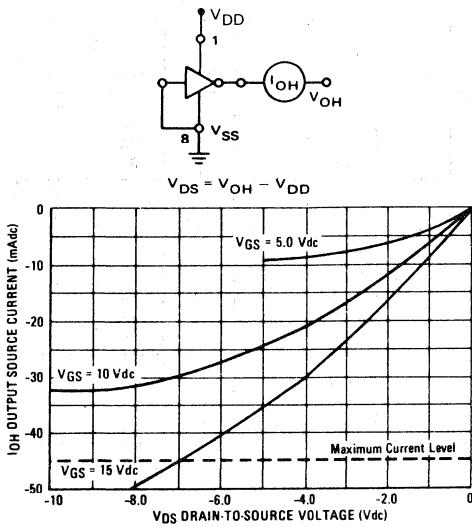
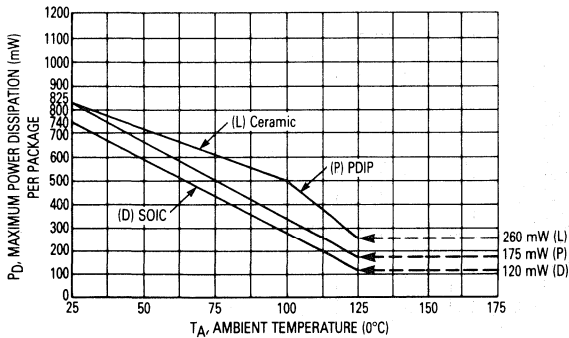


FIGURE 4 – AMBIENT TEMPERATURE POWER DERATING



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields **referenced to the VSS pin, only**. Extra precautions must be taken to avoid applications of any voltage higher than the maximum rated voltages to this high-impedance circuit. For proper operation, the ranges $V_{SS} \leq V_{in} \leq 18\text{ V}$ and $V_{SS} \leq V_{out} \leq V_{DD}$ are recommended.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either VSS or VDD). Unused outputs must be left open.

FIGURE 3 – TYPICAL OUTPUT SINK CHARACTERISTICS

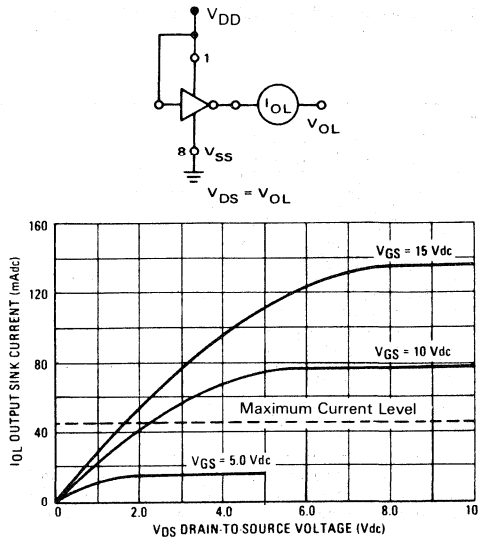
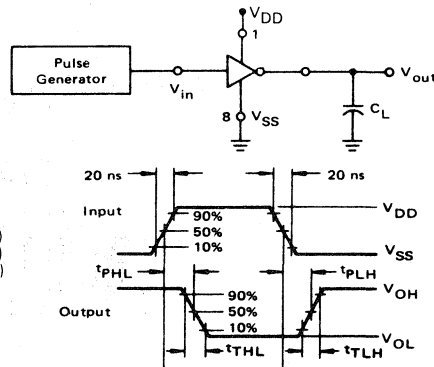


FIGURE 5 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



PIN ASSIGNMENT

1	VDD	NC	16
2	Out _A	Out _F	15
3	In _A	In _F	14
4	Out _B	NC	13
5	In _B	Out _E	12
6	Out _C	In _E	11
7	In _C	Out _D	10
8	VSS	In _D	9

NC = No Connection

6



MOTOROLA

**MC14051B
MC14052B
MC14053B**

ANALOG MULTIPLEXERS/DEMULTIPLEXERS

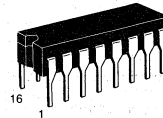
The MC14051B, MC14052B, and MC14053B analog multiplexers are digitally-controlled analog switches. The MC14051B effectively implements an SP8T solid state switch, the MC14052B a DP4T, and the MC14053B a Triple SPDT. All three devices feature low ON impedance and very low OFF leakage current. Control of analog signals up to the complete supply voltage range can be achieved.

- Triple Diode Protection on Control Inputs
- Switch Function is Break Before Make
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Analog Voltage Range ($V_{DD} - V_{EE}$) = 3.0 to 18 V
Note: V_{EE} must be $\leq V_{SS}$
- Linearized Transfer Characteristics
- Low-noise — 12 nV/ $\sqrt{\text{Cycle}}$, $f \geq 1.0$ kHz Typical
- Pin-for-Pin Replacement for CD4051, CD4052, and CD4053
- For 4PDT Switch, See MC14551B
- For Lower R_{ON} , Use the HC4051, HC4052, or HC4053 High-Speed CMOS Devices

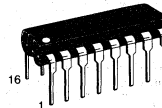
MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage (Referenced to V_{EE} , $V_{SS} \geq V_{EE}$)	-0.5 to +18.0	V
V_{in} , V_{out}	Input or Output Voltage (DC or Transient) (Referenced to V_{SS} for Control Inputs and V_{EE} for Switch I/O)	-0.5 to $V_{DD} + 0.5$	V
I_{in}	Input Current (DC or Transient), per Control Pin	± 10	mA
I_{sw}	Switch Through Current	± 25	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

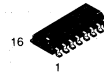
*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P and D/DW" Packages: -7.0 mW/°C From 65°C To 125°C
Ceramic "L" Packages: -12 mW/°C From 100°C To 125°C



**L SUFFIX
CERAMIC
CASE 620**



**P SUFFIX
PLASTIC
CASE 648**



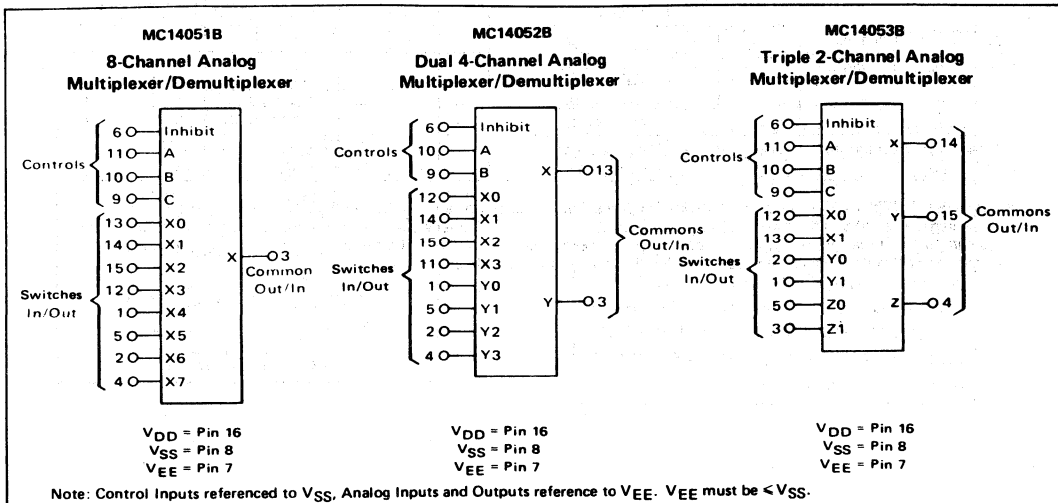
**D SUFFIX
SOIC
CASE 751B**

ORDERING INFORMATION

- MC14XXXBCP Plastic
- MC14XXXBCL Ceramic
- MC14XXXBD SOIC

$T_A = -55^\circ\text{C}$ to 125°C for all packages.

6



MC14051B•MC14052B•MC14053B

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V _{DD}	Test Conditions	-55°C		25°C			125°C		Unit
				Min	Max	Min	Typ #	Max	Min	Max	

SUPPLY REQUIREMENTS (Voltages Referenced to V_{EE})

Power Supply Voltage Range	V _{DD}	—	V _{DD} - 3.0 ≥ V _{SS} ≥ V _{EE}	3.0	18	3.0	—	18	3.0	18	V
Quiescent Current Per Package	I _{DD}	5.0 10 15	Control Inputs: V _{in} = V _{SS} or V _{DD} , Switch I/O: V _{EE} ≤ V _{I/O} ≤ V _{DD} , and ΔV _{switch} ≤ 500 mV**	—	5.0 10 20	—	0.005 0.010 0.015	5.0 10 20	—	150 300 600	μA
Total Supply Current (Dynamic Plus Quiescent, Per Package)	I _{D(AV)}	5.0 10 15	T _A = 25°C only (The channel component, (V _{in} - V _{out})/R _{on} , is not included.)	Typical			(0.07 μA/kHz)f + I _{DD} (0.20 μA/kHz)f + I _{DD} (0.36 μA/kHz)f + I _{DD}				μA

CONTROL INPUTS — INHIBIT, A, B, C (Voltages Referenced to V_{SS})

Low-Level Input Voltage	V _{IL}	5.0 10 15	R _{on} = per spec, I _{off} = per spec	— — —	1.5 3.0 4.0	— — —	2.25 4.50 6.75	1.5 3.0 4.0	— — —	1.5 3.0 4.0	V
High-Level Input Voltage	V _{IH}	5.0 10 15	R _{on} = per spec, I _{off} = per spec	3.5 7.0 11	— — —	3.5 7.0 11	2.75 5.50 8.25	— — —	3.5 7.0 11	— — —	V
Input Leakage Current	I _{in}	15	V _{in} = 0 or V _{DD}	—	±0.1	—	±0.00001	±0.1	—	±1.0	μA
Input Capacitance	C _{in}	—		—	—	—	5.0	7.5	—	—	pF

SWITCHES IN/OUT AND COMMONS OUT/IN — X, Y, Z (Voltages Referenced to V_{EE})

Recommended Peak-to-Peak Voltage Into or Out of the Switch	V _{I/O}	—	Channel On or Off	0	V _{DD}	0	—	V _{DD}	0	V _{DD}	V _{PP}
Recommended Static or Dynamic Voltage Across the Switch** (Figure 5)	ΔV _{switch}	—	Channel On	0	600	0	—	600	0	300	mV
Output Offset Voltage	V _{OO}	—	V _{in} = 0 V, No Load	—	—	—	10	—	—	—	μV
ON Resistance	R _{on}	5.0 10 15	ΔV _{switch} ≤ 500 mV**, V _{in} = V _{IL} or V _{IH} (Control), and V _{in} = 0 to V _{DD} (Switch)	— — —	800 400 220	— — —	250 120 80	1050 500 280	— — —	1200 520 300	Ω
ΔON Resistance Between Any Two Channels in the Same Package	ΔR _{on}	5.0 10 15		— — —	70 50 45	— — —	25 10 10	70 50 45	— — —	135 95 65	Ω
Off-Channel Leakage Current (Figure 10)	I _{off}	15	V _{in} = V _{IL} or V _{IH} (Control) Channel to Channel or Any One Channel	—	±100	—	±0.05	±100	—	±1000	nA
Capacitance, Switch I/O	C _{I/O}	—	Inhibit = V _{DD}	—	—	—	10	—	—	—	pF
Capacitance, Common O/I	C _{O/I}	—	Inhibit = V _{DD} (MC14051B) (MC14052B) (MC14053B)	— — —	— — —	— — —	60 32 17	— — —	— — —	— — —	pF
Capacitance, Feedthrough (Channel Off)	C _{I/O}	—	Pins Not Adjacent Pins Adjacent	— —	— —	— —	0.15 0.47	— —	— —	— —	pF

#Data labeled "Typ" is not to be used for design purposes, but is intended as an indication of the IC's potential performance.

**For voltage drops across the switch (ΔV_{switch}) > 600 mV (> 300 mV at high temperature), excessive V_{DD} current may be drawn; i.e. the current out of the switch may contain both V_{DD} and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded. (See first page of this data sheet.)

MC14051B•MC14052B•MC14053B

ELECTRICAL CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C) (V_{EE} ≤ V_{SS} unless otherwise indicated)

Characteristic	Symbol	V _{DD} -V _{EE} V _{dC}	Typ # All Types	Max	Unit				
Propagation Delay Times (Figure 6) Switch Input to Switch Output (R _L = 10 kΩ)	t _{PLH} , t _{PHL} t _{PHZ} , t _{PLZ} , t _{PZH} , t _{PZL}	5.0 10 15	35 15 12	90 40 30	ns				
MC14051 t _{PLH} , t _{PHL} = (0.17 ns/pF) C _L + 26.5 ns t _{PLH} , t _{PHL} = (0.08 ns/pF) C _L + 11 ns t _{PLH} , t _{PHL} = (0.06 ns/pF) C _L + 9.0 ns									
MC14052 t _{PLH} , t _{PHL} = (0.17 ns/pF) C _L + 21.5 ns t _{PLH} , t _{PHL} = (0.08 ns/pF) C _L + 8.0 ns t _{PLH} , t _{PHL} = (0.06 ns/pF) C _L + 7.0 ns									
MC14053 t _{PLH} , t _{PHL} = (0.17 ns/pF) C _L + 16.5 ns t _{PLH} , t _{PHL} = (0.08 ns/pF) C _L + 4.0 ns t _{PLH} , t _{PHL} = (0.06 ns/pF) C _L + 3.0 ns									
Inhibit to Output (R _L = 10 kΩ, V _{EE} = V _{SS}) Output "1" or "0" to High Impedance, or High Impedance to "1" or "0" Level						5.0 10 15	350 170 140	700 340 280	ns
MC14051B									
MC14052B									
MC14053B									
Control Input to Output (R _L = 10 kΩ, V _{EE} = V _{SS})									
MC14051B									
MC14052B									
MC14053B									
MC14051B		5.0 10 15	360 160 120	720 320 240	ns				
MC14052B									
MC14053B									
MC14051B	5.0 10 15	325 130 90	650 260 180	ns					
MC14052B									
MC14053B									
Second Harmonic Distortion (R _L = 10KΩ, f = 1kHz) V _{in} = 5 V _{pp}	—	10	0.07	—	%				
Bandwidth (Figure 7) (R _L = 1 kΩ, V _{in} = 1/2 (V _{DD} -V _{EE}) p-p, C _L = 50pF 20 Log $\frac{V_{out}}{V_{in}}$ = -3 dB)	BW	10	17	—	MHz				
Off Channel Feedthrough Attenuation (Figure 7) R _L = 1KΩ, V _{in} = 1/2 (V _{DD} - V _{EE}) p-p f _{in} = 4.5 MHz — MC14051B f _{in} = 30 MHz — MC14052B f _{in} = 55 MHz — MC14053B	—	10	-50	—	dB				
Channel Separation (Figure 8) (R _L = 1 kΩ, V _{in} = 1/2 (V _{DD} -V _{EE}) p-p, f _{in} = 3.0 MHz	—	10	-50	—	dB				
Crosstalk, Control Input to Common O/I (Figure 9) (R ₁ = 1 kΩ, R _L = 10 kΩ Control t _{TLH} = t _{THL} = 20 ns, Inhibit = V _{SS})	—	10	75	—	mV				

*The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range V_{SS} ≤ (V_{in} or V_{out}) ≤ V_{DD}. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS}, V_{EE}, or V_{DD}). Unused outputs must be left open.

MC14051B • MC14052B • MC14053B

FIGURE 1 – SWITCH CIRCUIT SCHEMATIC

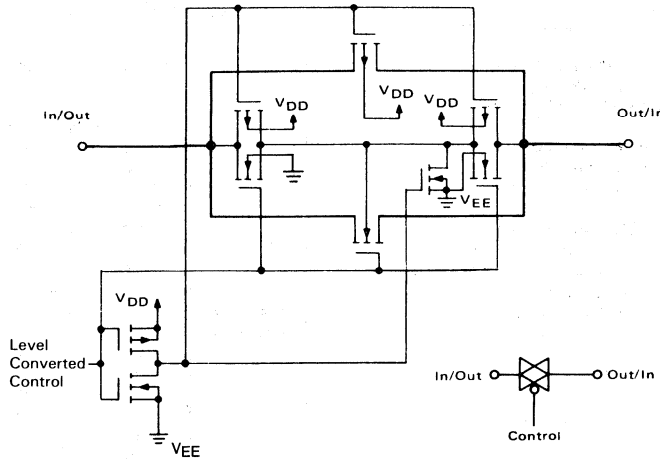
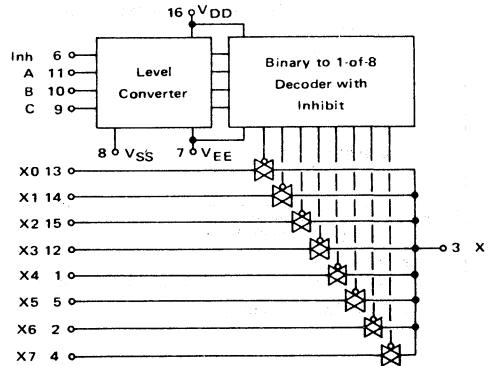


FIGURE 2 – MC14051B FUNCTIONAL DIAGRAM



TRUTH TABLE

Control Inputs			ON Switches						
Inhibit	Select			MC14051B		MC14052B		MC14053B	
	C*	B	A						
0	0	0	0	X0	Y0	X0	Z0	Y0	X0
0	0	0	1	X1	Y1	X1	Z0	Y0	X1
0	0	1	0	X2	Y2	X2	Z0	Y1	X0
0	0	1	1	X3	Y3	X3	Z0	Y1	X1
0	1	0	0	X4			Z1	Y0	X0
0	1	0	1	X5			Z1	Y0	X1
0	1	1	0	X6			Z1	Y1	X0
0	1	1	1	X7			Z1	Y1	X1
1	x	x	x	None	None	None			

*Not applicable for MC14052
x = Don't Care

FIGURE 3 – MC14052B FUNCTIONAL DIAGRAM

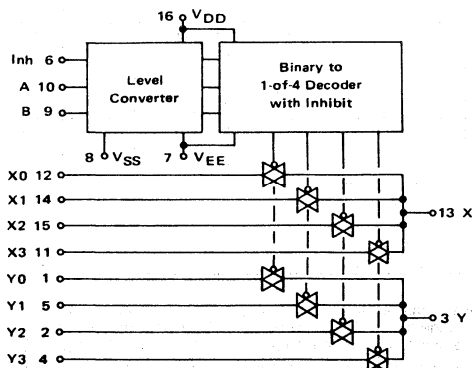
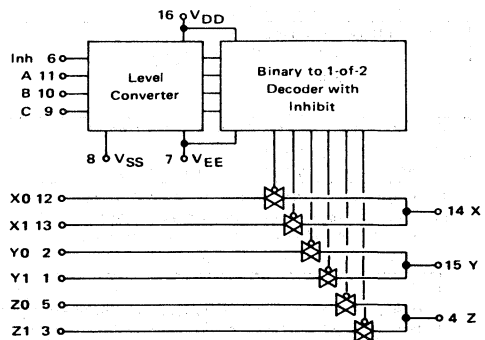


FIGURE 4 – MC14053B FUNCTIONAL DIAGRAM



MC14051B • MC14052B • MC14053B

TEST CIRCUITS

FIGURE 5 — ΔV ACROSS SWITCH

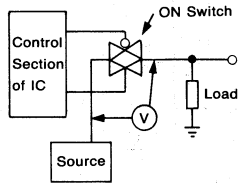


FIGURE 6 — PROPAGATION DELAY TIMES, CONTROL AND INHIBIT TO OUTPUT

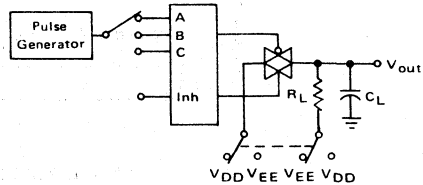


FIGURE 7 — BANDWIDTH AND OFF-CHANNEL FEEDTHROUGH ATTENUATION

A, B, and C inputs used to turn ON or OFF the switch under test.

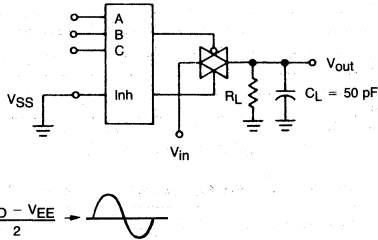


FIGURE 8 — CHANNEL SEPARATION (ADJACENT CHANNELS USED FOR SETUP)

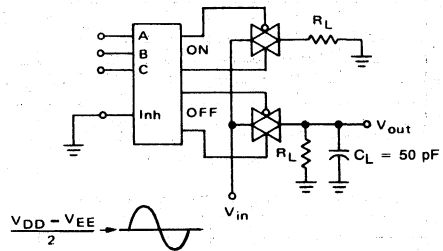


FIGURE 9 — CROSSTALK, CONTROL INPUT TO COMMON O/I

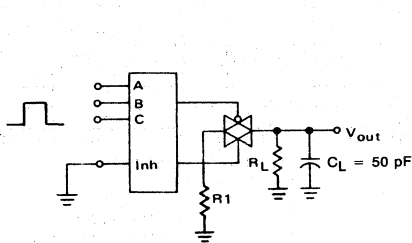
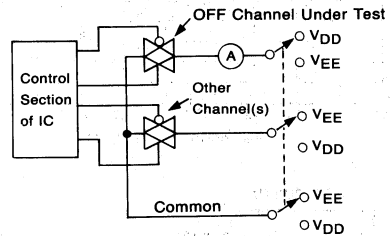


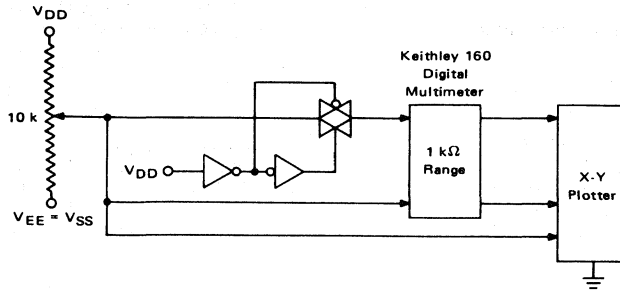
FIGURE 10 — OFF CHANNEL LEAKAGE



NOTE: See also Figures 7 and 8 on Page 6-51.

MC14051B • MC14052B • MC14053B

FIGURE 11 – CHANNEL RESISTANCE (R_{ON}) TEST CIRCUIT



TYPICAL RESISTANCE CHARACTERISTICS

FIGURE 12 – $V_{DD} = 7.5\text{ V}$, $V_{EE} = -7.5\text{ V}$

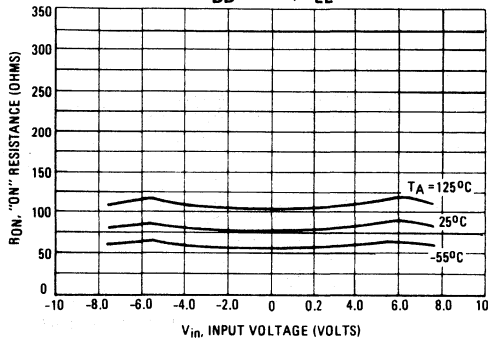


FIGURE 13 – $V_{DD} = 5.0\text{ V}$, $V_{EE} = -5.0\text{ V}$

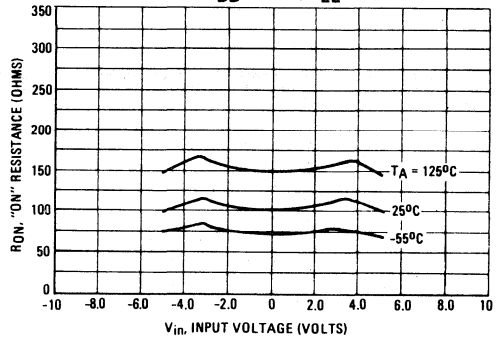


FIGURE 14 – $V_{DD} = 2.5\text{ V}$, $V_{EE} = -2.5\text{ V}$

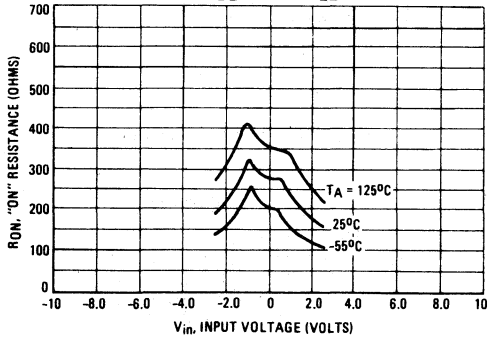
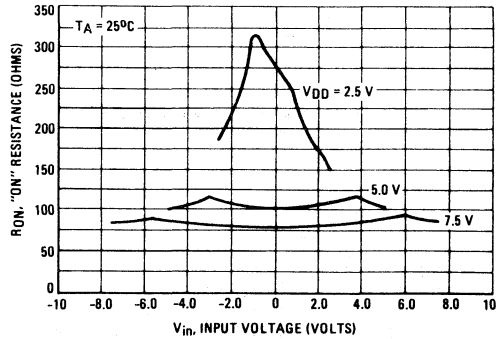


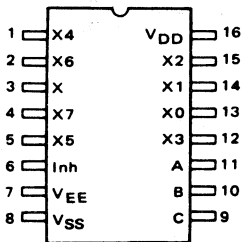
FIGURE 15 – COMPARISON AT 25°C, $V_{DD} = -V_{EE}$



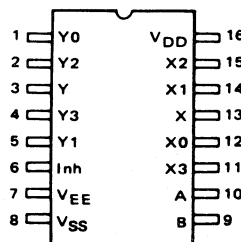
6

PIN ASSIGNMENT

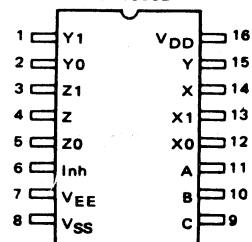
MC14051B



MC14052B



MC14053B



MC14051B•MC14052B•MC14053B

APPLICATIONS INFORMATION

Figure A illustrates use of the on-chip level converter detailed in Figures 2, 3, and 4. The 0-to-5 V Digital Control signal is used to directly control a 9 V_{p-p} analog signal.

The digital control logic levels are determined by V_{DD} and V_{SS}. The V_{DD} voltage is the logic high voltage; the V_{SS} voltage is logic low. For the example, V_{DD} = +5 V = logic high at the control inputs; V_{SS} = GND = 0 V = logic low.

The maximum analog signal level is determined by V_{DD} and V_{EE}. The V_{DD} voltage determines the maximum recommended peak above V_{SS}. The V_{EE} voltage determines the maximum swing below V_{SS}. For the example, V_{DD} - V_{SS} = 5 V maximum swing above V_{SS}; V_{SS} - V_{EE} = 5 V maximum swing below V_{SS}. The example shows a ± 4.5 V

signal which allows a ½ volt margin at each peak. If voltage transients above V_{DD} and/or below V_{EE} are anticipated on the analog channels, external diodes (D_X) are recommended as shown in Figure B. These diodes should be small signal types able to absorb the maximum anticipated current surges during clipping.

The *absolute* maximum potential difference between V_{DD} and V_{EE} is 18.0 V. Most parameters are specified up to 15 V which is the *recommended* maximum difference between V_{DD} and V_{EE}.

Balanced supplies are not required. However, V_{SS} must be greater than or equal to V_{EE}. For example, V_{DD} = +10 V, V_{SS} = +5 V, and V_{EE} = -3 V is acceptable. See the Table below.

FIGURE A — APPLICATION EXAMPLE

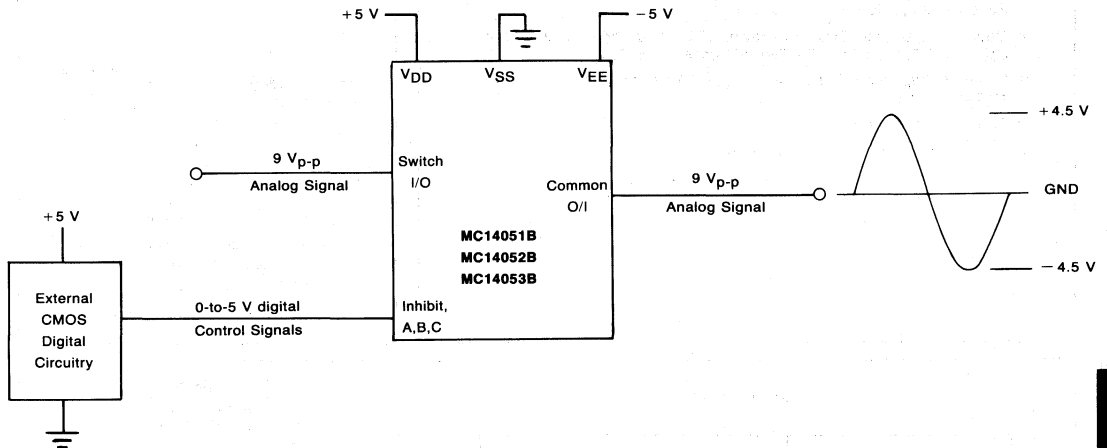
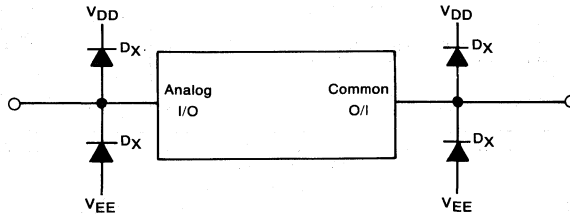


FIGURE B — EXTERNAL GERMANIUM OR SCHOTTKY CLIPPING DIODES



POSSIBLE SUPPLY CONNECTIONS

V _{DD} In Volts	V _{SS} In Volts	V _{EE} In Volts	Control Inputs Logic High/Logic Low In Volts	Maximum Analog Signal Range In Volts
+8	0	-8	+8/0	+8 to -8 = 16 V _{p-p}
+5	0	-12	+5/0	+5 to -12 = 17 V _{p-p}
+5	0	0	+5/0	+5 to 0 = 5 V _{p-p}
+5	0	-5	+5/0	+5 to -5 = 10 V _{p-p}
+10	+5	-5	+10/+5	+10 to -5 = 15 V _{p-p}

MC14060B

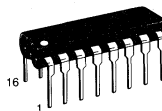
14-BIT BINARY COUNTER AND OSCILLATOR

The MC14060B is a 14-stage binary ripple counter with an on-chip oscillator buffer. The oscillator configuration allows design of either RC or crystal oscillator circuits. Also included on the chip is a reset function which places all outputs into the zero state and disables the oscillator. A negative transition on Clock will advance the counter to the next state. Schmitt trigger action on the input line permits very slow input rise and fall times. Applications include time delay circuits, counter controls, and frequency dividing circuits.

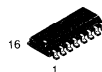
- Fully static operation
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 V to 18 V
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range
- Buffered Outputs Available from Stages 4 Through 10 and 12 Through 14
- Common Reset Line
- Pin-for-Pin Replacement for CD4060B



L SUFFIX
CERAMIC
CASE 620



P SUFFIX
PLASTIC
CASE 648





D SUFFIX
SOIC
CASE 751B

ORDERING INFORMATION

MC14XXXBCP Plastic
MC14XXXBCL Ceramic
MC14XXXBD SOIC

T_A = -55° to 125°C for all packages.

TRUTH TABLE

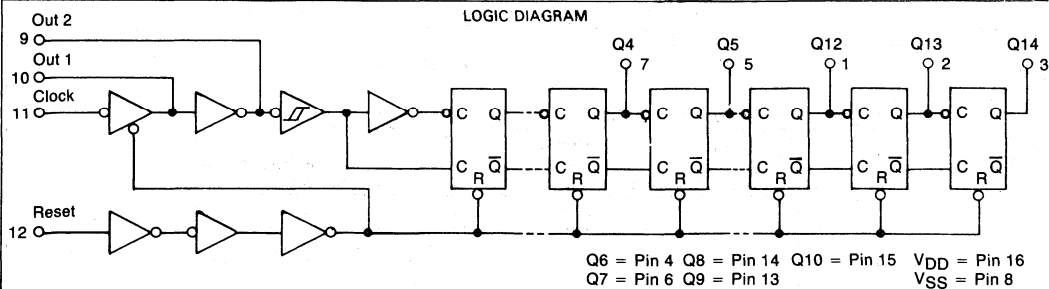
Clock	RESET	Output State
	L	No Change
	L	Advance to next state
X	H	All Outputs are low

X = Don't Care

PIN ASSIGNMENT

Q12	1	16	V _{DD}
Q13	2	15	Q10
Q14	3	14	Q8
Q6	4	13	Q9
Q5	5	12	Reset
Q7	6	11	Clock
Q4	7	10	Out 1
VSS	8	9	Out 2

LOGIC DIAGRAM



MC14060B

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V _{DD}	DC Supply Voltage	-0.5 to +18.0	V
V _{in} , V _{out}	Input or Output Voltage (DC or Transient)	-0.5 to V _{DD} + 0.5	V
I _{in} , I _{out}	Input or Output Current (DC or Transient), per Pin	± 10	mA
P _D	Power Dissipation, per Package†	500	mW
T _{stg}	Storage Temperature	-65 to +150	°C
T _L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.

†Temperature Derating: Plastic "P and D/DW" Packages: -7.0 mW/°C From 65°C To 125°C

Ceramic "L" Packages: -12 mW/°C From 100°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range V_{SS} ≤ (V_{in} or V_{out}) ≤ V_{DD}. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V _{DD} V	-55°C		25°C			125°C		Unit	
			Min	Max	M _{in}	Typ #	Max	Min	Max		
Output Voltage V _{in} = V _{DD} or 0 V _{in} = 0 or V _{DD}	V _{OL}	5.0	—	0.05	—	0	0.05	—	0.05	V	
		10	—	0.05	—	0	0.05	—	0.05		
	V _{OH}	5.0	4.95	—	4.95	5.0	—	4.95	—	V	
		10	9.95	—	9.95	10	—	9.95	—		
Input Voltage (V _O = 4.5 or 0.5 V) (V _O = 9.0 or 1.0 V) (V _O = 13.5 or 1.5 V)	V _{IL}	5.0	—	1.5	—	2.25	1.5	—	1.5	V	
		10	—	3.0	—	4.50	3.0	—	3.0		
	V _{IH}	5.0	3.5	—	3.5	2.75	—	3.5	—	V	
		10	7.0	—	7.0	5.50	—	7.0	—		
Input Voltage (V _O = 4.5 Vdc) (For Input 11 and Output 10) (V _O = 9.0 Vdc) (V _O = 13.5 Vdc)	V _{IL}	5.0	—	1.0	—	2.25	1.0	—	1.0	Vdc	
		10	—	2.0	—	4.50	2.0	—	2.0		
	V _{IH}	5.0	4.0	—	4.0	2.75	—	4.0	—	Vdc	
		10	8.0	—	8.0	5.50	—	8.0	—		
Output Drive Current (V _{OH} = 2.5 V) (Except Source (V _{OH} = 4.6 V) Pins 9 and 10) (V _{OH} = 9.5 V) (V _{OH} = 13.5 V)	I _{OH}	5.0	-3.0	—	-2.4	-4.2	—	-1.7	—	mA	
		5.0	-0.64	—	-0.51	-0.88	—	-0.36	—		
Sink (V _{OL} = 0.4 V) (V _{OL} = 0.5 V) (V _{OL} = 1.5 V)	I _{OL}	5.0	0.64	—	0.51	0.88	—	0.36	—	mA	
		10	1.6	—	1.3	2.25	—	0.9	—		
		15	4.2	—	3.4	8.8	—	2.4	—		
Input Current	I _{in}	15	—	±0.1	—	±0.0001	±0.1	—	±1.0	μA	
Input Capacitance (V _{in} = 0)	C _{in}	—	—	—	—	5.0	7.5	—	—	pF	
Quiescent Current (Per Package)	I _{DD}	5.0	—	5.0	—	0.005	5.0	—	150	μA	
		10	—	10	—	0.010	10	—	300		
		15	—	20	—	0.015	20	—	600		
Total Supply Current** (Dynamic plus Quiescent, Per Package) (C _L = 50 pF on all outputs, all buffers switching)	I _T	5.0	I _T = (0.25 μA/kHz) f + I _{DD}								μA
	10	I _T = (0.54 μA/kHz) f + I _{DD}									
	15	I _T = (0.85 μA/kHz) f + I _{DD}									

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C.

MC14060B

SWITCHING CHARACTERISTICS (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V _{DD} V _{dC}	Min	Typ #	Max	Unit
Output Rise Time (Counter Outputs)	t _{TLH}	5.0	—	40	200	ns
		10	—	25	100	
		15	—	20	80	
Output Fall Time (Counter Outputs)	t _{THL}	5.0	—	50	200	ns
		10	—	30	100	
		15	—	20	80	
Propagation Delay Time Clock to Q4 Clock to Q14	t _{PLH}	5.0	—	415	740	ns
		10	—	175	300	
		15	—	125	200	
	t _{PHL}	5.0	—	1.5	2.7	μs
		10	—	0.7	1.3	
		15	—	0.4	1.0	
Clock Pulse Width	t _{WH}	5.0	100	65	—	ns
		10	40	30	—	
		15	30	20	—	
Clock Pulse Frequency	f _φ	5.0	—	5	3.5	MHz
		10	—	14	8	
		15	—	17	12	
Clock Rise and Fall Time	t _{TLH}	5.0	No Limit			ns
	t _{THL}	10				
	15					
Reset Pulse Width	t _w	5.0	120	40	—	ns
		10	60	15	—	
		15	40	10	—	
Propagation Delay Time Reset to Qn	t _{PHL}	5.0	—	170	360	ns
		10	—	80	160	
		15	—	60	100	

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

FIGURE 1 — POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

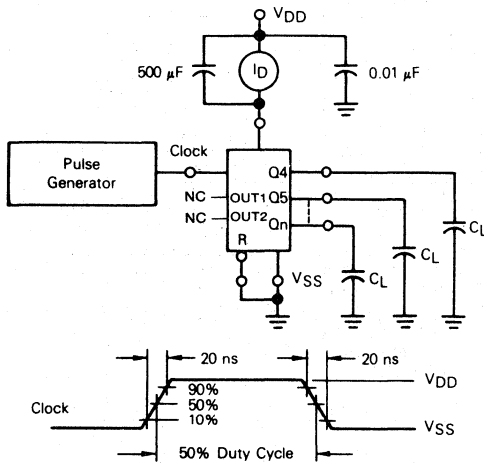
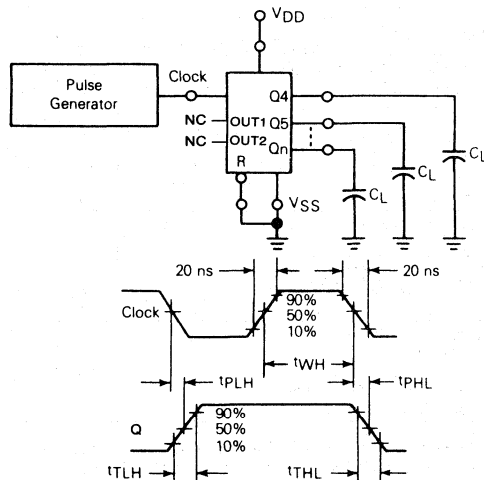
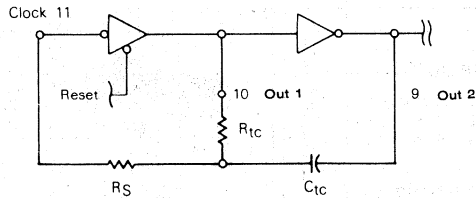


FIGURE 2 — SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



MC14060B

FIGURE 3 — OSCILLATOR CIRCUIT USING RC CONFIGURATION



$$f \approx \frac{1}{2.3 R_{Tc} C_{Tc}}$$

if $1 \text{ kHz} \leq f \leq 100 \text{ kHz}$
and $2R_{Tc} < R_S < 10R_{Tc}$
(f in Hz, R in ohms, C in farads)

The formula may vary for other frequencies. Recommended maximum value for the resistors is 1 M Ω .

TYPICAL RC OSCILLATOR CHARACTERISTICS

FIGURE 4 — RC OSCILLATOR STABILITY

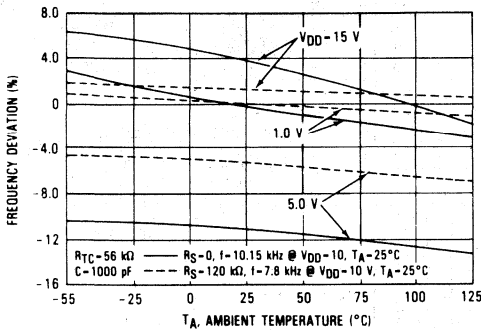


FIGURE 5 — RC OSCILLATOR FREQUENCY AS A FUNCTION OF R_{Tc} AND C

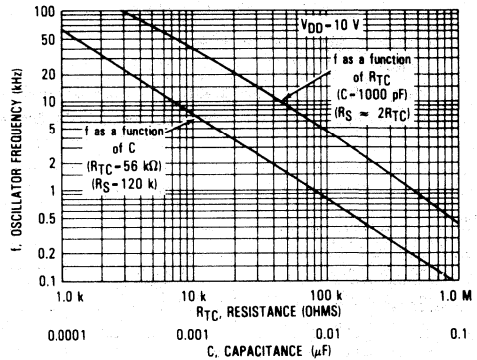


FIGURE 6 — TYPICAL CRYSTAL OSCILLATOR CIRCUIT

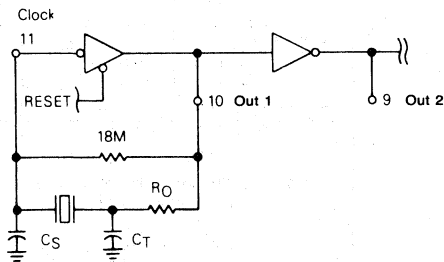


FIGURE 7 — TYPICAL DATA FOR CRYSTAL OSCILLATOR CIRCUIT

Characteristic	500 kHz Circuit	32 kHz Circuit	Unit
Crystal Characteristics			
Resonant Frequency	500	32	kHz
Equivalent Resistance, R_S	1.0	6.2	k Ω
External Resistor/Capacitor Values			
R_0	47	750	k Ω
C_T	82	82	pF
C_S	20	20	pF
Frequency Stability			
Frequency Changes as a Function of V_{DD} ($T_A = 25^\circ\text{C}$)			
V_{DD} Change from 5.0 V to 10 V	+6.0	+2.0	ppm
V_{DD} Change from 10 V to 15 V	+2.0	+2.0	ppm
Frequency Change as a Function of Temperature ($V_{DD} = 10 \text{ V}$)			
T_A Change from -55°C to $+25^\circ\text{C}$ Complete Oscillator*	+100	+120	ppm
T_A Change from $+25^\circ\text{C}$ to $+125^\circ\text{C}$ Complete Oscillator*	-160	-560	ppm

*Complete oscillator includes crystal, capacitors, and resistors.



MOTOROLA

MC14066B

QUAD ANALOG SWITCH/QUAD MULTIPLEXER

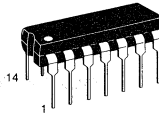
The MC14066B consists of four independent switches capable of controlling either digital or analog signals. This quad bilateral switch is useful in signal gating, chopper, modulator, demodulator and CMOS logic implementation.

The MC14066B is designed to be pin-for-pin compatible with the MC14016B, but has much lower ON resistance. Input voltage swings as large as the full supply voltage can be controlled via each independent control input.

- Triple Diode Protection on All Control Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Linearized Transfer Characteristics
- Low Noise — 12 nV/ $\sqrt{\text{Cycle}}$, $f \geq 1.0$ kHz typical
- Pin-for-Pin Replacement for CD4016, CD4016, MC14016B
- For Lower R_{ON} , Use The HC4066 High-Speed CMOS Device



L SUFFIX
CERAMIC
CASE 632



P SUFFIX
PLASTIC
CASE 646



D SUFFIX
SOIC
CASE 751A

ORDERING INFORMATION

MC14XXXBCP Plastic
MC14XXXBCL Ceramic
MC14XXXBD SOIC

$T_A = -55^\circ$ to 125°C for all packages.

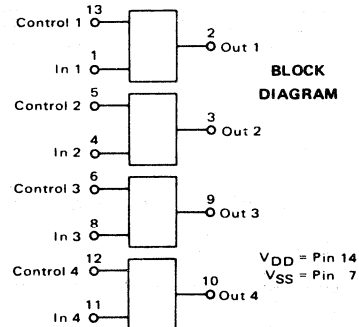
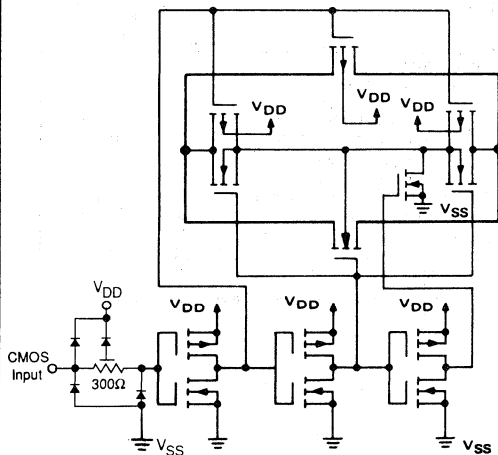
MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	-0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	-0.5 to $V_{DD} + 0.5$	V
I_{in}	Input Current (DC or Transient), per Control Pin	± 10	mA
I_{sw}	Switch Through Current	± 25	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	-65 to +150	$^\circ\text{C}$
T_L	Lead Temperature (8-Second Soldering)	260	$^\circ\text{C}$

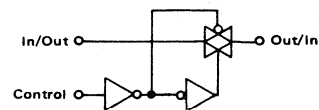
*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P and D/DW" Packages: -7.0 mW/ $^\circ\text{C}$ From 65°C To 125°C
Ceramic "L" Packages: -12 mW/ $^\circ\text{C}$ From 100°C To 125°C

6

CIRCUIT SCHEMATIC
(1/4 OF DEVICE SHOWN)



LOGIC DIAGRAM AND TRUTH TABLE
(1/4 OF DEVICE SHOWN)



Control	Switch	Logic Diagram Restrictions
0 = V_{SS}	OFF	$V_{SS} \leq V_{in} \leq V_{DD}$
1 = V_{DD}	ON	$V_{SS} \leq V_{out} \leq V_{DD}$

MC14066B

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V _{DD}	Test Conditions	-55°C		25°C			125°C		Unit
				Min	Max	Min	Typ #	Max	Min	Max	

SUPPLY REQUIREMENTS (Voltages Referenced to V_{EE})

Power Supply Voltage Range	V _{DD}	—		3.0	18	3.0	—	18	3.0	18	V	
Quiescent Current Per Package	I _{DD}	5.0 10 15	Control Inputs: V _{in} = V _{SS} or V _{DD} , Switch I/O: V _{SS} ≤ V _{I/O} ≤ V _{DD} , and ΔV _{switch} ≤ 500 mV**	— — —	0.25 0.5 1.0	— — —	0.005 0.010 0.015	0.25 0.5 1.0	— — —	7.5 15 30	μA	
Total Supply Current (Dynamic Plus Quiescent, Per Package)	I _{D(AV)}	5.0 10 15	T _A = 25°C only The channel component, (V _{in} - V _{out})/R _{ON} is not included.)	Typical (0.07 μA/kHz)f + I _{DD} (0.20 μA/kHz)f + I _{DD} (0.36 μA/kHz)f + I _{DD}								μA

CONTROL INPUTS (Voltages Referenced to V_{SS})

Low-Level Input Voltage	V _{IL}	5.0 10 15	R _{ON} = per spec, I _{off} = per spec	— — —	1.5 3.0 4.0	— — —	2.25 4.50 6.75	1.5 3.0 4.0	— — —	1.5 3.0 4.0	V
High-Level Input Voltage	V _{IH}	5.0 10 15	R _{ON} = per spec, I _{off} = per spec	3.5 7.0 11	— — —	3.5 7.0 11	2.75 5.50 8.25	— — —	3.5 7.0 11	— — —	V
Input Leakage Current	I _{in}	15	V _{in} = 0 or V _{DD}	—	±0.1	—	±0.00001	±0.1	—	±1.0	μA
Input Capacitance	C _{in}	—		—	—	—	5.0	7.5	—	—	pF

SWITCHES IN AND OUT (Voltages Referenced to V_{SS})

Recommended Peak-to-Peak Voltage Into or Out of the Switch	V _{I/O}	—	Channel On or Off	0	V _{DD}	0	—	V _{DD}	0	V _{DD}	V _{p-p}
Recommended Static or Dynamic Voltage Across the Switch** (Figure 1)	ΔV _{switch}	—	Channel On	0	600	0	—	600	0	300	mV
Output Offset Voltage	V _{OO}	—	V _{in} = 0 V, No Load	—	—	—	10	—	—	—	μV
ON Resistance	R _{ON}	5.0 10 15	ΔV _{switch} ≤ 500 mV**, V _{in} = V _{IL} or V _{IH} (Control), and V _{in} = 0 to V _{DD} (Switch)	— — —	800 400 220	— — —	250 120 80	1050 500 280	— — —	1200 520 300	Ω
ΔON Resistance Between Any Two Channels in the Same Package	ΔR _{ON}	5.0 10 15		— — —	70 50 45	— — —	25 10 10	70 50 45	— — —	135 95 65	Ω
Off-Channel Leakage Current (Figure 6)	I _{off}	15	V _{in} = V _{IL} or V _{IH} (Control) Channel to Channel or Any One Channel	—	±100	—	±0.05	±100	—	±1000	nA
Capacitance, Switch I/O	C _{I/O}	—	Switch Off	—	—	—	10	15	—	—	pF
Capacitance, Feedthrough (Switch Off)	C _{I/O}	—		—	—	—	0.47	—	—	—	pF

#Data labeled "Typ" is not to be used for design purposes, but is intended as an indication of the IC's potential performance.

**For voltage drops across the switch (ΔV_{switch}) > 600 mV (> 300 mV at high temperature), excessive V_{DD} current may be drawn; i.e. the current out of the switch may contain both V_{DD} and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded. (See first page of this data sheet.)

MC14066B

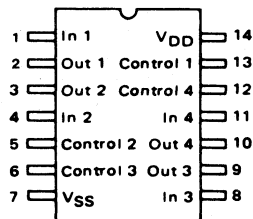
ELECTRICAL CHARACTERISTICS* ($C_L = 50$ pF, $T_A = 25^\circ\text{C}$ unless otherwise noted.)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ #	Max	Unit
Propagation Delay Times Input to Output ($R_L = 10$ k Ω) $V_{SS} = 0$ Vdc $t_{PLH}, t_{PHL} = (0.17 \text{ ns/pF}) C_L + 15.5 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.08 \text{ ns/pF}) C_L + 6.0 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.06 \text{ ns/pF}) C_L + 4.0 \text{ ns}$	t_{PLH}, t_{PHL}	5.0 10 15	— — —	20 10 7.0	40 20 15	ns
Control to Output ($R_L = 1$ k Ω) (Figure 2) Output "1" to High Impedance	t_{PHZ}	5.0 10 15	— — —	40 35 30	80 70 60	ns
Output "0" to High Impedance	t_{PLZ}	5.0 10 15	— — —	40 35 30	80 70 60	ns
High Impedance to Output "1"	t_{PZH}	5.0 10 15	— — —	60 20 15	120 40 30	ns
High Impedance to Output "0"	t_{PZL}	5.0 10 15	— — —	60 20 15	120 40 30	ns
Second Harmonic Distortion ($V_{in} = 1.77$ Vdc, RMS Centered @ 0.0 kHz, $R_L = 10$ k Ω , $f = 1.0$ kHz)	—	5.0	—	0.1	—	%
Bandwidth (Switch ON) (Figure 3) ($R_L = 1$ k Ω , $20 \text{ Log } \frac{V_{out}}{V_{in}} = -3$ dB, $C_L = 50$ pF, $V_{in} = 5$ V _{p-p})	—	5.0	—	65	—	MHz
Feedthrough Attenuation (Switch OFF) ($V_{in} = 5$ V _{p-p} , $R_L = 1$ k Ω , $f_{in} = 1.0$ MHz) (Figure 3)	—	5.0	—	-50	—	dB
Channel Separation (Figure 4) ($V_{in} = 5$ V _{p-p} , $R_L = 1$ k Ω , $f_{in} = 8.0$ MHz) (Switch A ON, Switch B OFF)	—	5.0	—	-50	—	dB
Crosstalk, Control Input to Signal Output (Figure 5) ($R_1 = 1$ k Ω , $R_L = 10$ k Ω , Control $t_{TLH} = t_{THL} = 20$ ns)	—	5.0	—	300	—	mV _{p-p}

*The formulas given are for the typical characteristics only at 25°C.
#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

PIN ASSIGNMENT



MC14066B

TEST CIRCUITS

FIGURE 1 — ΔV ACROSS SWITCH

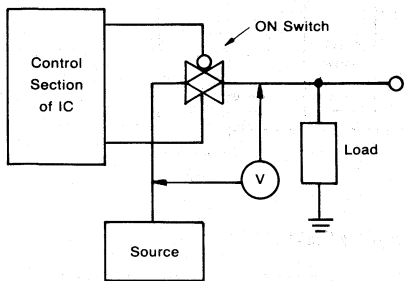


FIGURE 3 — BANDWIDTH AND FEEDTHROUGH ATTENUATION

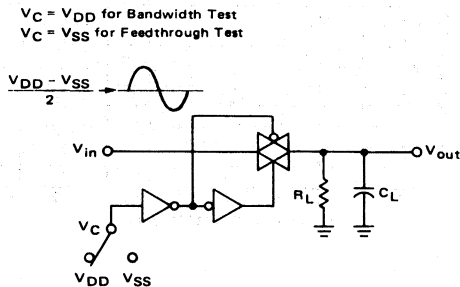


FIGURE 5 — CROSSTALK, CONTROL TO OUTPUT

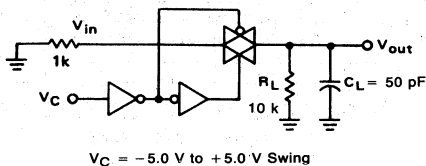


FIGURE 2 — TURN-ON DELAY TIME TEST CIRCUIT AND WAVEFORMS

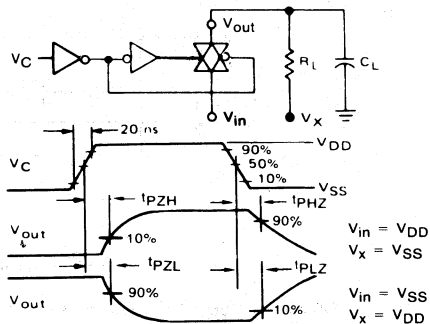


FIGURE 4 — CHANNEL SEPARATION

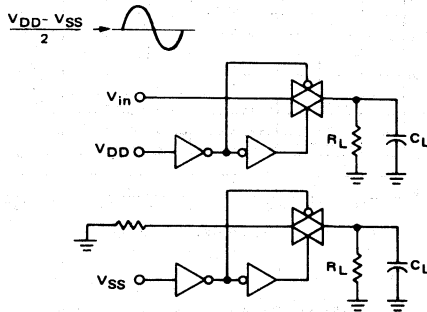
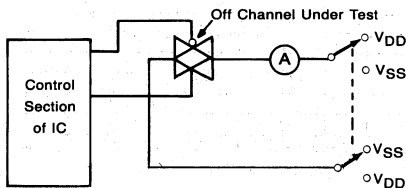
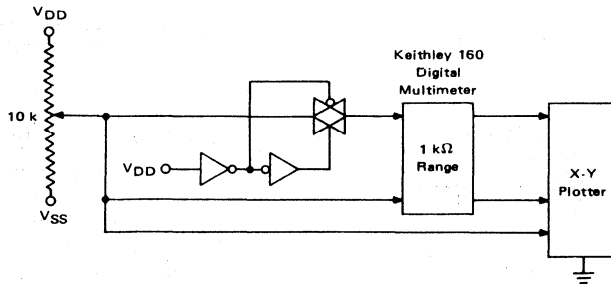


FIGURE 6 — OFF CHANNEL LEAKAGE



MC14066B

FIGURE 7 – CHANNEL RESISTANCE (R_{ON}) TEST CIRCUIT



TYPICAL RESISTANCE CHARACTERISTICS

FIGURE 8 – $V_{DD} = 7.5\text{ V}$, $V_{SS} = -7.5\text{ V}$

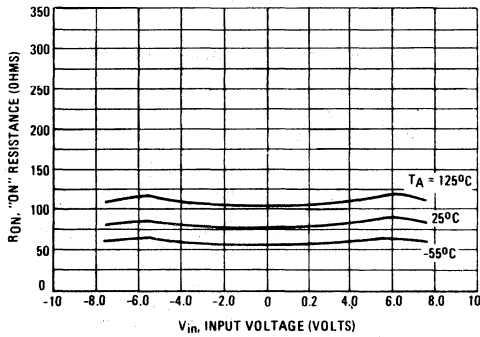


FIGURE 9 – $V_{DD} = 5.0\text{ V}$, $V_{SS} = -5.0\text{ V}$

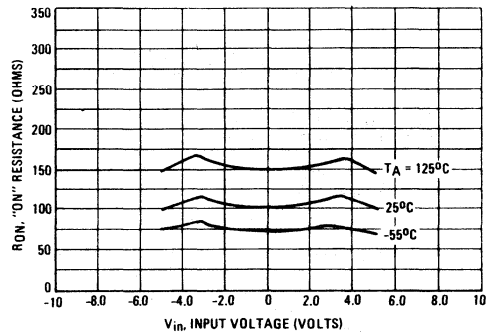


FIGURE 10 – $V_{DD} = 2.5\text{ V}$, $V_{SS} = -2.5\text{ V}$

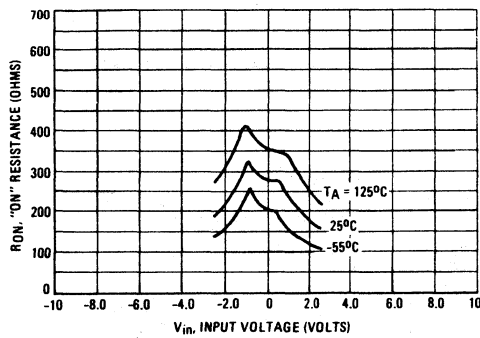
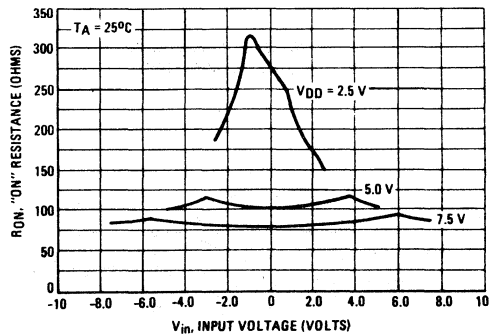


FIGURE 11 – COMPARISON AT 25°C, $V_{DD} = -V_{SS}$



6

MC14066B

APPLICATIONS INFORMATION

Figure A illustrates use of the Analog Switch. The 0-to-5 volt digital control signal is used to directly control a 5 volt peak-to-peak analog signal.

The digital control logic levels are determined by V_{DD} and V_{SS} . The V_{DD} voltage is the logic high voltage; the V_{SS} voltage is logic low. For the example, $V_{DD} = +5\text{ V} = \text{logic high}$ at the control inputs; $V_{SS} = \text{GND} = 0\text{ V} = \text{logic low}$.

The maximum analog signal level is determined by V_{DD} and V_{SS} . The analog voltage must not swing higher than V_{DD} or lower than V_{SS} .

The example shows a 5 volt peak-to-peak signal which allows no margin at either peak. If voltage transients above V_{DD} and/or below V_{SS} are anticipated on the analog channels, external diodes (D_x) are recommended as shown in Figure B. These diodes should be small signal types able to absorb the maximum anticipated current surges during clipping.

The *absolute* maximum potential difference between V_{DD} and V_{SS} is 18.0 volts. Most parameters are specified up to 15 volts which is the *recommended* maximum difference between V_{DD} and V_{SS} .

FIGURE A — APPLICATION EXAMPLE

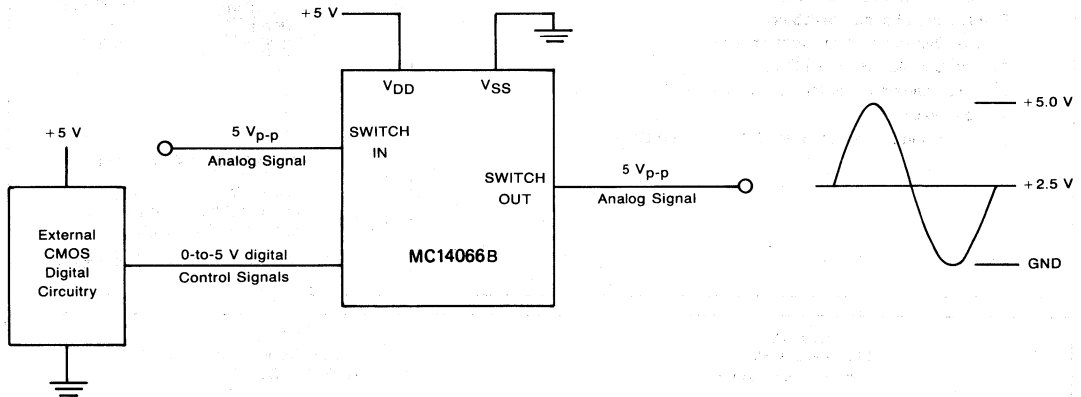
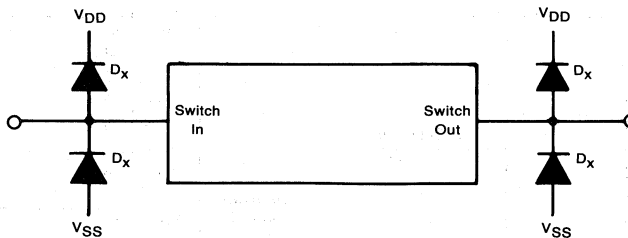


FIGURE B — EXTERNAL GERMANIUM OR SCHOTTKY CLIPPING DIODES





MOTOROLA

**MC14067B
MC14097B**

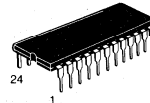
ANALOG MULTIPLEXERS/DEMULTIPLEXERS

The MC14067 and MC14097 multiplexers/demultiplexers are digitally controlled analog switches featuring low ON resistance and very low leakage current. These devices can be used in either digital or analog applications.

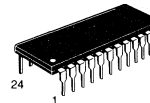
The MC14067 is a 16-channel multiplexer/demultiplexer with an inhibit and four binary control inputs A, B, C, and D. These control inputs select 1-of-16 channels by turning ON the appropriate analog switch (see MC14067 truth table.)

The MC14097 is a differential 8-channel multiplexer/demultiplexer with an inhibit and three binary control inputs A, B, and C. These control inputs select 1 of 8 pairs of channels by turning ON the appropriate analog switches (see MC14097 truth table).

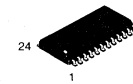
- Low OFF Leakage Current
- Matched Channel Resistance
- Low Quiescent Power Consumption
- Low Crosstalk Between Channels
- Wide Operating Voltage Range: 3 to 18 V
- Low Noise
- Pin for Pin Replacement for CD4067B and CD4097B



**L SUFFIX
CERAMIC
CASE 623**



**P SUFFIX
PLASTIC
CASE 709**



**DW SUFFIX
SOIC
CASE 751E**

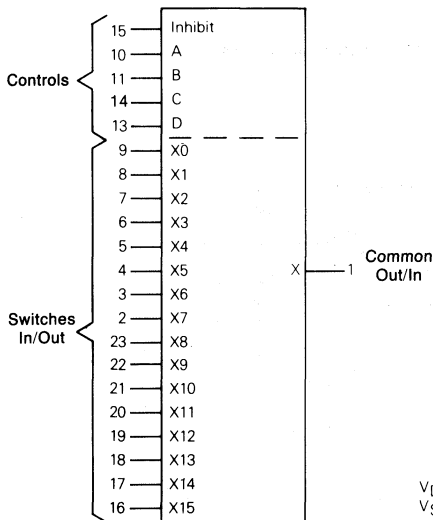
ORDERING INFORMATION

MC14XXXBCP Plastic
MC14XXXBCL Ceramic
MC14XXXBDW SOIC

$T_A = -55^\circ$ to 125°C for all packages.

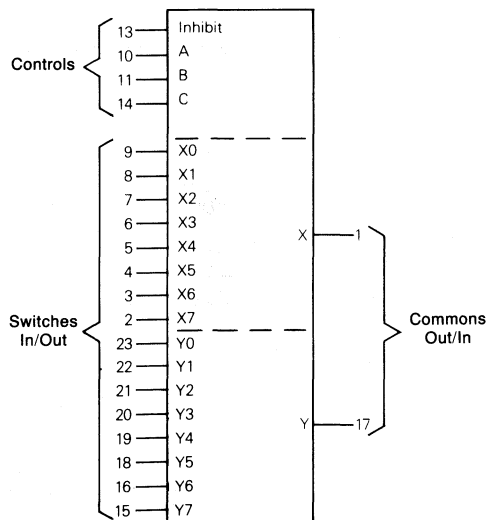
6

**MC14067B
16-Channel Analog
Multiplexer/Demultiplexer**



V_{DD} = Pin 24
 V_{SS} = Pin 12

**MC14097B
Dual 8-Channel Analog
Multiplexer/Demultiplexer**



MC14067B-MC14097B

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	-0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	-0.5 to $V_{DD} + 0.5$	V
I_{in}	Input Current (DC or Transient), per Control Pin	± 10	mA
I_{sw}	Switch Through Current	± 25	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
 †Temperature Derating: Plastic "P and D/DW" Packages: -7.0 mW/°C From 65°C To 125°C
 Ceramic "L" Packages: -12 mW/°C From 100°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

MC14067 TRUTH TABLE

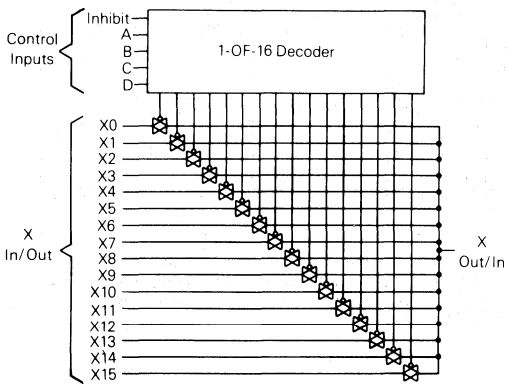
Control Inputs					Selected Channel
A	B	C	D	Inh	
X	X	X	X	1	None
0	0	0	0	0	X0
1	0	0	0	0	X1
0	1	0	0	0	X2
1	1	0	0	0	X3
0	0	1	0	0	X4
1	0	1	0	0	X5
0	1	1	0	0	X6
1	1	1	0	0	X7
0	0	0	1	0	X8
1	0	0	1	0	X9
0	1	0	1	0	X10
1	1	0	1	0	X11
0	0	1	1	0	X12
1	0	1	1	0	X13
0	1	1	1	0	X14
1	1	1	1	0	X15

MC14097 TRUTH TABLE

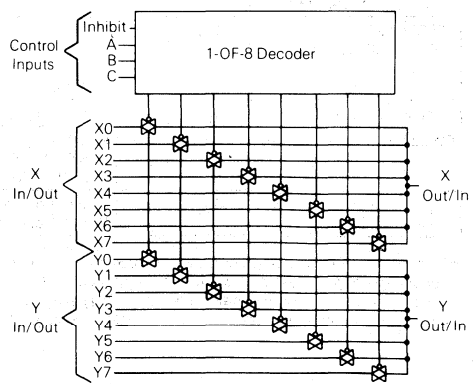
Control Inputs				Selected Channels
A	B	C	Inh	
X	X	X	1	None
0	0	0	0	X0 Y0
1	0	0	0	X1 Y1
0	1	0	0	X2 Y2
1	1	0	0	X3 Y3
0	0	1	0	X4 Y4
1	0	1	0	X5 Y5
0	1	1	0	X6 Y6
1	1	1	0	X7 Y7

X = Don't Care

MC14067 FUNCTIONAL DIAGRAM



MC14097 FUNCTIONAL DIAGRAM



MC14067B·MC14097B

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V _{DD}	Test Conditions	-55°C		25°C			125°C		Unit
				Min	Max	Min	Typ #	Max	Min	Max	

SUPPLY REQUIREMENTS (Voltages Referenced to V_{SS})

Power Supply Voltage Range	V _{DD}	—		3.0	18	3.0	—	18	3.0	18	V
Quiescent Current Per Package	I _{DD}	5.0 10 15	Control Inputs: V _{in} = V _{SS} or V _{DD} . Switch I/O: V _{SS} ≤ V _{I/O} ≤ V _{DD} , and ΔV _{switch} ≤ 500 mV**	— — —	5.0 10 20	— — —	0.005 0.010 0.015	5.0 10 20	— — —	150 300 600	μA
Total Supply Current (Dynamic Plus Quiescent, Per Package)	I _{D(AV)}	5.0 10 15	T _A = 25°C only (The channel component, (V _{in} - V _{out})/R _{on} , is not included.)	Typical			(0.07 μA/kHz)f + (0.20 μA/kHz)f + (0.36 μA/kHz)f +	I _{DD} I _{DD} I _{DD}			μA

CONTROL INPUTS — INHIBIT, A, B, C, D (Voltages Referenced to V_{SS})

Low-Level Input Voltage	V _{IL}	5.0 10 15	R _{on} = per spec, I _{off} = per spec	— — —	1.5 3.0 4.0	— — —	2.25 4.50 6.75	1.5 3.0 4.0	— — —	1.5 3.0 4.0	V
High-Level Input Voltage	V _{IH}	5.0 10 15	R _{on} = per spec, I _{off} = per spec	3.5 7.0 11	— — —	3.5 7.0 11	2.75 5.50 8.25	— — —	3.5 7.0 11	— — —	V
Input Leakage Current	I _{in}	15	V _{in} = 0 or V _{DD}	—	±0.1	—	±0.00001	±0.1	—	±1.0	μA
Input Capacitance	C _{in}	—		—	—	—	5.0	7.5	—	—	pF

SWITCHES IN/OUT AND COMMONS OUT/IN — X, Y (Voltages Referenced to V_{SS})

Recommended Peak-to-Peak Voltage Into or Out of the Switch	V _{I/O}	—	Channel On or Off	0	V _{DD}	0	—	V _{DD}	0	V _{DD}	V _{p-p}
Recommended Static or Dynamic Voltage Across the Switch** (Figure 1)	ΔV _{switch}	—	Channel On	0	600	0	—	600	0	300	mV
Output Offset Voltage	V _{OO}	—	V _{in} = 0 V, No Load	—	—	—	10	—	—	—	μV
ON Resistance	R _{on}	5.0 10 15	ΔV _{switch} ≤ 500 mV**, V _{in} = V _{IL} or V _{IH} (Control), and V _{in} = 0 to V _{DD} (Switch)	— — —	800 400 220	— — —	250 120 80	1050 500 280	— — —	1300 550 320	Ω
ΔON Resistance Between Any Two Channels in the Same Package	ΔR _{on}	5.0 10 15		— — —	70 50 45	— — —	25 10 10	70 50 45	— — —	135 95 65	Ω
Off-Channel Leakage Current (Figure 2)	I _{off}	15	V _{in} = V _{IL} or V _{IH} (Control) Channel to Channel or Any One Channel	—	±100	—	±0.05	±100	—	±1000	nA
Capacitance, Switch I/O	C _{I/O}	—	Inhibit = V _{DD}	—	—	—	10	—	—	—	pF
Capacitance, Common O/I	C _{O/I}	—	Inhibit = V _{DD} (MC14067B) (MC14097B)	— —	— —	— —	100 60	— —	— —	— —	pF
Capacitance, Feedthrough (Channel Off)	C _{I/O}	—	Pins Not Adjacent Pins Adjacent	— —	— —	— —	0.47	—	—	—	pF

#Data labeled "Typ" is not to be used for design purposes, but is intended as an indication of the IC's potential performance.
 **For voltage drops across the switch (ΔV_{switch}) >600 mV (>300 mV at high temperature), excessive V_{DD} current may be drawn; i.e. the current out of the switch may contain both V_{DD} and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded. (See first page of this data sheet.)

MC14067B·MC14097B

ELECTRICAL CHARACTERISTICS (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V _{DD} - V _{SS} V _{dC}	Typ #	Max	Unit
Propagation Delay Times Channel Input-to-Channel Output (R _L = 200kΩ) MC14067B	t _{PLH} , t _{PHL} (Figure 3)	5.0	35	90	ns
		10	15	40	
MC14097B		5.0	25	65	ns
		10	10	25	
		15	7	18	
Control Input-to-Channel Output Channel Turn-On Time (R _L = 10 kΩ) MC14067B/097B	t _{PZH} , t _{PZL} (Figure 4)	5.0	240	600	ns
		10	115	290	
		15	75	190	
Channel Turn-Off Time (R _L = 300 kΩ) MC14067B/097B	t _{PHZ} , t _{PLZ} (Figure 4)	5.0	250	625	ns
		10	120	300	
		15	75	190	
Any Pair of Address Inputs to Output MC14067B	t _{PLH} , t _{PHL} (Figure 10)	5.0	280	700	ns
		10	115	290	
MC14097B		5.0	250	625	ns
		10	100	250	
		15	75	190	
Second Harmonic Distortion (R _L = 10 kΩ, f = 1 kHz, V _{in} = 5 V _{p-p})	—	10	0.3	—	%
ON Channel Bandwidth [R _L = 1 kΩ, V _{in} = 1/2 (V _{DD} - V _{SS}) p-p (sine-wave)] 20 Log ₁₀ $\frac{V_{out}}{V_{in}}$ = -3 dB	BW (Figure 5)	10	15	—	MHz
MC14067B		10	25	—	
Off Channel Feedthrough Attenuation [R _L = 1 kΩ, V _{in} = 1/2 (V _{DD} - V _{SS}) p-p (sine-wave)] f _{in} = 20 MHz - MC14067B f _{in} = 12 MHz - MC14097B	— (Figure 5)	10	-40	—	dB
Channel Separation [R _L = 1 kΩ, V _{in} = 1/2 (V _{DD} - V _{SS}) p-p (sine-wave)] f _{in} = 20 MHz	— (Figure 6)	10	-40	—	
Crosstalk, Control Inputs-to-Common O/I (R ₁ = 1kΩ, R _L = 10 kΩ, Control t _r = t _f = 20 ns, Inhibit = V _{SS})	— (Figure 7)	10	30	—	mV

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

MC14067B•MC14097B

FIGURE 1 — ΔV ACROSS SWITCH

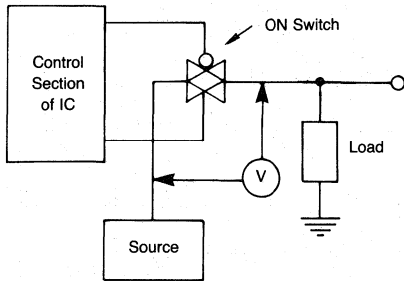
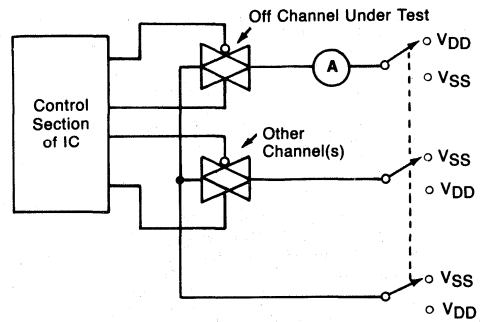
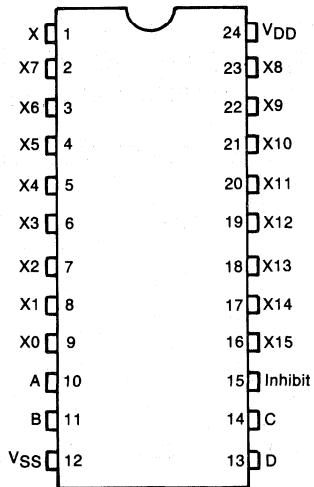


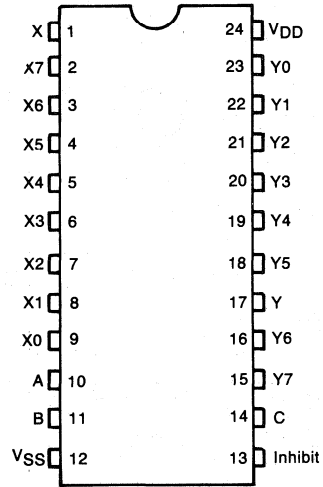
FIGURE 2 — OFF CHANNEL LEAKAGE



**MC14067B
PIN ASSIGNMENT**



**MC14097B
PIN ASSIGNMENT**



MC14067B·MC14097B

FIGURE 3 — PROPAGATION DELAY TEST CIRCUIT AND WAVEFORMS V_{in} to V_{out}

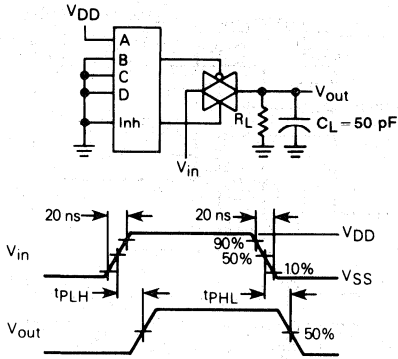


FIGURE 4 — TURN-ON AND DELAY TURN-OFF TEST CIRCUIT AND WAVEFORMS

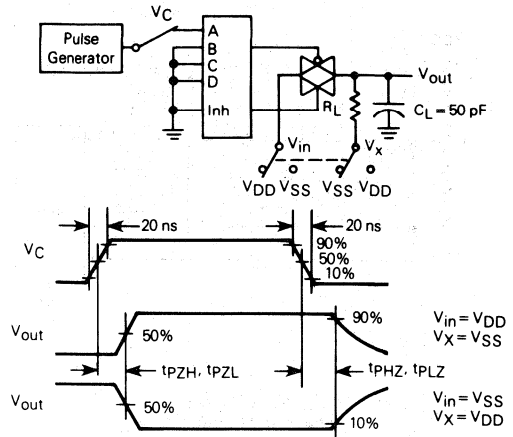


FIGURE 5 — BANDWIDTH AND OFF-CHANNEL FEEDTHROUGH ATTENUATION

A, B, and C inputs used to turn ON or OFF the switch under test.

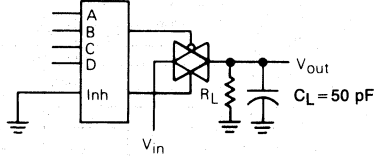


FIGURE 6 — CHANNEL SEPARATION (Adjacent Channels Used for Setup)

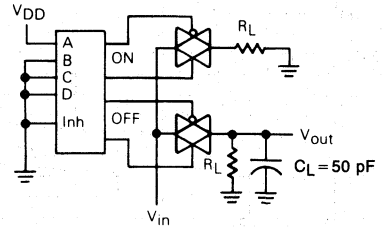


FIGURE 7 — CROSSTALK, CONTROL TO COMMON O/I

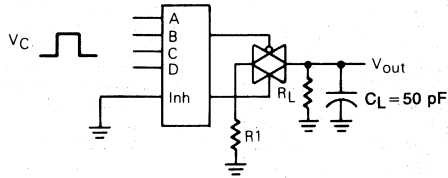


FIGURE 9 — CHANNEL RESISTANCE (R_{ON}) TEST CIRCUIT

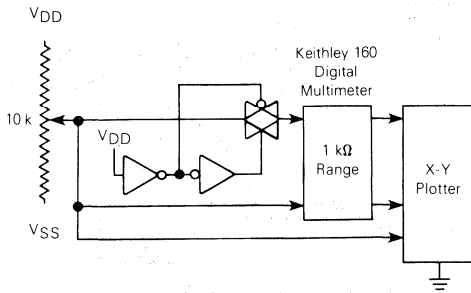
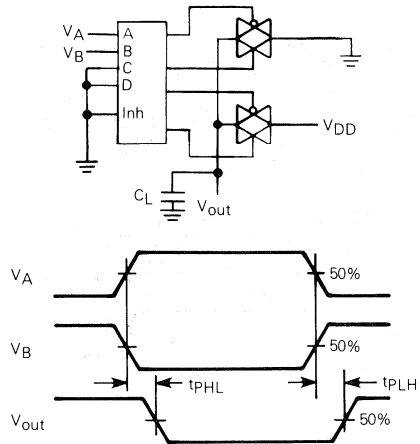


FIGURE 10 — PROPAGATION DELAY, ANY PAIR OF ADDRESS INPUTS to OUTPUT



TYPICAL RESISTANCE CHARACTERISTICS

FIGURE 11 — $V_{DD} = 7.5 \text{ V}$, $V_{SS} = -7.5 \text{ V}$

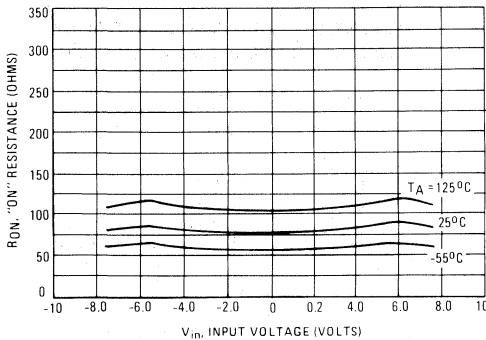


FIGURE 12 — $V_{DD} = 5.0 \text{ V}$, $V_{SS} = -5.0 \text{ V}$

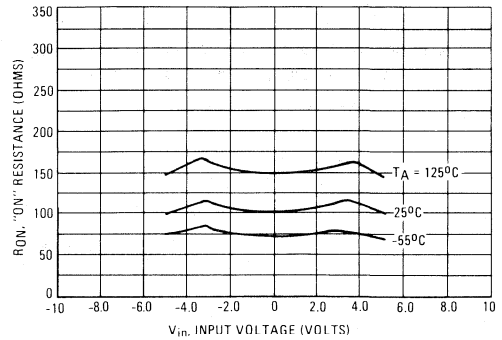


FIGURE 13 — $V_{DD} = 2.5 \text{ V}$, $V_{SS} = -2.5 \text{ V}$

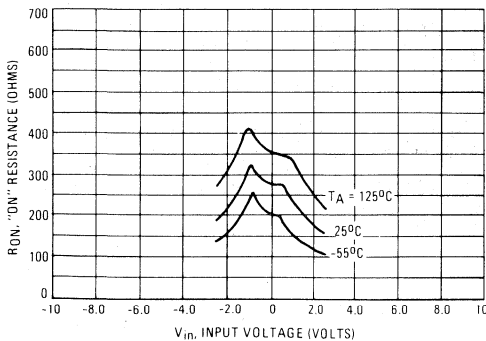
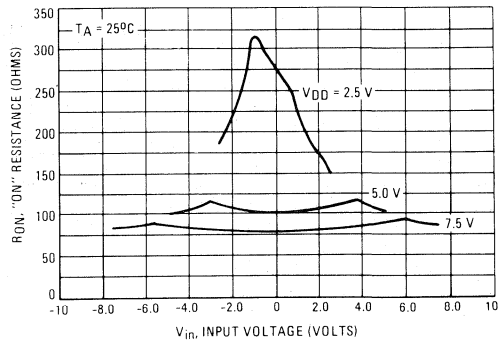


FIGURE 14 — COMPARISON AT 25°C, $V_{DD} = -V_{SS}$



6

MC14067B•MC14097B

APPLICATIONS INFORMATION

Figure A illustrates use of the Analog Multiplexer/Demultiplexer. The 0-to-5 volt Digital Control signal is used to directly control a 5 V_{p-p} analog signal.

The digital control logic levels are determined by V_{DD} and V_{SS} . The V_{DD} voltage is the logic high voltage; the V_{SS} voltage is logic low. For the example, $V_{DD} = +5\text{ V} = \text{logic high}$ at the control inputs; $V_{SS} = \text{GND} = 0\text{ V} = \text{logic low}$.

The maximum analog signal level is determined by V_{DD} and V_{SS} . The analog voltage must swing neither higher than V_{DD} nor lower than V_{SS} . The example

shows a 5 V_{p-p} signal which allows no margin at either peak. If voltage transients above V_{DD} and/or below V_{SS} are anticipated on the analog channels, external diodes (D_x) are recommended as shown in Figure B. These diodes should be small signal types able to absorb the maximum anticipated current surges during clipping.

The *absolute* maximum potential difference between V_{DD} and V_{SS} is 18.0 volts. Most parameters are specified up to 15 V which is the *recommended* maximum difference between V_{DD} and V_{SS} .

FIGURE A — APPLICATION EXAMPLE

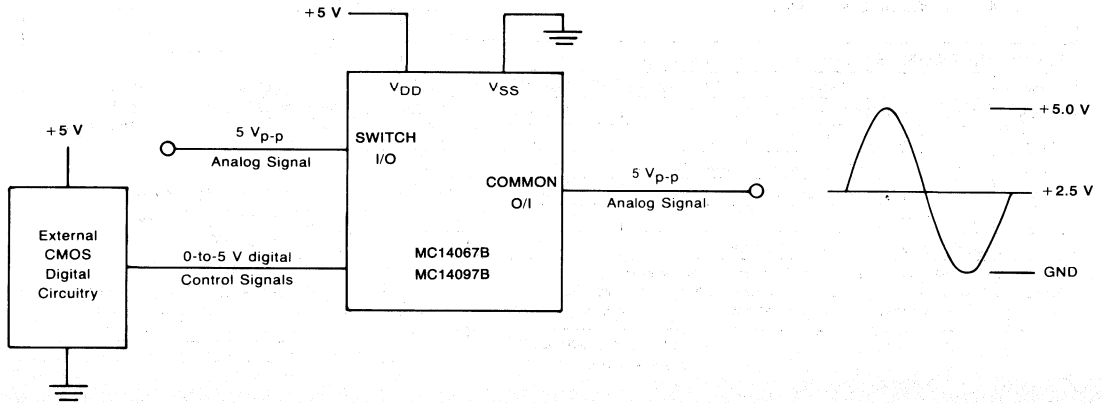
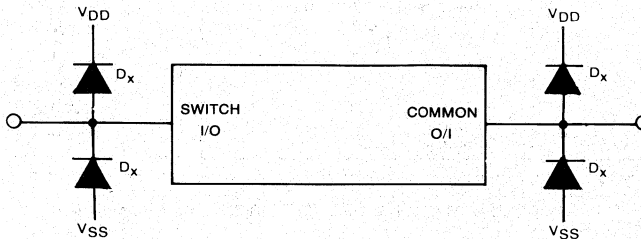


FIGURE B — EXTERNAL GERMANIUM OR SCHOTTKY CLIPPING DIODES





MOTOROLA

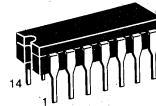
MC14068B
See Page 6-5

MC14069UB

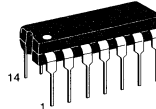
HEX INVERTER

The MC14069UB hex inverter is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These inverters find primary use where low power dissipation and/or high noise immunity is desired. Each of the six inverters is a single stage to minimize propagation delays.

- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-Power TTL Loads or One Low-Power Schottky TTL Load Over the Rated Temperature Range
- Triple Diode Protection on All Inputs (see Page 5-2)
- Pin-for-Pin Replacement for CD4069UB
- Meets JEDEC UB Specifications



L SUFFIX
CERAMIC
CASE 632



P SUFFIX
PLASTIC
CASE 646



D SUFFIX
SOIC
CASE 751A

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	-0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	-0.5 to $V_{DD} + 0.5$	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	± 10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.

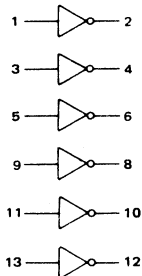
†Temperature Derating: Plastic "P and D/DW" Packages: -7.0 mW/°C From 65°C To 125°C
Ceramic "L" Packages: -12 mW/°C From 100°C To 125°C

ORDERING INFORMATION

MC14XXXUBCP Plastic
MC14XXXUBCL Ceramic
MC14XXXUBD SOIC

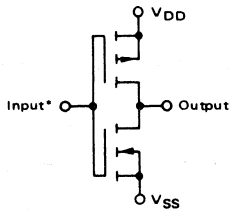
$T_A = -55^\circ$ to 125° C for all packages.

LOGIC DIAGRAM



V_{DD} = Pin 14
 V_{SS} = Pin 7

CIRCUIT SCHEMATIC
(1/6 OF CIRCUIT SHOWN)



*Double diode protection on all inputs not shown.

PIN ASSIGNMENT

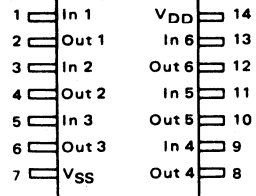
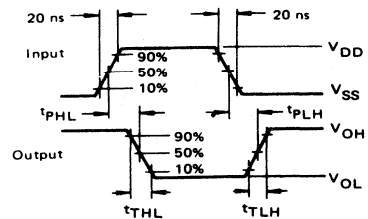
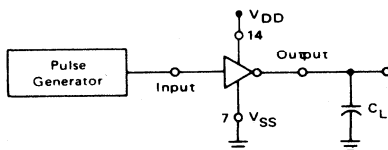


FIGURE 1 - SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



MC14069UB

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V _{DD} V _{dC}	-55°C		25°C			125°C		Unit
			Min	Max	Min	Typ #	Max	Min	Max	
Output Voltage V _{in} = V _{DD}	"0" Level V _{OL}	5.0	—	0.05	—	0	0.05	—	0.05	V _{dC}
		10	—	0.05	—	0	0.05	—	0.05	
		15	—	0.05	—	0	0.05	—	0.05	
	"1" Level V _{OH}	5.0	4.95	—	4.95	5.0	—	4.95	—	
		10	9.95	—	9.95	10	—	9.95	—	
		15	14.95	—	14.95	15	—	14.95	—	
Input Voltage (V _O = 4.5 V _{dC}) (V _O = 9.0 V _{dC}) (V _O = 13.5 V _{dC})	"0" Level V _{IL}	5.0	—	1.0	—	2.25	1.0	—	1.0	V _{dC}
		10	—	2.0	—	4.50	2.0	—	2.0	
		15	—	2.5	—	6.75	2.5	—	2.5	
	"1" Level V _{IH}	5.0	4.0	—	4.0	2.75	—	4.0	—	
		10	8.0	—	8.0	5.50	—	8.0	—	
		15	12.5	—	12.5	8.25	—	12.5	—	
Output Drive Current (V _{OH} = 2.5 V _{dC}) (V _{OH} = 4.6 V _{dC}) (V _{OH} = 9.5 V _{dC}) (V _{OH} = 13.5 V _{dC})	Source I _{OH}	5.0	-3.0	—	-2.4	-4.2	—	-1.7	—	mAdc
		5.0	-0.64	—	-0.51	-0.88	—	-0.36	—	
		10	-1.6	—	-1.3	-2.25	—	-0.9	—	
	Sink I _{OL}	5.0	0.64	—	0.51	0.88	—	0.36	—	
		10	1.6	—	1.3	2.25	—	0.9	—	
		15	4.2	—	3.4	8.8	—	2.4	—	
Input Current	I _{in}	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	μAdc
Input Capacitance (V _{in} = 0)	C _{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)	I _{DD}	5.0	—	0.25	—	0.0005	0.25	—	7.5	μAdc
10	—	0.5	—	0.0010	—	0.5	—	15	—	
15	—	1.0	—	0.0015	—	1.0	—	30	—	
Total Supply Current**† (Dynamic plus Quiescent, Per Gate) (C _L = 50 pF)	I _T	5.0	I _T = (0.3 μA/kHz) f + I _{DD} /6							μAdc
10	I _T = (0.6 μA/kHz) f + I _{DD} /6									
15	I _T = (0.9 μA/kHz) f + I _{DD} /6									
Output Rise and Fall Times** (C _L = 50 pF)	t _{TLH} , t _{THL}	5.0	—	—	—	100	200	—	—	ns
t _{TLH} :t _{THL} = (1.35 ns/pF) C _L + 33 ns	10	—	—	—	—	50	100	—	—	
t _{TLH} :t _{THL} = (0.60 ns/pF) C _L + 20 ns	15	—	—	—	—	40	80	—	—	
t _{TLH} :t _{THL} = (0.40 ns/pF) C _L + 20 ns										
Propagation Delay Times** (C _L = 50 pF)	t _{PLH} , t _{PHL}	5.0	—	—	—	65	125	—	—	ns
t _{PLH} :t _{PHL} = (0.90 ns/pF) C _L + 20 ns	10	—	—	—	—	40	75	—	—	
t _{PLH} :t _{PHL} = (0.36 ns/pF) C _L + 22 ns	15	—	—	—	—	30	55	—	—	
t _{PLH} :t _{PHL} = (0.26 ns/pF) C _L + 17 ns										

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) V/k$$

where: I_T is in μA (per package), C_L in pF, V = (V_{DD} - V_{SS}) in volts, f in kHz is input frequency, and k = 0.002.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained

to the range V_{SS} ≤ (V_{in} or V_{out}) ≤ V_{DD}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.



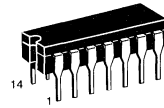
MC14070B MC14077B

CMOS SSI

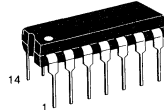
QUAD EXCLUSIVE "OR" AND "NOR" GATES

The MC14070B quad exclusive OR gate and the MC14077B quad exclusive NOR gate are constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These complementary MOS logic gates find primary use where low power dissipation and/or high noise immunity is desired.

- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- All Outputs Buffered
- Capable of Driving Two Low-Power TTL Loads or One Low-Power Schottky TTL Load Over the Rated Temperature Range
- Double Diode Protection on All Inputs
- MC14070B — Replacement for CD4030B and CD4070B Types
- MC14077B — Replacement for CD4077B Type



L SUFFIX
CERAMIC
CASE 632



P SUFFIX
PLASTIC
CASE 646



D SUFFIX
SOIC
CASE 751A

ORDERING INFORMATION

MC14XXXBCP Plastic
MC14XXXBCL Ceramic
MC14XXXBD SOIC

T_A = -55° to 125°C for all packages.

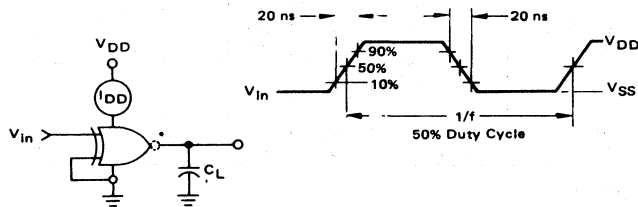
MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V _{DD}	DC Supply Voltage	-0.5 to +18.0	V
V _{In, Vout}	Input or Output Voltage (DC or Transient)	-0.5 to V _{DD} + 0.5	V
I _{In, Iout}	Input or Output Current (DC or Transient), per Pin	± 10	mA
P _D	Power Dissipation, per Package†	500	mW
T _{stg}	Storage Temperature	-65 to +150	°C
T _L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.

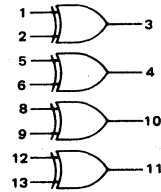
†Temperature Derating: Plastic "P and D/DW" Packages: -7.0 mW/°C From 65°C To 125°C
Ceramic "L" Packages: -12 mW/°C From 100°C To 125°C

FIGURE 1 — POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

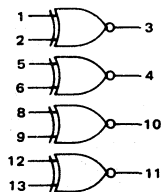


*Inverted output on MC14077B only.

MC14070B Quad Exclusive OR Gate

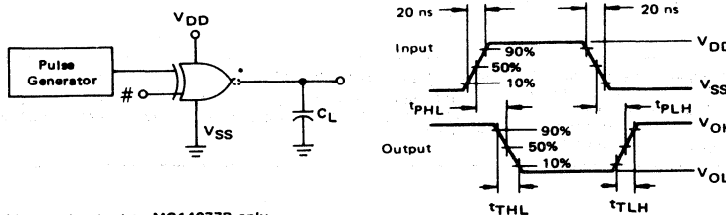


MC14077B Quad Exclusive NOR Gate



V_{DD} = Pin 14
V_{SS} = Pin 7
(Both Devices)

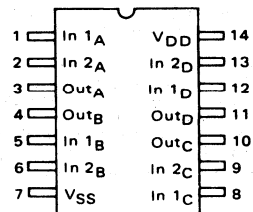
FIGURE 2 — SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



*Inverted output on MC14077B only.

#Connect unused input to V_{DD} for MC14070B, to V_{SS} for MC14077B.

PIN ASSIGNMENT



MC14070B•MC14077B

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V _{DD} Vdc	-55°C		25°C			125°C		Unit
			Min	Max	Min	Typ #	Max	Min	Max	
Output Voltage V _{in} = V _{DD} or 0	V _{OL}	5.0 10 15	—	0.05	—	0	0.05	—	0.05	Vdc
			—	0.05	—	0	0.05	—	0.05	
—			0.05	—	0	0.05	—	0.05		
V _{in} = 0 or V _{DD}	V _{OH}	5.0 10 15	4.95	—	4.95	5.0	—	4.95	—	Vdc
			9.95	—	9.95	10	—	9.95	—	
			14.95	—	14.95	15	—	14.95	—	
Input Voltage (V _O = 4.5 or 0.5 Vdc) (V _O = 9.0 or 1.0 Vdc) (V _O = 13.5 or 1.5 Vdc)	V _{IL}	5.0 10 15	—	1.5	—	2.25	1.5	—	1.5	Vdc
			—	3.0	—	4.50	3.0	—	3.0	
			—	4.0	—	6.75	4.0	—	4.0	
	V _{IH}	5.0 10 15	3.5	—	3.5	2.75	—	3.5	—	Vdc
			7.0	—	7.0	5.50	—	7.0	—	
			11	—	11	8.25	—	11	—	
Output Drive Current (V _{OH} = 2.5 Vdc) (V _{OH} = 4.6 Vdc) (V _{OH} = 9.5 Vdc) (V _{OH} = 13.5 Vdc)	Source	I _{OH}	5.0	-3.0	—	-2.4	-4.2	—	-1.7	mAdc
			5.0	-0.64	—	-0.51	-0.88	—	-0.36	
			10	-1.6	—	-1.3	-2.25	—	-0.9	
	Sink	I _{OL}	5.0 10 15	0.64	—	0.51	0.88	—	0.36	mAdc
				1.6	—	1.3	2.25	—	0.9	
				4.2	—	3.4	8.8	—	2.4	
Input Current	I _{in}	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	μAdc
Input Capacitance (V _{in} = 0)	C _{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)	I _{DD}	5.0 10 15	—	0.25	—	0.0005	0.25	—	7.5	μAdc
			—	0.5	—	0.0010	0.5	—	15	
			—	1.0	—	0.0015	1.0	—	30	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C _L = 50 pF on all outputs, all buffers switching)	I _T	5.0 10 15	I _T = (0.3 μA/kHz) f + I _{DD}						μAdc	
			I _T = (0.6 μA/kHz) f + I _{DD}							
			I _T = (0.9 μA/kHz) f + I _{DD}							
Output Rise and Fall Times** (C _L = 50 pF) t _{TLH} , t _{THL} = (1.35 ns/pF) C _L + 33 ns t _{TLH} , t _{THL} = (0.60 ns/pF) C _L + 20 ns t _{TLH} , t _{THL} = (0.40 ns/pF) C _L + 20 ns	t _{TLH} , t _{THL}	5.0 10 15	—	—	—	100	200	—	—	ns
			—	—	—	50	100	—	—	
			—	—	—	40	80	—	—	
			—	—	—	—	—	—	—	
Propagation Delay Times** (C _L = 50 pF) t _{PLH} , t _{PHL} = (0.90 ns/pF) C _L + 130 ns t _{PLH} , t _{PHL} = (0.36 ns/pF) C _L + 57 ns t _{PLH} , t _{PHL} = (0.26 ns/pF) C _L + 37 ns	t _{PLH} , t _{PHL}	5.0 10 15	—	—	—	175	350	—	—	ns
			—	—	—	75	150	—	—	
			—	—	—	55	110	—	—	
			—	—	—	—	—	—	—	

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) \text{ V/k}$$

where: I_T is in μA (per package), C_L in pF, V = (V_{DD} - V_{SS}) in volts, f in kHz is input frequency, and k = 0.002.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range V_{SS} ≤ (V_{in} or V_{out}) ≤ V_{DD}. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.



MOTOROLA

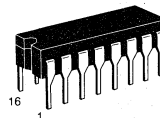
MC14071B thru MC14073B,
MC14075B
See Page 6-5

MC14076B

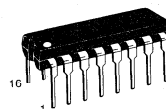
**4-BIT D-TYPE REGISTER
with THREE-STATE OUTPUTS**

The MC14076B 4-Bit Register consists of four D-type flip-flops operating synchronously from a common clock. OR gated output-disable inputs force the outputs into a high-impedance state for use in bus organized systems. OR gated data-disable inputs cause the Q outputs to be fed back to the D inputs of the flip-flops. Thus they are inhibited from changing state while the clocking process remains undisturbed. An asynchronous master reset is provided to clear all four flip-flops simultaneously independent of the clock or disable inputs.

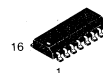
- Three-State Outputs with Gated Control Lines
- Fully Independent Clock Allows Unrestricted Operation for the Two Modes: Parallel Load and Do Nothing
- Asynchronous Master Reset
- Four Bus Buffer Registers
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-Power TTL Loads or One Low-Power Schottky TTL Load Over the Rated Temperature Range
- Schottky TTL Load Over the Rated Temper



L SUFFIX
CERAMIC
CASE 620



P SUFFIX
PLASTIC
CASE 648



D SUFFIX
SOIC
CASE 751B

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	-0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	-0.5 to $V_{DD} + 0.5$	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	± 10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P and D/DW" Packages: -7.0 mW/°C From 65°C To 125°C
Ceramic "L" Packages: -12 mW/°C From 100°C To 125°C

ORDERING INFORMATION

MC14XXXBCP Plastic
MC14XXXBCL Ceramic
MC14XXXBD SOIC

$T_A = -55^\circ$ to 125° C for all packages.

6

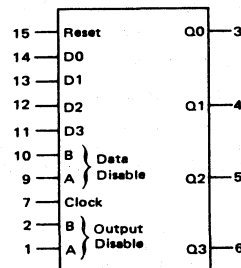
FUNCTION TABLE

INPUTS					OUTPUT Q
Reset	Clock	Data Disable		Data D	
		A	B		
1	X	X	X	X	0
0	0	X	X	X	Q_n
0		1	X	X	Q_n
0		X	1	X	Q_n
0		0	0	0	0
0		0	0	1	1

When either output disable A or B (or both) is (are) high the output is disabled to the high-impedance state; however sequential operation of the flip-flops is not affected.

X = Don't Care.

BLOCK DIAGRAM



V_{DD} = Pin 16
 V_{SS} = Pin 8

MC14076B

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V _{DD} V _d c	-55°C		25°C			125°C		Unit
			Min	Max	Min	Typ #	Max	Min	Max	
Output Voltage V _{in} = V _{DD} or 0	V _{OL}	5.0	—	0.05	—	0	0.05	—	0.05	V _d c
		10	—	0.05	—	0	0.05	—	0.05	
V _{in} = 0 or V _{DD}	V _{OH}	5.0	4.95	—	4.95	5.0	—	4.95	—	V _d c
		10	9.95	—	9.95	10	—	9.95	—	
Input Voltage (V _O = 4.5 or 0.5 V _d c) (V _O = 9.0 or 1.0 V _d c) (V _O = 13.5 or 1.5 V _d c)	V _{IL}	5.0	—	1.5	—	2.25	1.5	—	1.5	V _d c
		10	—	3.0	—	4.50	3.0	—	3.0	
(V _O = 0.5 or 4.5 V _d c) (V _O = 1.0 or 9.0 V _d c) (V _O = 1.5 or 13.5 V _d c)	V _{IH}	5.0	3.5	—	3.5	2.75	—	3.5	—	V _d c
		10	7.0	—	7.0	5.50	—	7.0	—	
Output Drive Current (V _{OH} = 2.5 V _d c) (V _{OH} = 4.6 V _d c) (V _{OH} = 9.5 V _d c) (V _{OH} = 13.5 V _d c)	I _{OH}	5.0	-3.0	—	-2.4	-4.2	—	-1.7	—	mA _d c
		5.0	-0.64	—	-0.51	-0.88	—	-0.36	—	
(V _{OL} = 0.4 V _d c) (V _{OL} = 0.5 V _d c) (V _{OL} = 1.5 V _d c)	I _{OL}	5.0	0.64	—	0.51	0.88	—	0.36	—	mA _d c
		10	1.6	—	1.3	2.25	—	0.9	—	
15	4.2	—	3.4	8.8	—	2.4	—	—		
Input Current	I _{in}	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	μA _d c
Input Capacitance (V _{in} = 0)	C _{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)	I _{DD}	5.0	—	5.0	—	0.005	5.0	—	150	μA _d c
		10	—	10	—	0.010	10	—	300	
15	—	20	—	—	—	0.015	20	—	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C _L = 50 pF on all outputs, all buffers switching)	I _T	5.0	I _T = (0.75 μA/kHz) f + I _{DD}							μA _d c
		10	I _T = (1.50 μA/kHz) f + I _{DD}							
15	I _T = (2.25 μA/kHz) f + I _{DD}									
Three-State Leakage Current	I _{TL}	15	—	±0.1	—	±0.00001	±0.1	—	±3.0	μA _d c

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) Vfk$$

where: I_T is in μA (per package), C_L in pF, V = (V_{DD} - V_{SS}) in volts, f in kHz is input frequency, and k = 0.002.

MC14076B

SWITCHING CHARACTERISTICS* ($C_L = 50 \text{ pF}$, $T_A = 25^\circ\text{C}$)

Characteristic	Symbol	V _{DD} Vdc	Min	Typ #	Max	Unit
Output Rise and Fall Time $t_{TLH}, t_{THL} = (1.5 \text{ ns/pF}) C_L + 25 \text{ ns}$ $t_{TLH}, t_{THL} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$ $t_{TLH}, t_{THL} = (0.55 \text{ ns/pF}) C_L + 9.5 \text{ ns}$	t_{TLH}, t_{THL}	5.0 10 15	— — —	100 50 40	200 100 80	ns
Propagation Delay Time Clock to Q $t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 215 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 92 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 65 \text{ ns}$ Reset to Q $t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 215 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 92 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 65 \text{ ns}$	t_{PLH}, t_{PHL}	5.0 10 15 5.0 10 15	— — — — — —	300 125 90 300 125 90	600 250 180 600 250 180	ns
3-State Propagation Delay, Output "1" or "0" to High Impedance	t_{PHZ}, t_{PLZ}	5.0 10 15	— — —	150 60 45	300 120 90	ns
3-State Propagation Delay, High Impedance to "1" or "0" Level	t_{PZH}, t_{PZL}	5.0 10 15	— — —	200 80 60	400 160 120	ns
Clock Pulse Width	t_{WH}	5.0 10 15	260 110 80	130 55 40	— — —	ns
Reset Pulse Width	t_{WH}	5.0 10 15	370 150 110	185 75 55	— — —	ns
Data Setup Time	t_{su}	5.0 10 15	30 10 4	15 5 2	— — —	ns
Data Hold Time	t_h	5.0 10 15	130 60 50	65 30 25	— — —	ns
Data Disable Setup Time	t_{su}	5.0 10 15	220 80 50	110 40 25	— — —	ns
Clock Pulse Rise and Fall Time	t_{TLH}, t_{THL}	5.0 10 15	— — —	— — —	15 5 4	μs
Clock Pulse Frequency	f_{cl}	5.0 10 15	— — —	3.6 9.0 12	1.8 4.5 6.0	MHz

*The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

MC14076B

FIGURE 1 - TIMING DIAGRAM

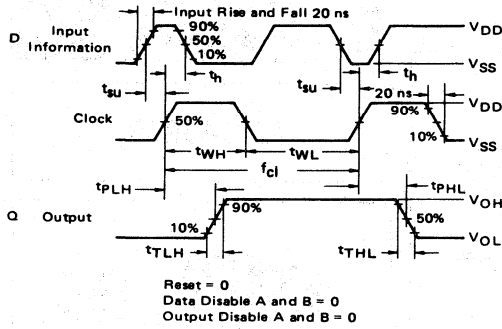
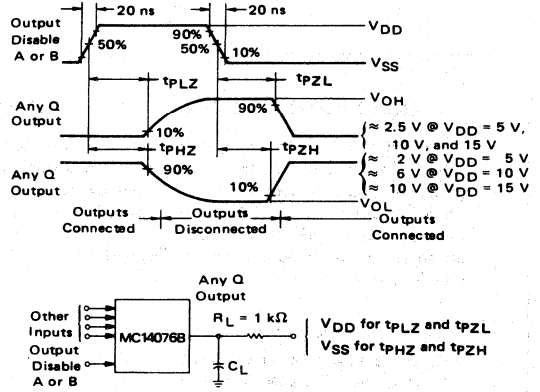
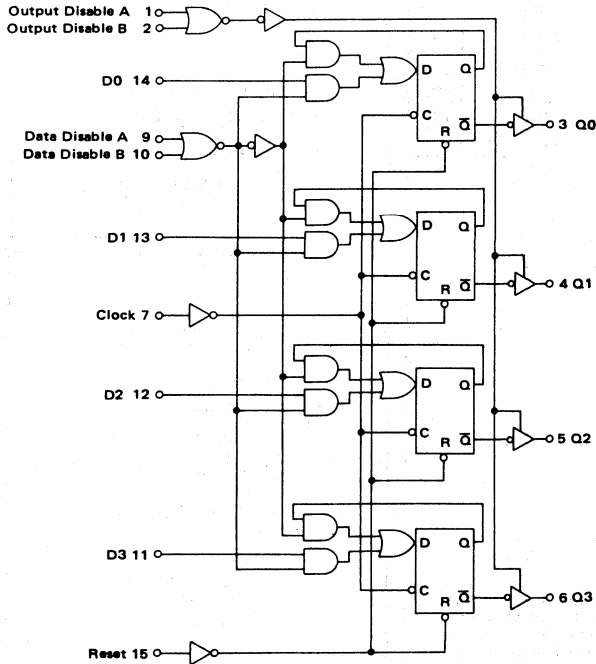


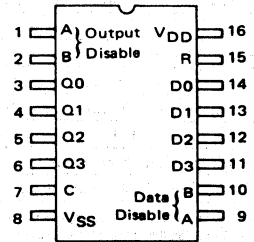
FIGURE 2 - THREE-STATE PROPAGATION DELAY WAVESHAVE AND CIRCUIT



EQUIVALENT
FUNCTIONAL BLOCK DIAGRAM



PIN ASSIGNMENT





MOTOROLA

MC14077B
See Page 6-160

**MC14078B, MC14081B,
MC14082B**
See Page 6-5

MC14093B

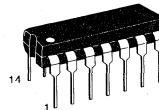
QUAD 2-INPUT "NAND" SCHMITT TRIGGER

The MC14093B Schmitt trigger is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These devices find primary use where low power dissipation and/or high noise immunity is desired. The MC14093B may be used in place of the MC14011B quad 2-input NAND gate for enhanced noise immunity or to "square up" slowly changing waveforms.

- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-Power TTL Loads or One Low-Power Schottky TTL Load Over the Rated Temperature Range
- Triple Diode Protection on All Inputs
- Pin-for-Pin Compatible with CD4093
- Can be Used to Replace MC14011B
- Independent Schmitt-Trigger at each Input



L SUFFIX
CERAMIC
CASE 632



P SUFFIX
PLASTIC
CASE 646



D SUFFIX
SOIC
CASE 751A

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V _{DD}	DC Supply Voltage	-0.5 to +18.0	V
V _{in} , V _{out}	Input or Output Voltage (DC or Transient)	-0.5 to V _{DD} + 0.5	V
I _{in} , I _{out}	Input or Output Current (DC or Transient), per Pin	± 10	mA
P _D	Power Dissipation, per Package†	500	mW
T _{stg}	Storage Temperature	-65 to +150	°C
T _L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
 †Temperature Derating: Plastic "P and D/DW" Packages: -7.0 mW/°C From 65°C To 125°C
 Ceramic "L" Packages: -12 mW/°C From 100°C To 125°C

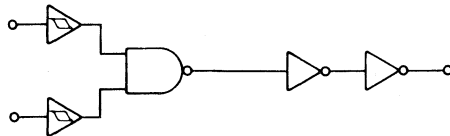
ORDERING INFORMATION

MC14XXXBCP Plastic
 MC14XXXBCL Ceramic
 MC14XXXBD SOIC

T_A = -55° to 125°C for all packages.

6

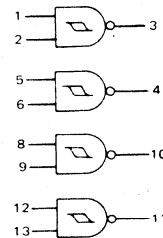
EQUIVALENT CIRCUIT SCHEMATIC (1/4 OF CIRCUIT SHOWN)



This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range V_{SS} ≤ (V_{in} or V_{out}) ≤ V_{DD}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

LOGIC DIAGRAM



V_{DD} = Pin 14
 V_{SS} = Pin 7

MC14093B

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V _{DD} Vdc	-55°C		25°C			125°C		Unit
			Min	Max	Min	Typ #	Max	Min	Max	
Output Voltage "0" Level V _{in} = V _{DD} or 0	V _{OL}	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
		10	—	0.05	—	0	0.05	—	0.05	
15		—	0.05	—	0	0.05	—	0.05		
V _{in} = 0 or V _{DD} "1" Level	V _{OH}	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc
		10	9.95	—	9.95	10	—	9.95	—	
		15	14.95	—	14.95	15	—	14.95	—	
Output Drive Current (V _{OH} = 2.5 Vdc) (V _{OH} = 4.6 Vdc) (V _{OH} = 9.5 Vdc) (V _{OH} = 13.5 Vdc) (V _{OL} = 0.4 Vdc) (V _{OL} = 0.5 Vdc) (V _{OL} = 1.5 Vdc)	Source I _{OH}	5.0	-3.0	—	-2.4	-4.2	—	-1.7	—	mAdc
		5.0	-0.64	—	-0.51	-0.88	—	-0.36	—	
		10	-1.6	—	-1.3	-2.25	—	-0.9	—	
		15	-4.2	—	-3.4	-8.8	—	-2.4	—	
	Sink I _{OL}	5.0	0.64	—	0.51	0.88	—	0.36	—	mAdc
		10	1.6	—	1.3	2.25	—	0.9	—	
15		4.2	—	3.4	8.8	—	2.4	—		
Input Current	I _{in}	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	μAdc
Input Capacitance (V _{in} = 0)	C _{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)	I _{DD}	5.0	—	0.25	—	0.0005	0.25	—	7.5	μAdc
		10	—	0.5	—	0.0010	0.5	—	15	
		15	—	1.0	—	0.0015	1.0	—	30	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C _L = 50 pF on all outputs, all buffers switching)	I _T	5.0	I _T = (1.2 μA/kHz) f + I _{DD}						μAdc	
		10	I _T = (2.4 μA/kHz) f + I _{DD}							
		15	I _T = (3.6 μA/kHz) f + I _{DD}							
Hysteresis Voltage	V _{HT}	5.0	0.3	2.0	0.3	1.1	2.0	0.3	2.0	Vdc
		10	1.2	3.4	1.2	1.7	3.4	1.2	3.4	
		15	1.6	5.0	1.6	2.1	5.0	1.6	5.0	
Threshold Voltage Positive-Going	V _{T+}	5.0	2.2	3.6	2.2	2.9	3.6	2.2	3.6	Vdc
		10	4.6	7.1	4.6	5.9	7.1	4.6	7.1	
		15	6.8	10.8	6.8	8.8	10.8	6.8	10.8	
Negative-Going	V _{T-}	5.0	0.9	2.8	0.9	1.9	2.8	0.9	2.8	Vdc
		10	2.5	5.2	2.5	3.9	5.2	2.5	5.2	
		15	4.0	7.4	4.0	5.8	7.4	4.0	7.4	

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) \text{ Vfk}$$

where: I_T is in μA (per package), C_L in pF, V = (V_{DD} - V_{SS}) in volts, f in kHz is input frequency, and k = 0.004.

MC14093B

SWITCHING CHARACTERISTICS (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V _{DD} Vdc	Min	Typ #	Max	Unit
Output Rise Time	t _{TLH}	5.0	—	100	200	ns
		10	—	50	100	
		15	—	40	80	
Output Fall Time	t _{THL}	5.0	—	100	200	ns
		10	—	50	100	
		15	—	40	80	
Propagation Delay Time	t _{PLH} , t _{PHL}	5.0	—	125	250	ns
		10	—	50	100	
		15	—	40	80	

#Data labeled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

FIGURE 1 – SWITCHING TIME TEST CIRCUIT AND WAVE FORMS

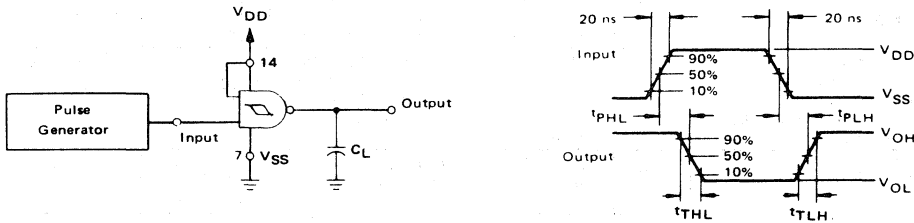
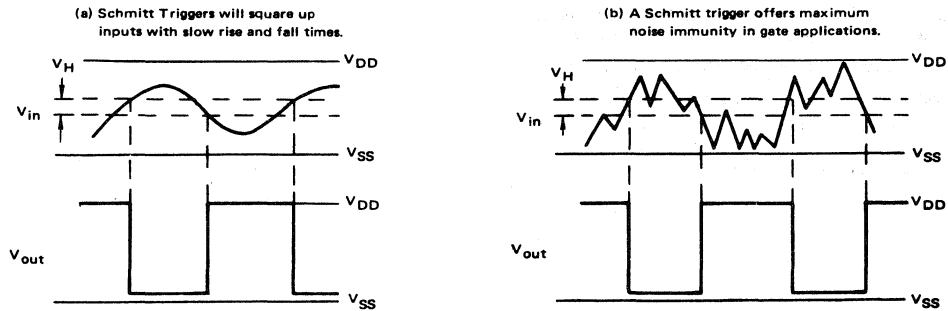


FIGURE 2 – TYPICAL SCHMITT TRIGGER APPLICATIONS



MC14093B

FIGURE 3 – TYPICAL OUTPUT SOURCE CHARACTERISTICS TEST CIRCUIT

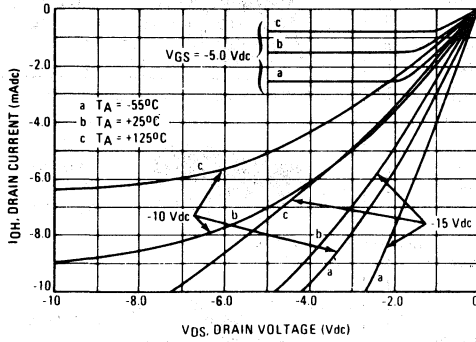
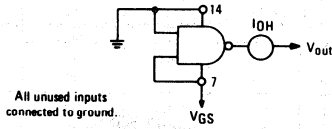


FIGURE 4 – TYPICAL OUTPUT SINK CHARACTERISTICS TEST CIRCUIT

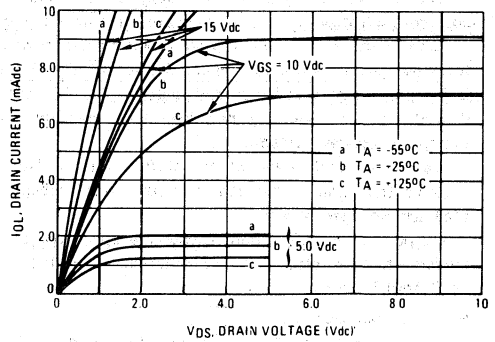
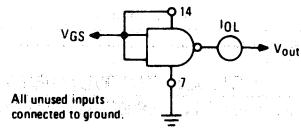
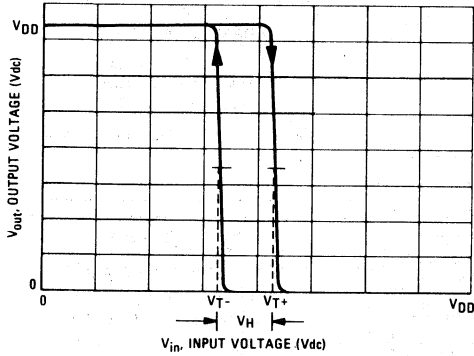
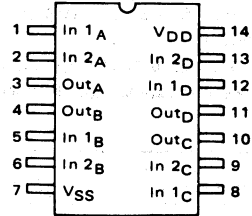


FIGURE 5 – TYPICAL TRANSFER CHARACTERISTICS



PIN ASSIGNMENT





MOTOROLA

MC14094B

**8-STAGE SHIFT/STORE REGISTER
WITH THREE-STATE OUTPUTS**

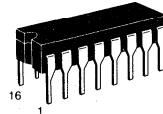
The MC14094B combines an 8-stage shift register with a data latch for each stage and a three-state output from each latch.

Data is shifted on the positive clock transition and is shifted from the seventh stage to two serial outputs. The Q_S output data is for use in high-speed cascaded systems. The Q'_S output data is shifted on the following negative clock transition for use in low-speed cascaded systems.

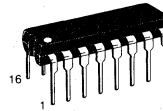
Data from each stage of the shift register is latched on the negative transition of the strobe input. Data propagates through the latch while strobe is high.

Outputs of the eight data latches are controlled by three-state buffers which are placed in the high-impedance state by a logic Low on Output Enable.

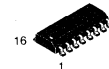
- Three-State Outputs
- Capable of Driving Two Low-Power TTL Loads or One Low-Power Schottky TTL Load Over the Rated Temperature Range
- Input Diode Protection
- Data Latch
- Dual Outputs for Data Out on Both Positive and Negative Clock Transitions
- Useful for Serial-to-Parallel Data Conversion
- Pin-for-Pin Compatible with CD4094B



L SUFFIX
CERAMIC
CASE 620



P SUFFIX
PLASTIC
CASE 648



D SUFFIX
SOIC
CASE 751B

ORDERING INFORMATION

- MC14XXXBCP Plastic
- MC14XXXBCL Ceramic
- MC14XXXBD SOIC

T_A = -55° to 125°C for all packages.

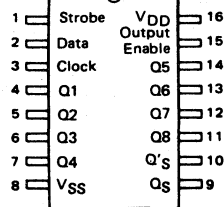
MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V _{DD}	DC Supply Voltage	-0.5 to +18.0	V
V _{in} , V _{out}	Input or Output Voltage (DC or Transient)	-0.5 to V _{DD} + 0.5	V
I _{in} , I _{out}	Input or Output Current (DC or Transient), per Pin	± 10	mA
P _D	Power Dissipation, per Package†	500	mW
T _{stg}	Storage Temperature	-65 to +150	°C
T _L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.

†Temperature Derating: Plastic "P and D/DW" Packages: -7.0 mW/°C From 65°C To 125°C
Ceramic "L" Packages: -12 mW/°C From 100°C To 125°C

PIN ASSIGNMENT



6

Clock	Output Enable	Strobe	Data	Parallel Outputs		Serial Outputs	
				Q ₁	Q _N	Q _S *	Q' _S
	0	X	X	Z	Z	Q ₇	No Chg.
	0	X	X	Z	Z	No Chg.	Q ₇
	1	0	X	No Chg.	No Chg.	Q ₇	No Chg.
	1	1	0	0	Q _N -1	Q ₇	No Chg.
	1	1	1	1	Q _N -1	Q ₇	No Chg.
	1	1	1	No Chg.	No Chg.	No Chg.	Q ₇

Z = High Impedance

X = Don't Care

*At the positive clock edge, information in the 7th shift register stage is transferred to Q₈ and Q_S.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range V_{SS} ≤ (V_{in} or V_{out}) ≤ V_{DD}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

MC14094B

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V _{DD} V _{dC}	-55°C		25°C			125°C		Unit	
			Min	Max	Min	Typ #	Max	Min	Max		
Output Voltage V _{in} = V _{DD} or 0	V _{OL}	5.0	—	0.05	—	0	0.05	—	0.05	V _{dC}	
		10	—	0.05	—	0	0.05	—	0.05		
V _{in} = 0 or V _{DD}	V _{OH}	5.0	4.95	—	4.95	5.0	—	4.95	—	V _{dC}	
		10	9.95	—	9.95	10	—	9.95	—		
Input Voltage (V _O = 4.5 or 0.5 V _{dC}) (V _O = 9.0 or 1.0 V _{dC}) (V _O = 13.5 or 1.5 V _{dC})	V _{IL}	5.0	—	1.5	—	2.25	1.5	—	1.5	V _{dC}	
		10	—	3.0	—	4.50	3.0	—	3.0		
(V _O = 0.5 or 4.5 V _{dC}) (V _O = 1.0 or 9.0 V _{dC}) (V _O = 1.5 or 13.5 V _{dC})	V _{IH}	5.0	3.5	—	3.5	2.75	—	3.5	—	V _{dC}	
		10	7.0	—	7.0	5.50	—	7.0	—		
Output Drive Current (V _{OH} = 2.5 V _{dC}) (V _{OH} = 4.6 V _{dC}) (V _{OH} = 9.5 V _{dC}) (V _{OH} = 13.5 V _{dC})	Source	I _{OH}	5.0	-3.0	—	-2.4	-4.2	—	-1.7	—	mAdc
	Sink		5.0	-0.64	—	-0.51	-0.88	—	-0.36	—	
(V _{OL} = 0.4 V _{dC}) (V _{OL} = 0.5 V _{dC}) (V _{OL} = 1.5 V _{dC})		I _{OL}	10	-1.6	—	-1.3	-2.25	—	-0.9	—	mAdc
	15		-4.2	—	-3.4	-8.8	—	-2.4	—		
Input Current	I _{in}	15	—	±0.1	—	±0.0001	±0.1	—	±1.0	μAdc	
Input Capacitance (V _{in} = 0)	C _{in}	—	—	—	—	5.0	7.5	—	—	pF	
Quiescent Current (Per Package)	I _{DD}	5.0	—	5.0	—	0.005	5.0	—	150	μAdc	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C _L = 50 pF on all outputs, all buffers switching)	I _T	10	—	10	—	0.010	10	—	300		
		15	—	20	—	0.015	20	—	600		
3-State Output Leakage Current	I _{TL}	15	—	±0.1	—	±0.0001	±0.1	—	±3.0	μA	

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) \text{ V/k}$$

where: I_T is in μA (per package), C_L in pF, V = (V_{DD} - V_{SS}) in volts, f in kHz is input frequency, and k = 0.001.

MC14094B

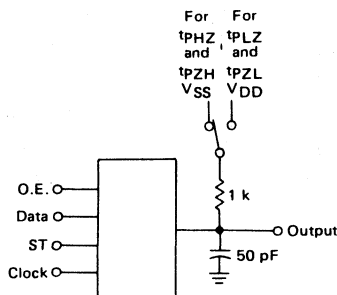
SWITCHING CHARACTERISTICS* ($C_L = 50 \text{ pF}$, $T_A = 25^\circ\text{C}$)

Characteristic	Symbol	V _{DD} V _{dc}	Min	Typ #	Max	Unit	
Output Rise and Fall Time $t_{TLH}, t_{THL} = (1.35 \text{ ns/pF}) C_L + 33 \text{ ns}$ $t_{TLH}, t_{THL} = (0.6 \text{ ns/pF}) C_L + 20 \text{ ns}$ $t_{TLH}, t_{THL} = (0.4 \text{ ns/pF}) C_L + 20 \text{ ns}$	$t_{TLH},$ t_{THL}	5.0	—	100	200	ns	
		10	—	50	100		
		15	—	40	80		
Propagation Delay Time Clock to Serial out QS $t_{PLH}, t_{PHL} = (0.90 \text{ ns/pF}) C_L + 305 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.36 \text{ ns/pF}) C_L + 107 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.26 \text{ ns/pF}) C_L + 82 \text{ ns}$ Clock to Serial out Q'S $t_{PLH}, t_{PHL} = (0.90 \text{ ns/pF}) C_L + 350 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.36 \text{ ns/pF}) C_L + 149 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.26 \text{ ns/pF}) C_L + 62 \text{ ns}$ Clock to Parallel out $t_{PLH}, t_{PHL} = (0.90 \text{ ns/pF}) C_L + 375 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.35 \text{ ns/pF}) C_L + 177 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.26 \text{ ns/pF}) C_L + 122 \text{ ns}$ Strobe to Parallel out $t_{PLH}, t_{PHL} = (0.90 \text{ ns/pF}) C_L + 245 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.36 \text{ ns/pF}) C_L + 87 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.26 \text{ ns/pF}) C_L + 87 \text{ ns}$ Output Enable to Output $t_{PHZ}, t_{PZL} = (0.90 \text{ ns/pF}) C_L + 95 \text{ ns}$ $t_{PHZ}, t_{PZL} = (0.36 \text{ ns/pF}) C_L + 57 \text{ ns}$ $t_{PHZ}, t_{PZL} = (0.26 \text{ ns/pF}) C_L + 42 \text{ ns}$ $t_{PLZ}, t_{PZH} = (0.90 \text{ ns/pF}) C_L + 180 \text{ ns}$ $t_{PLZ}, t_{PZH} = (0.36 \text{ ns/pF}) C_L + 77 \text{ ns}$ $t_{PLZ}, t_{PZH} = (0.26 \text{ ns/pF}) C_L + 57 \text{ ns}$	$t_{PLH},$ t_{PHL}	5.0	—	350	600	ns	
		10	—	125	250		
		15	—	95	190		
		5.0	—	230	460		
		10	—	110	220		
		15	—	75	150		
		5.0	—	420	840		
		10	—	195	390		
		15	—	135	270		
		5.0	—	290	580		
	10	—	145	290			
	15	—	100	200			
		$t_{PHZ},$ t_{PZL}	5.0	—	140	280	
	10		—	75	150		
	15		—	55	110		
		$t_{PLZ},$ t_{PZH}	5.0	—	225	450	
	10		—	95	190		
	15		—	70	140		
	Setup Time Data in to Clock	t_{su}	5.0	125	60	—	ns
			10	55	30	—	
15			35	20	—		
Hold Time Clock to Data	t_h	5.0	0	-40	—	ns	
		10	20	-10	—		
		15	20	0	—		
Clock Pulse Width, High	t_{WH}	5.0	200	100	—	ns	
		10	100	50	—		
		15	83	40	—		
Clock Rise and Fall Time	$t_{r(cl)}$ $t_{f(cl)}$	5	—	—	15	μs	
		10	—	—	5.0		
		15	—	—	4.0		
Clock Pulse Frequency	f_{cl}	5.0	—	2.5	1.25	MHz	
		10	—	5.0	2.5		
		15	—	6.0	3.0		
Strobe Pulse Width	t_{WL}	5.0	200	100	—	ns	
		10	80	40	—		
		15	70	35	—		

*The formulas given are for the typical characteristics only at 25°C.

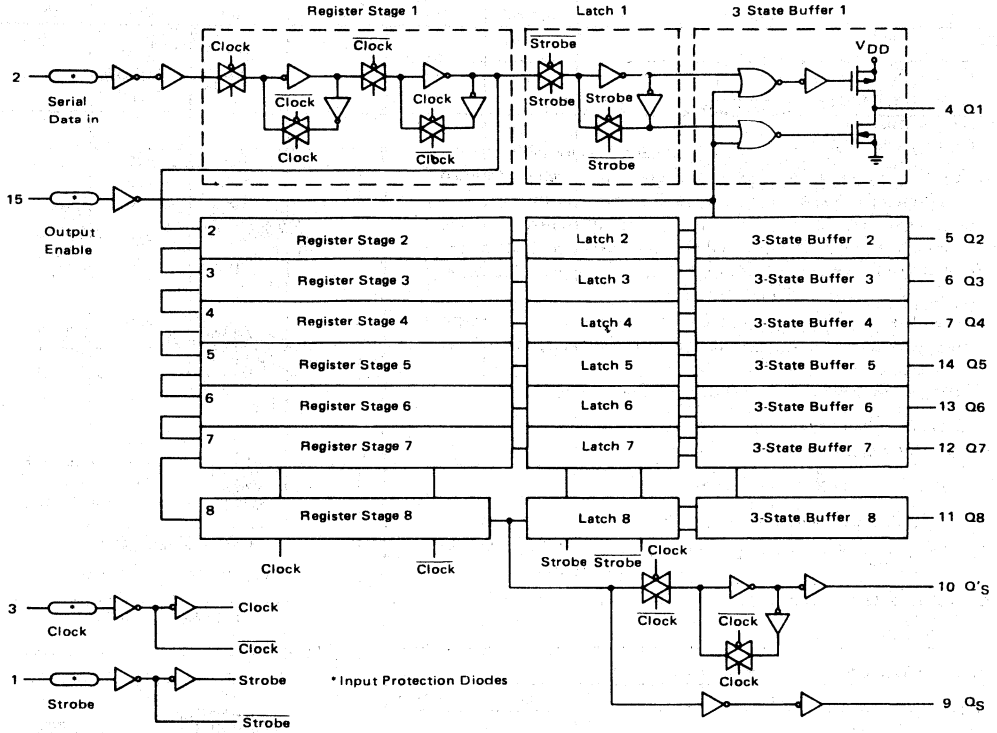
#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

3-STATE TEST CIRCUIT

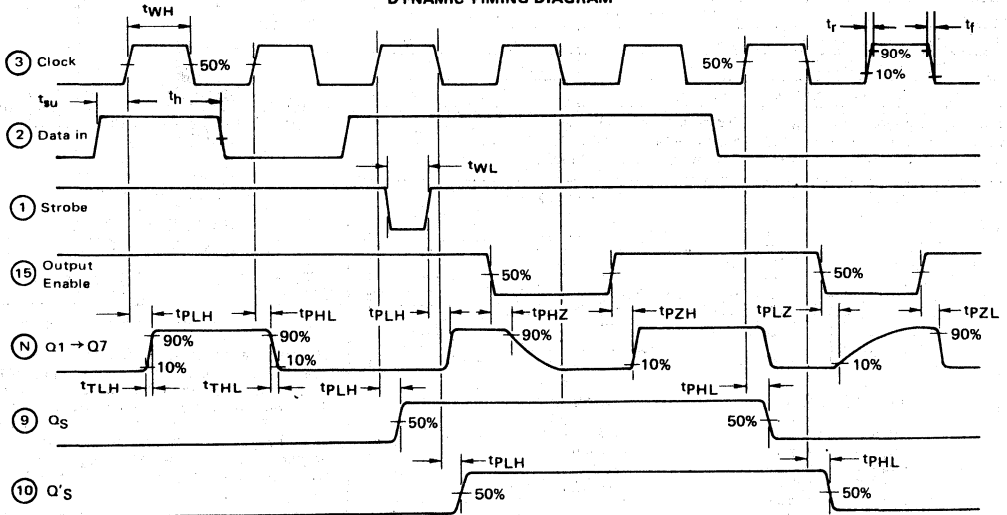


MC14094B

BLOCK DIAGRAM



DYNAMIC TIMING DIAGRAM





MOTOROLA

MC14097B
See Page 150

MC14099B
MC14599B

8-BIT ADDRESSABLE LATCHES

The MC14099B and MC14599B are 8-bit addressable latches. Data is entered in serial form when the appropriate latch is addressed (via address pins A0, A1, A2) and write disable is in the low state. Chip enable must be high for writing into MC14599B. For the MC14599B the data pin is a bidirectional data port and for the MC14099B the input is a unidirectional write only port. The Write/Read line controls this port in the MC14599B.

The data is presented in parallel at the output of the eight latches independently of the state of Write Disable, Write/Read or Chip Enable.

A Master Reset capability is available on both parts.

- Serial Data Input
- Parallel Output
- Master Reset
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-Power Schottky TTL Load over the Rated Temperature Range
- MC14099B pin for pin compatible with CD4099B

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

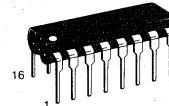
Symbol	Parameter	Value	Unit
V _{DD}	DC Supply Voltage	-0.5 to +18.0	V
V _{in} , V _{out}	Input or Output Voltage (DC or Transient)	-0.5 to V _{DD} + 0.5	V
I _{in} , I _{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
P _D	Power Dissipation, per Package†	500	mW
T _{stg}	Storage Temperature	-65 to +150	°C
T _L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.

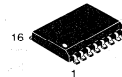
†Temperature Derating: Plastic "P and D/DW" Packages: -7.0 mW/°C From 65°C To 125°C
Ceramic "L" Packages: -12 mW/°C From 100°C To 125°C



L SUFFIX
CERAMIC
CASE 620



P SUFFIX
PLASTIC
CASE 648

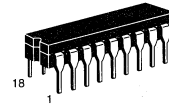


DW SUFFIX
SOIC
CASE 751G

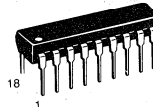
ORDERING INFORMATION

MC14099BCP Plastic
MC14099BCL Ceramic
MC14099BDW SOIC

T_A = -55°C to +125°C for all packages.



L SUFFIX
CERAMIC PACKAGE
CASE 726



P SUFFIX
PLASTIC PACKAGE
CASE 707

ORDERING INFORMATION

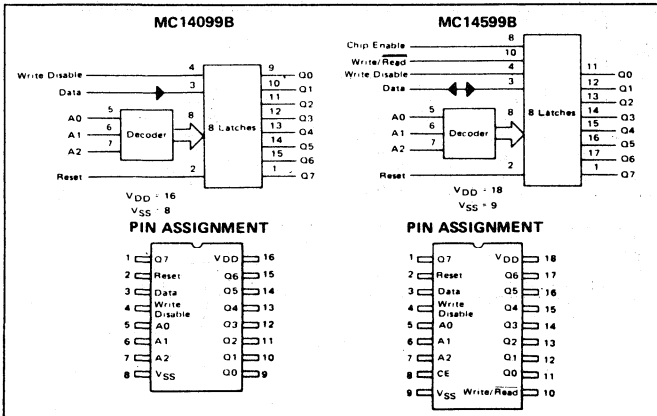
MC14599BCP Plastic
MC14599BCL Ceramic

T_A = -55°C to +125°C for all packages.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range V_{SS} ≤ (V_{in} or V_{out}) ≤ V_{DD}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

6



MC14099B•MC14599B

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V _{DD} V _{dC}	-55°C		25°C			125°C		Unit
			Min	Max	Min	Typ #	Max	Min	Max	
Output Voltage V _{in} = V _{DD} or 0	V _{OL}	5.0	—	0.05	—	0	0.05	—	0.05	V _{dC}
		10	—	0.05	—	0	0.05	—	0.05	
V _{in} = 0 or V _{DD}	V _{OH}	5.0	4.95	—	4.95	5.0	—	4.95	—	V _{dC}
		10	9.95	—	9.95	10	—	9.95	—	
Input Voltage (V _O = 4.5 or 0.5 V _{dC}) (V _O = 9.0 or 1.0 V _{dC}) (V _O = 13.5 or 1.5 V _{dC})	V _{IL}	5.0	—	1.5	—	2.25	1.5	—	1.5	V _{dC}
		10	—	3.0	—	4.50	3.0	—	3.0	
(V _O = 0.5 or 4.5 V _{dC}) (V _O = 1.0 or 9.0 V _{dC}) (V _O = 1.5 or 13.5 V _{dC})	V _{IH}	5.0	3.5	—	3.5	2.75	—	3.5	—	V _{dC}
		10	7.0	—	7.0	5.50	—	7.0	—	
Output Drive Current (V _{OH} = 2.5 V _{dC}) (V _{OH} = 4.6 V _{dC}) (V _{OH} = 9.5 V _{dC}) (V _{OH} = 13.5 V _{dC})	I _{OH}	5.0	-3.0	—	-2.4	-4.2	—	-1.7	—	mAdc
		5.0	-0.64	—	-0.51	-0.88	—	-0.36	—	
(V _{OL} = 0.4 V _{dC}) (V _{OL} = 0.5 V _{dC}) (V _{OL} = 1.5 V _{dC})	I _{OL}	5.0	0.64	—	0.51	0.88	—	0.36	—	mAdc
		10	1.6	—	1.3	2.25	—	0.9	—	
		15	4.2	—	3.4	8.8	—	2.4	—	
Input Current	I _{in}	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	μAdc
Input Capacitance (V _{in} = 0)	C _{in}	—	—	—	—	5.0	7.5	—	—	pF
Input Capacitance MC14599B — Data (pin 3) (V _{in} = 0)	C _{in}	—	—	—	—	15	22.5	—	—	pF
Quiescent Current (Per Package)	I _{DD}	5.0	—	5.0	—	0.005	5.0	—	150	μAdc
		10	—	10	—	0.010	10	—	300	
		15	—	20	—	0.015	20	—	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C _L = 50 pF on all outputs, all buffers switching)	I _T	5.0	I _T = (1.5 μA/kHz) f + I _{DD} I _T = (3.0 μA/kHz) f + I _{DD} I _T = (4.5 μA/kHz) f + I _{DD}						150	μAdc
		10							300	
		15							600	

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) V/k$$

where: I_T is in μA (per package), C_L in pF, V = (V_{DD} - V_{SS}) in volts, f in kHz is input frequency, and k = 0.004.

MC14099B•MC14599B

SWITCHING CHARACTERISTICS* ($C_L = 50 \text{ pF}$, $T_A = 25^\circ\text{C}$)

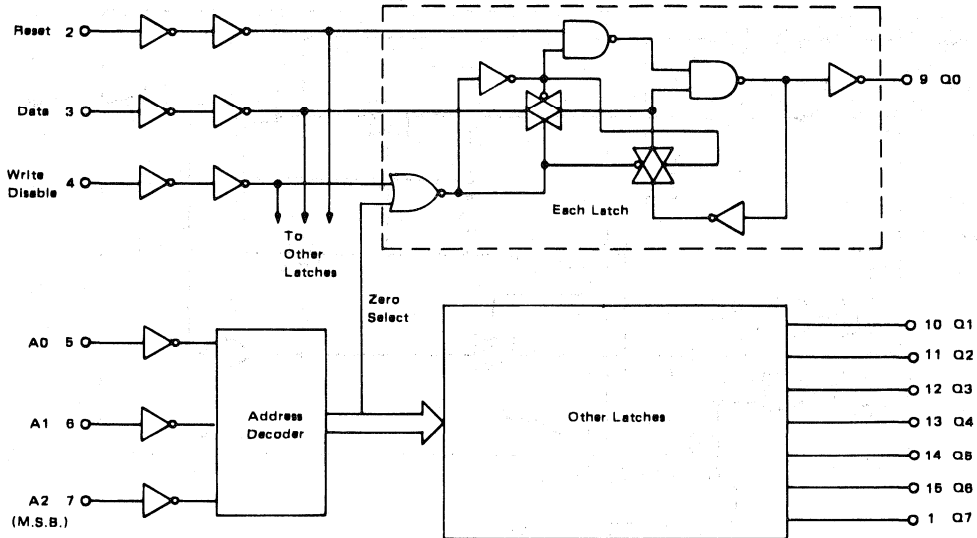
Characteristic	Symbol	V _{DD} V _{dC}	Min	Typ. #	Max	Unit
Output Rise and Fall Time $t_{TLH}, t_{THL} = (1.35 \text{ ns/pF}) C_L + 32 \text{ ns}$ $t_{TLH}, t_{THL} = (0.6 \text{ ns/pF}) C_L + 20 \text{ ns}$ $t_{TLH}, t_{THL} = (0.4 \text{ ns/pF}) C_L + 20 \text{ ns}$	t_{TLH} , t_{THL}	5.0 10 15	— — —	100 50 40	200 100 80	ns
Propagation Delay Time Data to Output Q	t_{PHL} , t_{PLH}	5.0 10 15	— — —	200 75 50	400 150 100	ns
Write Disable to Output Q		5.0 10 15	— — —	200 80 60	400 180 120	ns
Reset to Output Q		5.0 10 15	— — —	175 80 65	350 160 130	ns
CE to Output Q (MC14599B only)		5.0 10 15	— — —	225 100 75	450 200 150	ns
Propagation Delay Time, MC14599B only Chip Enable, Write/Read to Data	t_{PHL} , t_{PLH}	5.0 10 15	— — —	200 80 65	400 160 130	ns
Address to Data		5.0 10 15	— — —	200 90 75	400 180 150	ns
Pulse Widths Reset	$t_{w(H)}$ $t_{w(L)}$	5.0 10 15	150 75 50	75 40 25	— — —	ns
Write Disable		5.0 10 15	320 160 120	160 80 60	— — —	ns
Set Up Time Data to Write Disable	t_{su}	5.0 10 15	100 50 35	50 25 20	— — —	ns
Hold Time Write Disable to Data	t_h	5.0 10 15	150 75 50	75 40 25	— — —	ns
Set Up Time Address to Write Disable	t_{su}	5.0 10 15	100 80 40	45 30 10	— — —	ns
Removal Time Write Disable to Address	t_{rem}	5.0 10 15	0 0 0	-80 -40 -40	— — —	ns

*The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

MC14099B • MC14599B

MC14099B
FUNCTION DIAGRAM



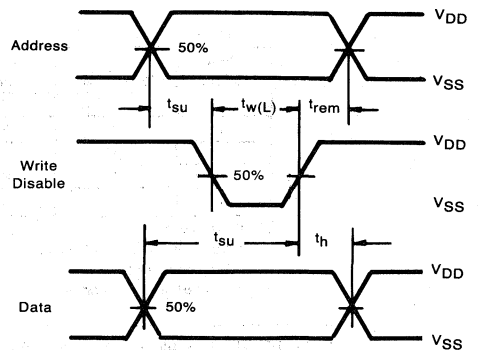
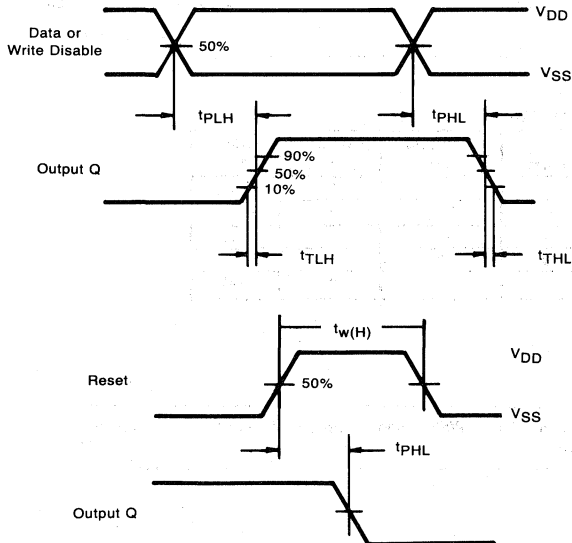
TRUTH TABLE

Write Disable	Reset	Addressed Latch	Unaddressed Latches
0	0	Data	Q_n^*
0	1	Data	Reset [†]
1	0	Q_n^*	Q_n^*
1	1	Reset	Reset

* Q_n is previous state of latch.
† Reset to zero state.

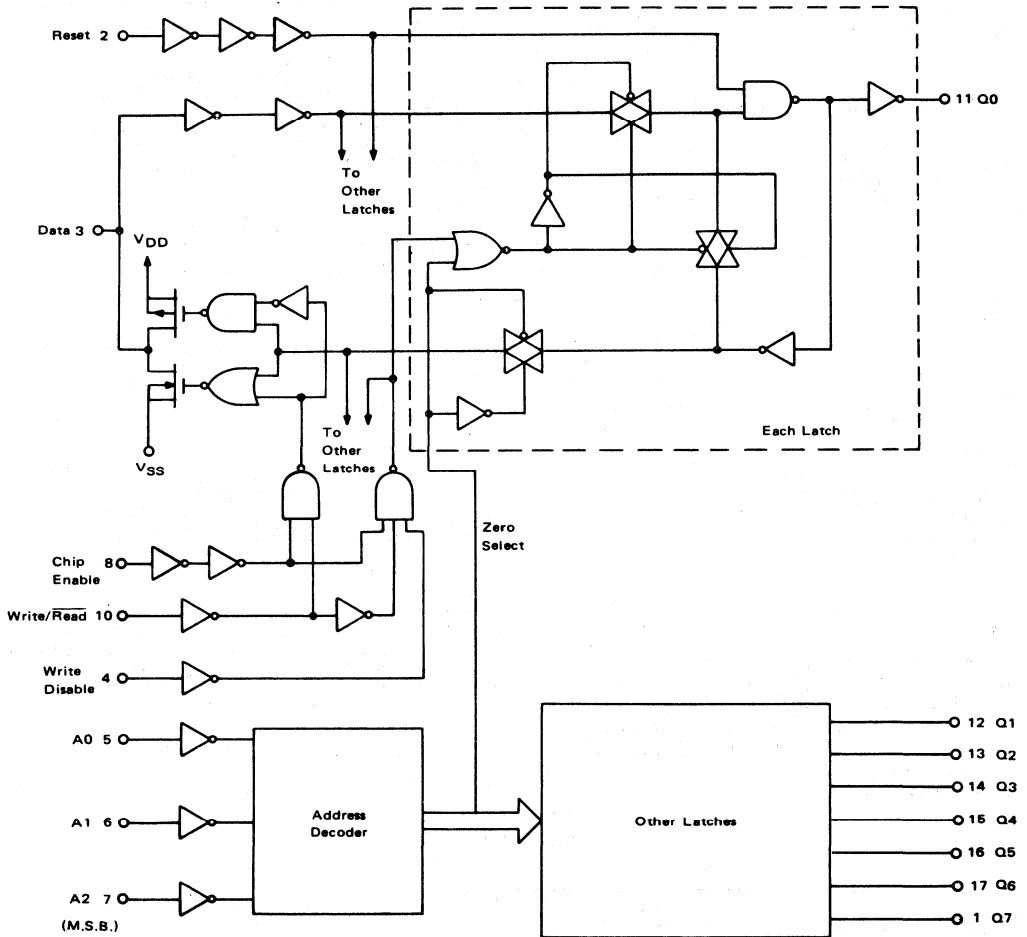
CAUTION: To avoid unintentional data changes in the latches, Write Disable must be active (high) during transitions on the address inputs A0, A1, and A2.

SWITCHING WAVEFORMS



MC14099B•MC14599B

MC14599B
FUNCTION DIAGRAM



TRUTH TABLE

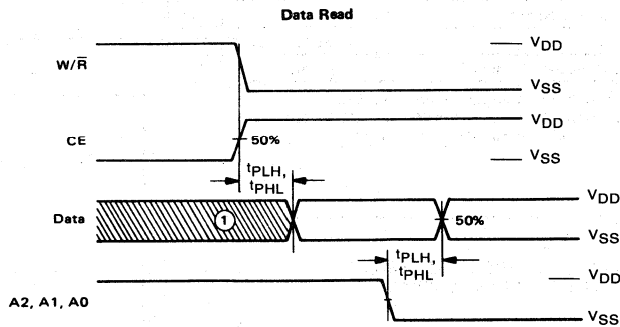
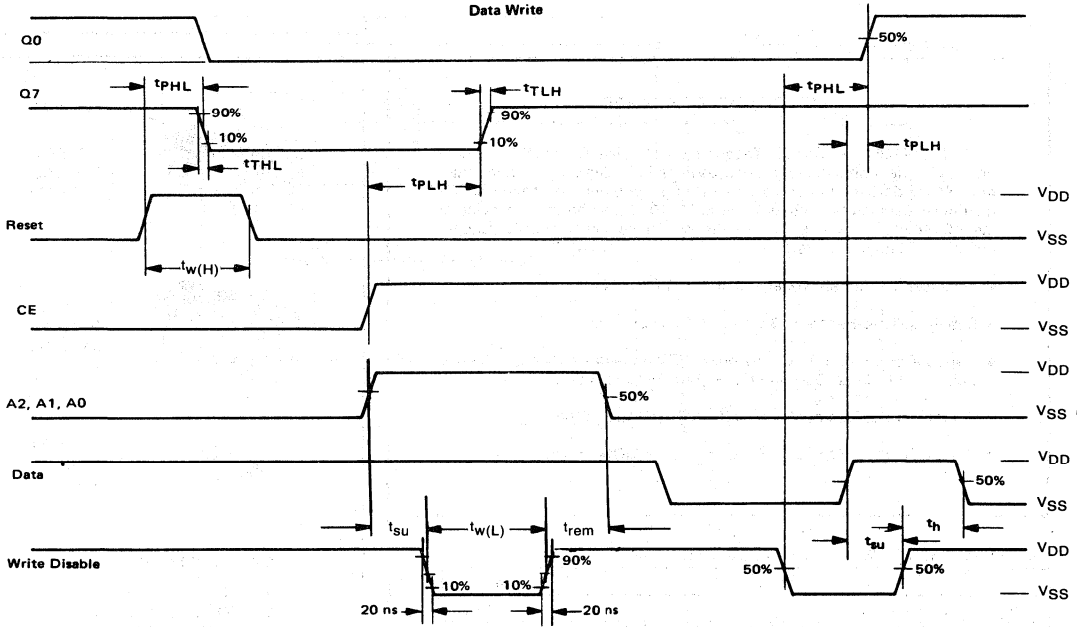
Chip Enable	Write/Read	Write Disable	Reset	Addressed Latch	Other Latches	Data Pin
0	X	X	0	*	*	Z
1	1	0	0	Data	*	Input
1	1	1	0	*	*	Z
1	0	X	0	*	*	Q _n
X	X	X	1	0	0	Z/0

X = Don't care.
 * = No change in state of latch.
 Z = High impedance.
 Q_n = State of addressed latch.

CAUTION: To avoid unintentional data changes in the latches, Write Disable must be active (high) during transitions on the address inputs A0, A1, and A2.

MC14099B•MC14599B

MC14599B SWITCHING WAVEFORMS



NOTE: 1. Invalid Data Output
2. Reset in LOW State



MOTOROLA

MC14106B

HEX SCHMITT TRIGGER

The MC14106B hex Schmitt Trigger is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These devices find primary use where low power dissipation and/or high noise immunity is desired. The MC14106B may be used in place of the MC14069UB hex inverter for enhanced noise immunity or to "square up" slowly changing waveforms.

- Increased Hysteresis Voltage Over the MC14584B
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range
- Pin-for-Pin Replacement for CD40106B and MM74C14
- Can Be Used to Replace the MC14584B or MC14069UB



L SUFFIX
CERAMIC
CASE 632



P SUFFIX
PLASTIC
CASE 646



D SUFFIX
SOIC
CASE 751A

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V _{DD}	DC Supply Voltage	-0.5 to +18.0	V
V _{in} , V _{out}	Input or Output Voltage (DC or Transient)	-0.5 to V _{DD} + 0.5	V
I _{in} , I _{out}	Input or Output Current (DC or Transient), per Pin	± 10	mA
P _D	Power Dissipation, per Package†	500	mW
T _{stg}	Storage Temperature	-65 to +150	°C
T _L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P and D/DW" Packages: -7.0 mW/°C From 65°C To 125°C
Ceramic "L" Packages: -12 mW/°C From 100°C To 125°C

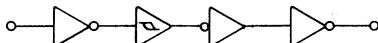
ORDERING INFORMATION

MC14XXXBCP Plastic
MC14XXXBCL Ceramic
MC14XXXBD SOIC

T_A = -55° to 125°C for all packages.

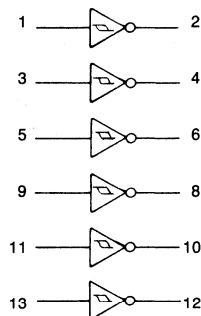
6

EQUIVALENT CIRCUIT SCHEMATIC (1/6 OF CIRCUIT SHOWN)



This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range V_{SS} ≤ (V_{in} or V_{out}) ≤ V_{DD}. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

LOGIC DIAGRAM



V_{DD} = Pin 14
V_{SS} = Pin 7

MC14106B

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V _{DD} Vdc	-55°C		25°C			125°C		Unit
			Min	Max	Min	Typ #	Max	Min	Max	
Output Voltage V _{in} = V _{DD} V _{in} = 0	"0" Level V _{OL}	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
		10	—	0.05	—	0	0.05	—	0.05	
		15	—	0.05	—	0	0.05	—	0.05	
	"1" Level V _{OH}	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc
		10	9.95	—	9.95	10	—	9.95	—	
		15	14.95	—	14.95	15	—	14.95	—	
Hysteresis Voltage	V _{H†}	5.0	0.3	2.0	0.3	1.1	2.0	0.3	2.0	Vdc
		10	1.2	3.4	1.2	1.7	3.4	1.2	3.4	
		15	1.6	5.0	1.6	2.1	5.0	1.6	5.0	
Threshold Voltage Positive-Going Negative-Going	V _{T+}	5.0	2.2	3.6	2.2	2.9	3.6	2.2	3.6	Vdc
		10	4.6	7.1	4.6	5.9	7.1	4.6	7.1	
		15	6.8	10.8	6.8	8.8	10.8	6.8	10.8	
	V _{T-}	5.0	0.9	2.8	0.9	1.9	2.8	0.9	2.8	Vdc
		10	2.5	5.2	2.5	3.9	5.2	2.5	5.2	
		15	4.0	7.4	4.0	5.8	7.4	4.0	7.4	
Output Drive Current (V _{OH} = 2.5 Vdc) (V _{OH} = 4.6 Vdc) (V _{OH} = 9.5 Vdc) (V _{OH} = 13.5 Vdc) (V _{OL} = 0.4 Vdc) (V _{OL} = 0.5 Vdc) (V _{OL} = 1.5 Vdc)	Source I _{OH}	5.0	-3.0	—	-2.4	-4.2	—	-1.7	—	mAdc
		10	-0.64	—	-0.51	-0.88	—	-0.36	—	
		15	-1.6	—	-1.3	-2.25	—	-0.9	—	
	Sink I _{OL}	5.0	0.64	—	0.51	0.88	—	0.36	—	mAdc
		10	1.6	—	1.3	2.25	—	0.9	—	
		15	4.2	—	3.4	8.8	—	2.4	—	
Input Current	I _{in}	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	μAdc
Input Capacitance (V _{in} = 0)	C _{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)	I _{DD}	5.0	—	0.25	—	0.0005	0.25	—	7.5	μAdc
		10	—	0.5	—	0.0010	0.5	—	15	
		15	—	1.0	—	0.0015	1.0	—	30	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C _L = 50 pF on all outputs, all buffers switching)	I _T	5.0	I _T = (1.8 μA/kHz) f + I _{DD}							μAdc
		10	I _T = (3.6 μA/kHz) f + I _{DD}							
		15	I _T = (5.4 μA/kHz) f + I _{DD}							

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) \text{ V/k}$$

where: I_T is in μA (per package), C_L in pF, V = (V_{DD} - V_{SS}) in volts, f in kHz is input frequency, and k = 0.001.

†V_H = V_{T+} - V_{T-} (But maximum variation of V_H is specified as less than V_{T+max} - V_{T-min}).

MC14106B

SWITCHING CHARACTERISTICS ($C_L = 50 \text{ pF}$, $T_A = 25^\circ\text{C}$)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ #	Max	Unit
Output Rise Time	t_{TLH}	5.0	—	100	200	ns
		10	—	50	100	
		15	—	40	80	
Output Fall Time	t_{THL}	5.0	—	100	200	ns
		10	—	50	100	
		15	—	40	80	
Propagation Delay Time	t_{PLH} , t_{PHL}	5.0	—	125	250	ns
		10	—	50	100	
		15	—	40	80	

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

FIGURE 1 — SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

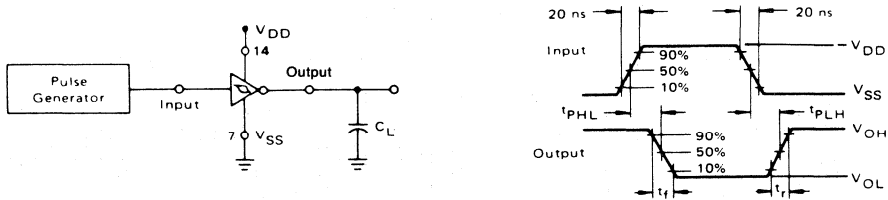
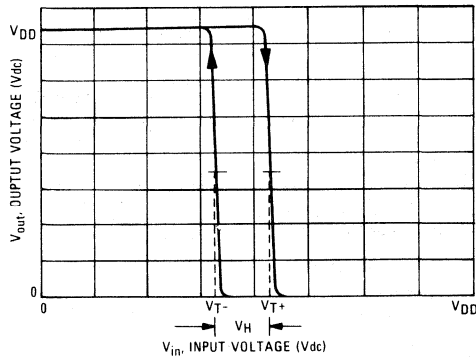
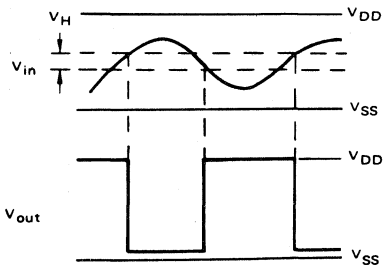


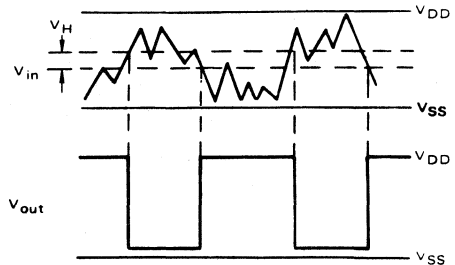
FIGURE 2 — TYPICAL TRANSFER CHARACTERISTICS



APPLICATIONS



(a) Schmitt Triggers will square up inputs with slow rise and fall times.

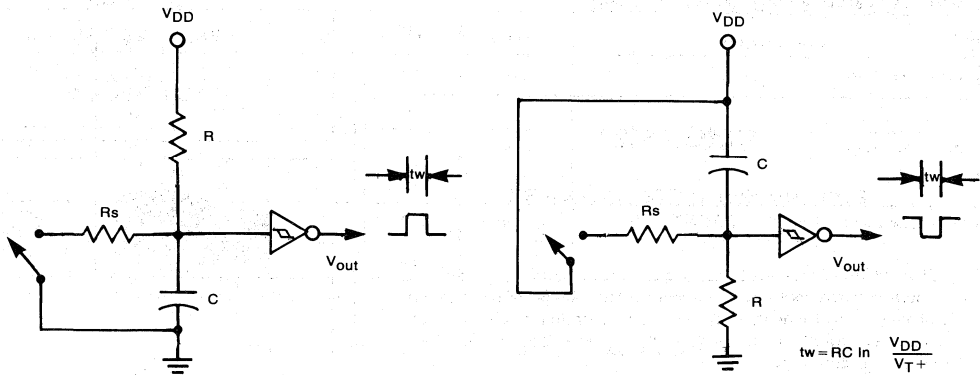


(b) A Schmitt trigger offers maximum noise immunity in gate applications.

FIGURE 3

MC14106B

FIGURE 4 — MONOSTABLE MULTIVIBRATOR



Useful as Pushbutton/Keyboard Debounce Circuit.

FIGURE 5 — ASTABLE MULTIVIBRATOR

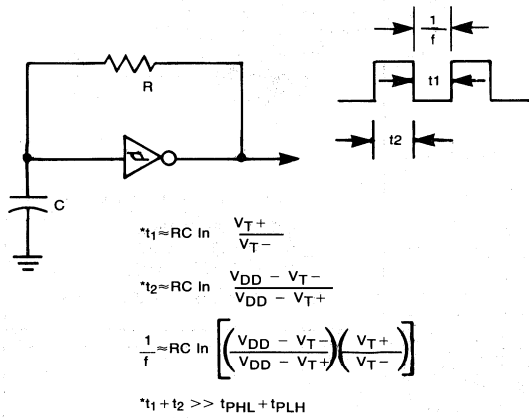
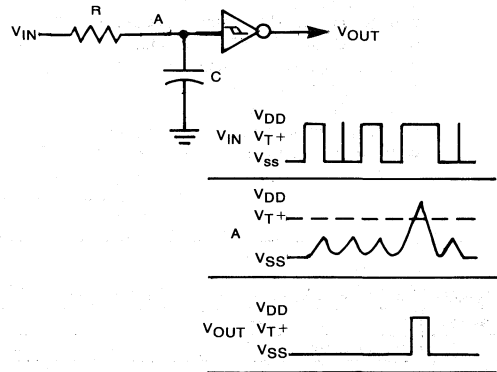
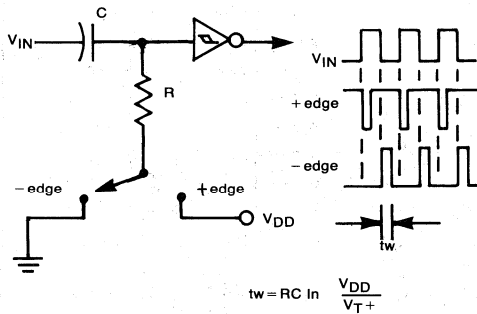


FIGURE 6 — INTEGRATOR



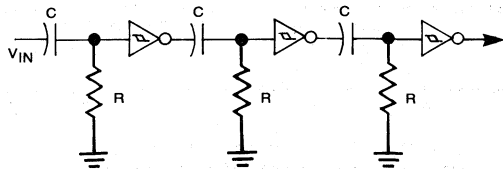
Useful in discriminating against short pulse durations.

FIGURE 7 — DIFFERENTIATOR



Useful as an edge detector circuit.

FIGURE 8 — POSITIVE EDGE TIME DELAY CIRCUIT





MOTOROLA

CMOS MSI

SYNCHRONOUS PRESETTABLE 4-BIT COUNTERS

The MC14160B – MC14163B are synchronous programmable counters constructed with complementary MOS P-Channel and N-Channel enhancement mode devices in a single monolithic structure. These counters are functionally equivalent to the 74160–74163 TTL counters.

Two are synchronous programmable BCD counters with asynchronous and synchronous clear inputs respectively (MC14160B, MC14162B). The other two are synchronous programmable 4-bit binary counters with the asynchronous and synchronous clear respectively (MC14161B, MC14163B).

- Internal Look-Ahead for Fast Counting
- Carry Output for N-Bit Cascading
- Synchronously Programmable
- Synchronous Counting
- Load Control Line
- Synchronous or Asynchronous Clear
- Positive Edge Clocked

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

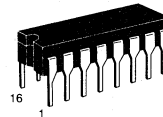
Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	-0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	-0.5 to $V_{DD} + 0.5$	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	± 10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.

†Temperature Derating: Plastic "P and D/DW" Packages: -7.0 mW/°C From 65°C To 125°C
Ceramic "L" Packages: -12 mW/°C From 100°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

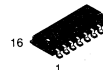
MC14160B
MC14161B
MC14162B
MC14163B



L SUFFIX
CERAMIC
CASE 620



P SUFFIX
PLASTIC
CASE 648



D SUFFIX
SOIC
CASE 751B

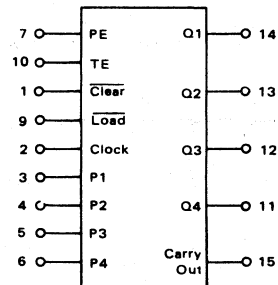
ORDERING INFORMATION

MC14XXXBCP Plastic
MC14XXXBCL Ceramic
MC14XXXBD SOIC

$T_A = -55^\circ\text{C}$ to 125°C for all packages.

6

BLOCK DIAGRAM



$V_{DD} = \text{Pin 16}$
 $V_{SS} = \text{Pin 8}$

MC14160B thru MC14163B

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V _{DD} Vdc	-55°C		25°C			125°C		Unit	
			Min	Max	Min	Typ #	Max	Min	Max		
Output Voltage V _{in} = V _{DD} or 0	V _{OL}	5.0	—	0.05	—	0	0.05	—	0.05	Vdc	
		10	—	0.05	—	0	0.05	—	0.05		
		15	—	0.05	—	0	0.05	—	0.05		
	V _{in} = 0 or V _{DD}	V _{OH}	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc
		10	9.95	—	9.95	10	—	9.95	—		
		15	14.95	—	14.95	15	—	14.95	—		
Input Voltage (V _O = 4.5 or 0.5 Vdc) (V _O = 9.0 or 1.0 Vdc) (V _O = 13.5 or 1.5 Vdc)	V _{IL}	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc	
		10	—	3.0	—	4.50	3.0	—	3.0		
		15	—	4.0	—	6.75	4.0	—	4.0		
	V _{IH}	5.0	3.5	—	3.5	2.75	—	3.5	—	—	Vdc
		10	7.0	—	7.0	5.50	—	7.0	—	—	
		15	11	—	11	8.25	—	11	—	—	
Output Drive Current (V _{OH} = 2.5 Vdc) (V _{OH} = 4.6 Vdc) (V _{OH} = 9.5 Vdc) (V _{OH} = 13.5 Vdc)	Source I _{OH}	5.0	-3.0	—	-2.4	-4.2	—	-1.7	—	mAdc	
		5.0	-0.64	—	-0.51	-0.88	—	-0.36	—		
		10	-1.6	—	-1.3	-2.25	—	-0.9	—		
	Sink I _{OL}	5.0	0.64	—	0.51	0.88	—	0.36	—	mAdc	
		10	1.6	—	1.3	2.25	—	0.9	—		
		15	4.2	—	3.4	8.8	—	2.4	—		
Input Current	I _{in}	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	μAdc	
Input Capacitance (V _{in} = 0)	C _{in}	—	—	—	—	5.0	7.5	—	—	pF	
Quiescent Current (Per Package)	I _{DD}	5.0	—	5.0	—	0.005	5.0	—	150	μAdc	
		10	—	10	—	0.010	10	—	300		
		15	—	20	—	0.015	20	—	600		
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C _L = 50 pF on all outputs, all buffers switching)	I _T	5.0	I _T = (0.56 μA/kHz) f + I _{DD}						μAdc		
		10	I _T = (1.10 μA/kHz) f + I _{DD}								
		15	I _T = (1.90 μA/kHz) f + I _{DD}								

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

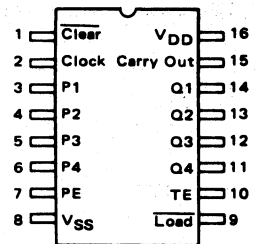
**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) V/k$$

where: I_T is in μA (per package), C_L in pF, V = (V_{DD} - V_{SS}) in volts, f in kHz is input frequency, and k = 0.001.

PIN ASSIGNMENT



MC14160B thru MC14163B

SWITCHING CHARACTERISTICS (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V _{DD} V _{dC}	Min	Typ #	Max	Unit
Output Rise Time	t _{TLH}	5.0 10 15	— — —	100 50 40	200 100 80	ns
Output Fall Time	t _{THL}	5.0 10 15	— — —	100 50 40	200 100 80	ns
Propagation Delay Time Clock to Q t _{PLH} , t _{PHL} = (0.90 ns/pF) C _L + 305 ns t _{PLH} , t _{PHL} = (0.36 ns/pF) C _L + 132 ns t _{PLH} , t _{PHL} = (0.26 ns/pF) C _L + 87 ns Clock to Carry Out t _{PLH} , t _{PHL} = (0.90 ns/pF) C _L + 395 ns t _{PLH} , t _{PHL} = (0.36 ns/pF) C _L + 167 ns t _{PLH} , t _{PHL} = (0.26 ns/pF) C _L + 112 ns TE to Carry Out t _{PLH} , t _{PHL} = (0.90 ns/pF) C _L + 225 ns t _{PLH} , t _{PHL} = (0.36 ns/pF) C _L + 112 ns t _{PLH} , t _{PHL} = (0.26 ns/pF) C _L + 77 ns Clear to Q (MC14160B, MC14161B only) t _{PLH} , t _{PHL} = (0.90 ns/pF) C _L + 110 ns t _{PLH} , t _{PHL} = (0.36 ns/pF) C _L + 37 ns t _{PLH} , t _{PHL} = (0.26 ns/pF) C _L + 22 ns	t _{PLH} , t _{PHL}	5.0 10 15	— — —	350 150 100	700 300 200	ns
Setup Times Data to Clock Load to Clock Enable to Clock (PE or TE) Clear to Clock (MC14162B, MC14163B only)	t _{su}	5.0 10 15 5.0 10 15 5.0 10 15 5.0 10 15	320 130 90 600 260 180 420 170 120 310 110 70	160 65 45 300 130 90 210 85 60 155 55 35	— — — — — — — — — — — —	ns
Hold Times Clock to Data Clock to Load Clock to PE Clock to TE Clock to Clear (MC14162B, MC14163B only)	t _h	5.0 10 15 5.0 10 15 5.0 10 15 5.0 10 15	-10 -5 0 -40 -10 -5 -40 -10 0 -150 -30 -20 80 30 -10	-60 -25 -15 -195 -80 -50 -175 -70 -40 -280 -130 -80 40 15 -70	— — — — — — — — — — — — — — —	ns
Clear Removal Time (MC14160B, MC14161B only)	t _{rem}	5.0 10 15	90 65 55	30 20 20	— — —	ns

MC14160B thru MC14163B

SWITCHING CHARACTERISTICS ($C_L = 50$ pF, $T_A = 25^\circ\text{C}$) (Continued)

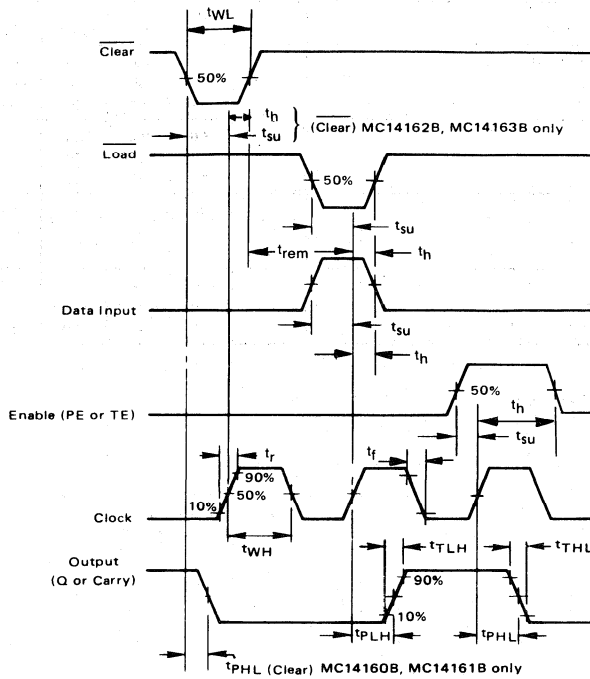
Characteristic	Symbol	V_{DD} Vdc	Min	Typ #	Max	Unit
Clear Pulse Width, Low (MC14160B, MC14161B only)	t_{WL}	5.0	200	100	—	ns
		10	90	45	—	
		15	60	30	—	
Clock Pulse Width, High	t_{WH}	5.0	250	125	—	ns
		10	100	50	—	
		15	70	35	—	
Clock Rise and Fall Time	$t_r,$ t_f	5	—	—	15	μs
		10	—	—	5	
		15	—	—	4	
Clock Pulse Frequency	f_{cl}	5.0	—	2.0	1.0	MHz
		10	—	5.0	2.5	
		15	—	8.0	4.0	

*The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

MC14160B thru MC14163B

SWITCHING WAVEFORMS



FUNCTIONAL DESCRIPTION

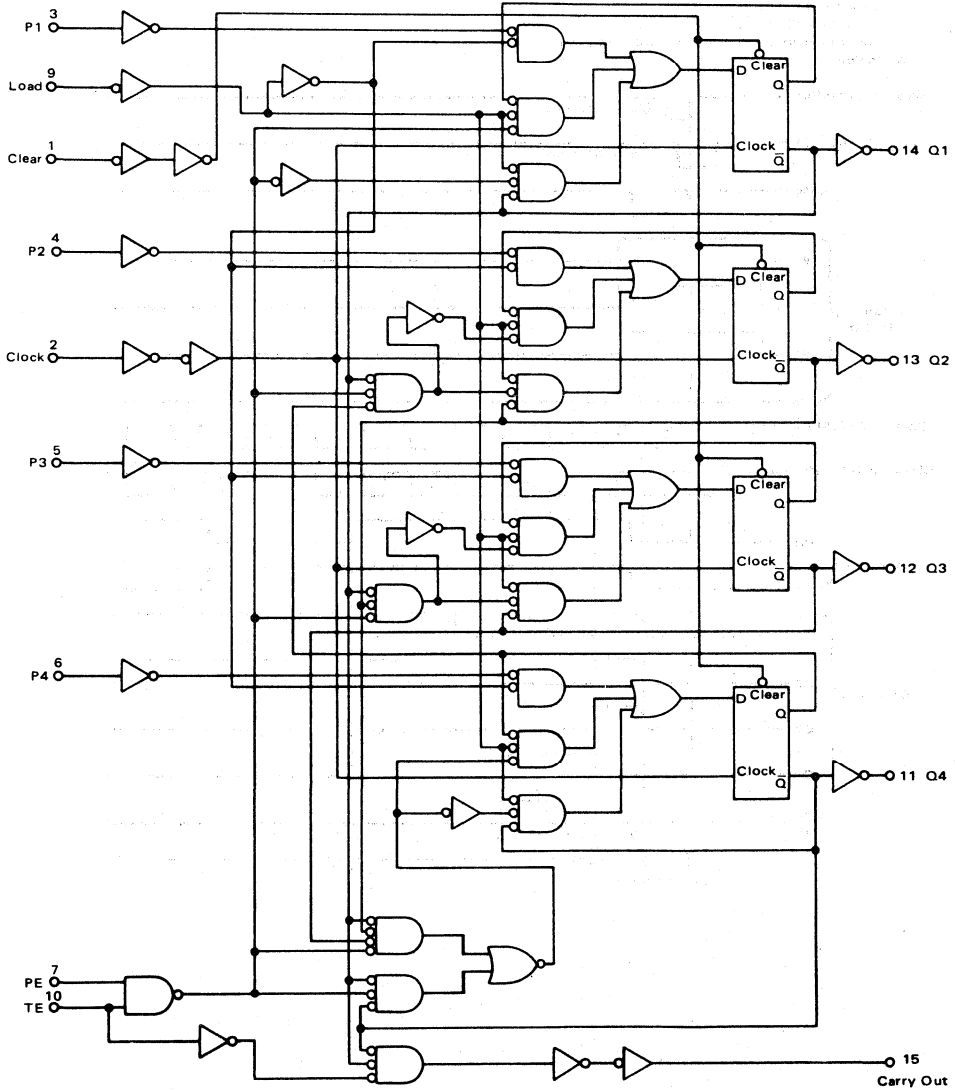
These counters are fully programmable; that is the outputs may be preset to either level. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the levels of the enable inputs. The clear function for the MC14160B, MC14161B is asynchronous and a low level at the clear input sets all four of the flip-flop outputs low regardless of the levels of the clock, load or enable inputs. The clear function for the MC14162B and MC14163B is synchronous and a low level at the clear inputs sets all four of the flip-flop outputs low after the next clock pulse, regardless of the levels of the enable inputs. This synchronous clear allows the count length to be modified easily; decoding the maximum count de-

sired can be accomplished with one external NAND gate. The gate output is connected to the clear input to synchronously clear the counter to 0000 (LLLL).

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a carry output. Both count-enable inputs (PE, TE) must be high to count, and enable input TE fed forward to enable the carry output. The carry output thus enabled will produce a positive output pulse with a duration approximately equal to the positive portion of the Q1 output. This positive overflow carry pulse can be used to enable successive cascaded stages.

MC14160B thru MC14163B

MC14160B, MC14162B LOGIC DIAGRAM
(Clear is synchronous for MC14162B)



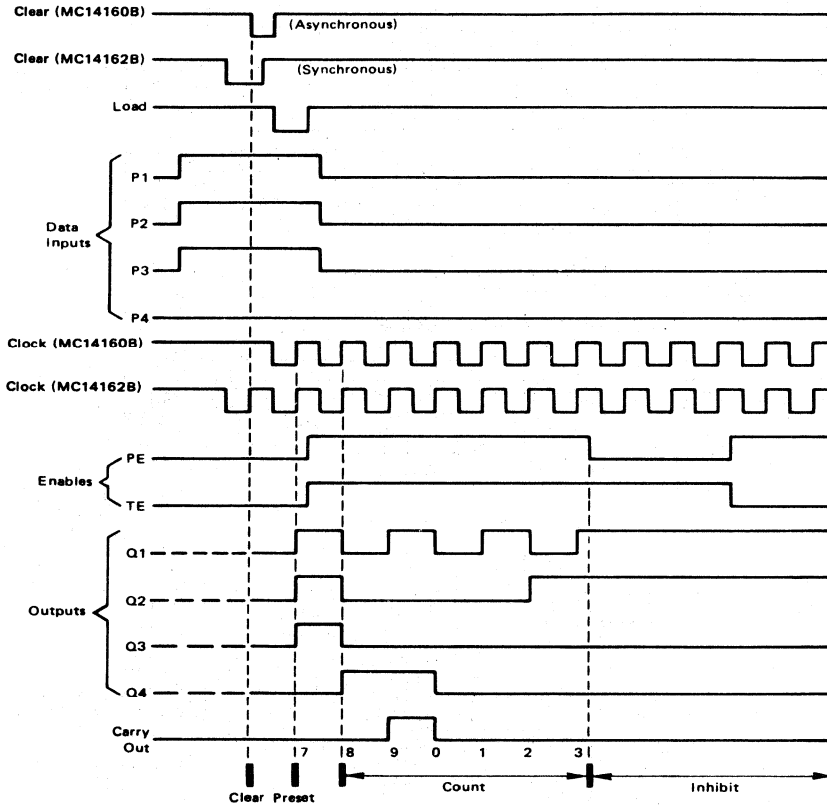
6

MC14160B thru MC14163B

MC14160B, MC14162B TIMING DIAGRAM

Sequence illustrated in waveforms:

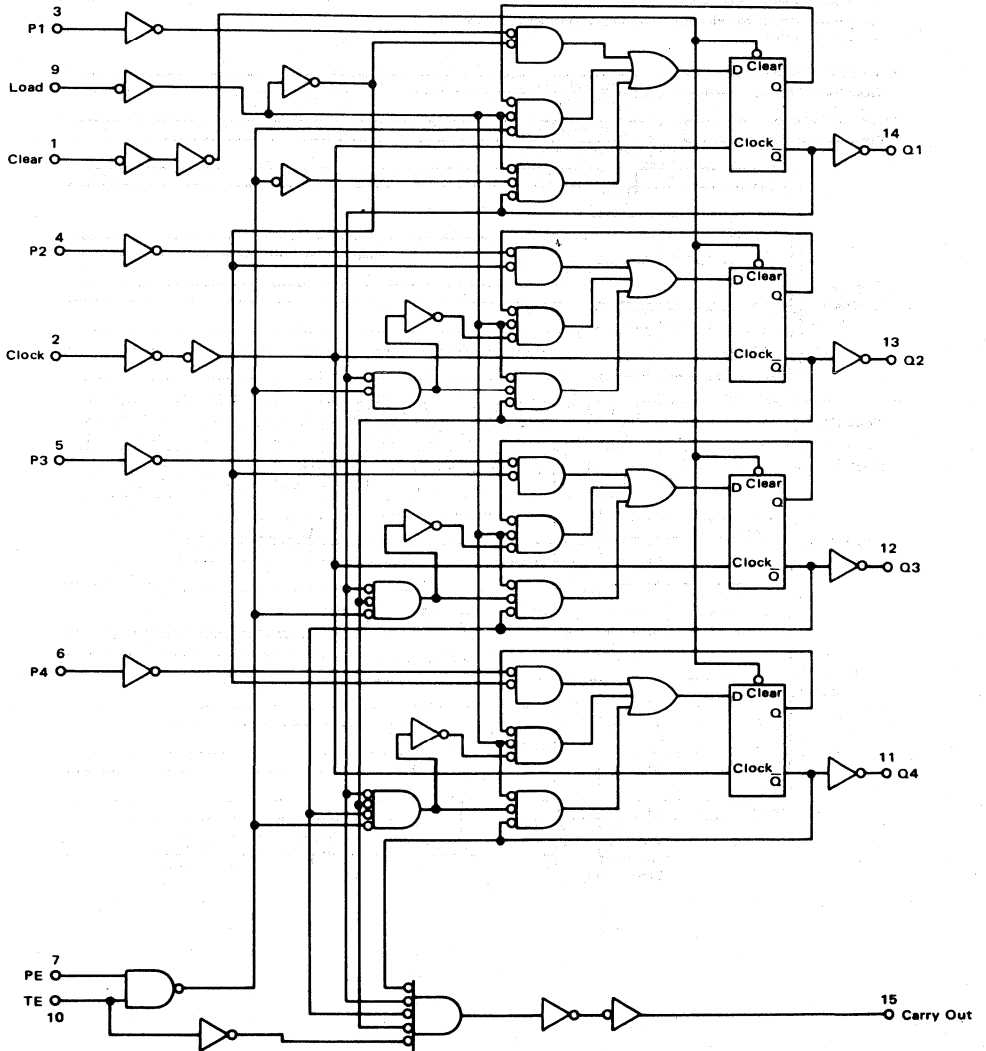
1. Clear outputs to zero.
2. Preset to BCD seven.
3. Count to eight, nine, zero, one, two, and three.
4. Inhibit



6

MC14160B thru MC14163B

MC14161B, MC14163B LOGIC DIAGRAM
(Clear is Synchronous for MC14163B)



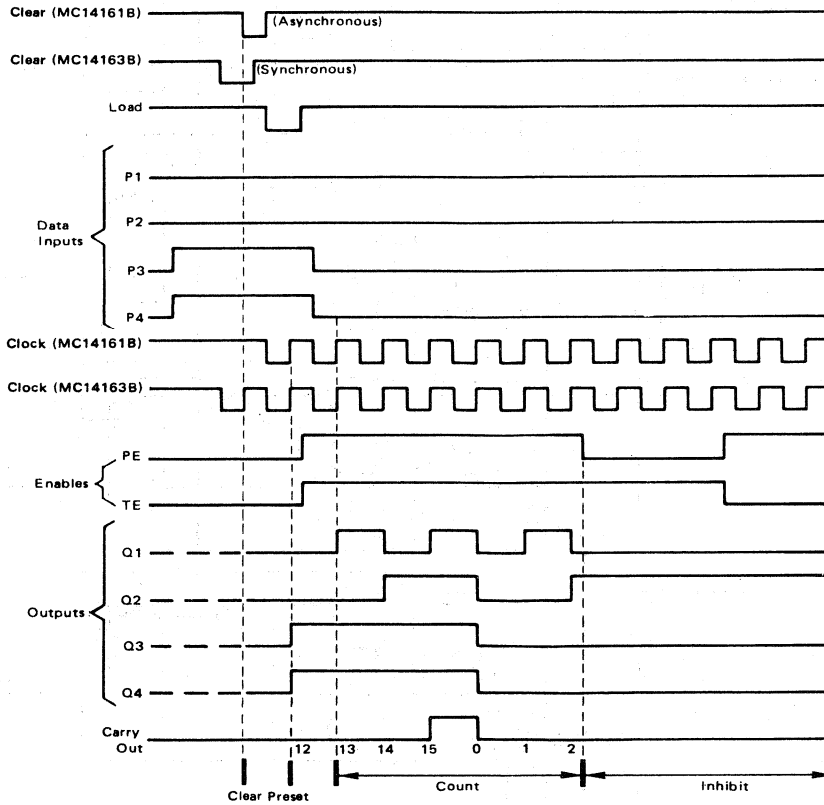
6

MC14160B thru MC14163B

MC14161B, MC14163B TIMING DIAGRAM

Sequence illustrated in waveforms:

1. Clear outputs to zero.
2. Preset to binary twelve.
3. Count to thirteen, fourteen, fifteen, zero, one, and two.
4. Inhibit





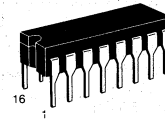
MOTOROLA

MC14174B

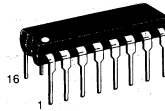
HEX TYPE D FLIP-FLOP

The MC14174B hex type D flip-flop is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. Data on the D inputs which meets the setup time requirements is transferred to the Q outputs on the positive edge of the clock pulse. All six flip-flops share common clock and reset inputs. The reset is active low, and independent of the clock.

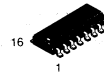
- Static Operation
- All Inputs and Outputs Buffered
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-Power Schottky TTL Load over the Rated Temperature Range
- Functional Equivalent to TTL 74174



L SUFFIX
CERAMIC
CASE 620



P SUFFIX
PLASTIC
CASE 648



D SUFFIX
SOIC
CASE 751B

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	-0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	-0.5 to $V_{DD} + 0.5$	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	± 10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P and D/DW" Packages: -7.0 mW/°C From 65°C To 125°C
Ceramic "L" Packages: -12 mW/°C From 100°C To 125°C

ORDERING INFORMATION

MC14XXXBCP Plastic
MC14XXXBCL Ceramic
MC14XXXBD SOIC

$T_A = -55^\circ\text{C}$ to 125°C for all packages.

TRUTH TABLE
(Positive Logic)

	INPUTS			OUTPUT
	Clock	Data	Reset	Q
	0	1	1	0
	1	1	1	1
	X	X	1	Q
	X	X	0	0

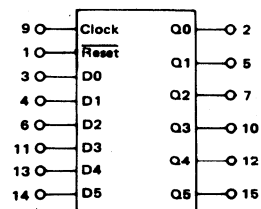
No Change

X = Don't Care

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

BLOCK DIAGRAM



$V_{DD} = \text{Pin } 16$
 $V_{SS} = \text{Pin } 8$

MC14174B

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V _{DD} Vdc	-55°C		25°C			125°C		Unit
			Min	Max	Min	Typ #	Max	Min	Max	
Output Voltage V _{in} = V _{DD} or 0 V _{in} = 0 or V _{DD}	"0" Level VOL	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
		10	—	0.05	—	0	0.05	—	0.05	
		15	—	0.05	—	0	0.05	—	0.05	
	"1" Level VOH	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc
		10	9.95	—	9.95	10	—	9.95	—	
		15	14.95	—	14.95	15	—	14.95	—	
Input Voltage (V _O = 4.5 or 0.5 Vdc) (V _O = 9.0 or 1.0 Vdc) (V _O = 13.5 or 1.5 Vdc) (V _O = 0.5 or 4.5 Vdc) (V _O = 1.0 or 9.0 Vdc) (V _O = 1.5 or 13.5 Vdc)	"0" Level V _{IL}	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc
		10	—	3.0	—	4.50	3.0	—	3.0	
		15	—	4.0	—	6.75	4.0	—	4.0	
	"1" Level V _{IH}	5.0	3.5	—	3.5	2.75	—	3.5	—	Vdc
		10	7.0	—	7.0	5.50	—	7.0	—	
		15	11	—	11	8.25	—	11	—	
Output Drive Current (V _{OH} = 2.5 Vdc) (V _{OH} = 4.6 Vdc) (V _{OH} = 9.5 Vdc) (V _{OH} = 13.5 Vdc) (V _{OL} = 0.4 Vdc) (V _{OL} = 0.5 Vdc) (V _{OL} = 1.5 Vdc)	Source I _{OH}	5.0	-3.0	—	-2.4	-4.2	—	-1.7	—	mAdc
		5.0	-0.64	—	-0.51	-0.88	—	-0.36	—	
		10	-1.6	—	-1.3	-2.25	—	-0.9	—	
	Sink I _{OL}	5.0	0.64	—	0.51	0.88	—	0.36	—	mAdc
		10	1.6	—	1.3	2.25	—	0.9	—	
		15	4.2	—	3.4	8.8	—	2.4	—	
Input Current	I _{in}	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	μAdc
Input Capacitance (V _{in} = 0)	C _{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)	I _{DD}	5.0	—	5.0	—	0.005	5.0	—	150	μAdc
		10	—	10	—	0.010	10	—	300	
		15	—	20	—	0.015	20	—	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C _L = 50 pF on all outputs, all buffers switching)	I _T	5.0	I _T = (1.1 μA/kHz) f + I _{DD}							μAdc
		10	I _T = (2.3 μA/kHz) f + I _{DD}							
		15	I _T = (3.7 μA/kHz) f + I _{DD}							

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) V/k$$

where: I_T is in μA (per package), C_L in pF, V = (V_{DD} - V_{SS}) in volts, f in kHz is input frequency, and k = 0.003.

MC14174B

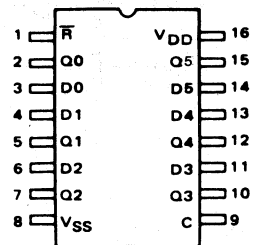
SWITCHING CHARACTERISTICS* ($C_L = 50 \text{ pF}$, $T_A = 25^\circ\text{C}$)

Characteristic	Symbol	VDD Vdc	All Types			Unit
			Min	Typ #	Max	
Output Rise and Fall Time t_{TLH} , $t_{THL} = (1.35 \text{ ns/pF}) C_L + 32 \text{ ns}$ t_{TLH} , $t_{THL} = (0.6 \text{ ns/pF}) C_L + 20 \text{ ns}$ t_{TLH} , $t_{THL} = (0.4 \text{ ns/pF}) C_L + 20 \text{ ns}$	t_{TLH} , t_{THL}	5.0 10 15	— — —	100 50 40	200 100 80	ns
Propagation Delay Time — Clock to Q t_{PLH} , $t_{PHL} = (0.9 \text{ ns/pF}) C_L + 165 \text{ ns}$ t_{PLH} , $t_{PHL} = (0.36 \text{ ns/pF}) C_L + 64 \text{ ns}$ t_{PLH} , $t_{PHL} = (0.26 \text{ ns/pF}) C_L + 52 \text{ ns}$	t_{PLH} , t_{PHL}	5.0 10 15	— — —	210 85 65	400 160 120	ns
Propagation Delay Time — Reset to Q $t_{PHL} = (0.9 \text{ ns/pF}) C_L + 205 \text{ ns}$ $t_{PHL} = (0.36 \text{ ns/pF}) C_L + 79 \text{ ns}$ $t_{PHL} = (0.26 \text{ ns/pF}) C_L + 62 \text{ ns}$	t_{PHL}	5.0 10 15	— — —	250 100 75	500 200 150	ns
Clock Pulse Width	t_{WH}	5.0 10 15	150 90 70	75 45 35	— — —	ns
Reset Pulse Width	t_{WL}	5.0 10 15	200 100 80	100 50 40	— — —	ns
Clock Pulse Frequency	f_{cl}	5.0 10 15	— — —	7.0 12.0 15.5	2.0 5.0 6.5	MHz
Clock Pulse Rise and Fall Time	t_{TLH} , t_{THL}	5.0 10 15	— — —	— — —	15 5.0 4.0	μs
Data Setup Time	t_{su}	5.0 10 15	40 20 15	20 10 0	— — —	ns
Data Hold Time	t_h	5.0 10 15	80 40 30	40 20 15	— — —	ns
Reset Removal Time	t_{rem}	5.0 10 15	250 100 80	125 50 40	— — —	ns

*The formulas given are for the typical characteristics only at 25°C.

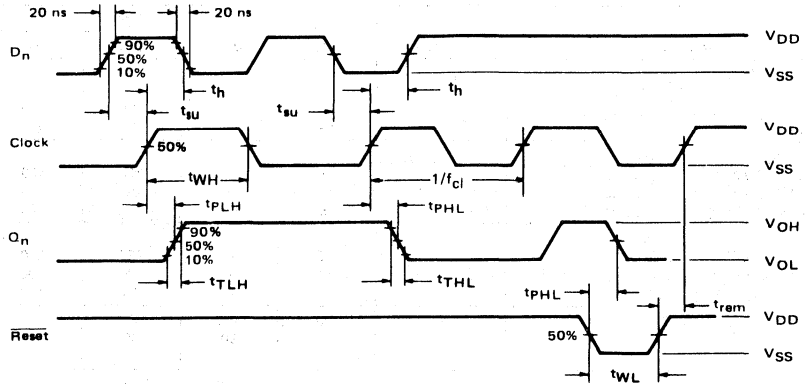
#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

PIN ASSIGNMENT

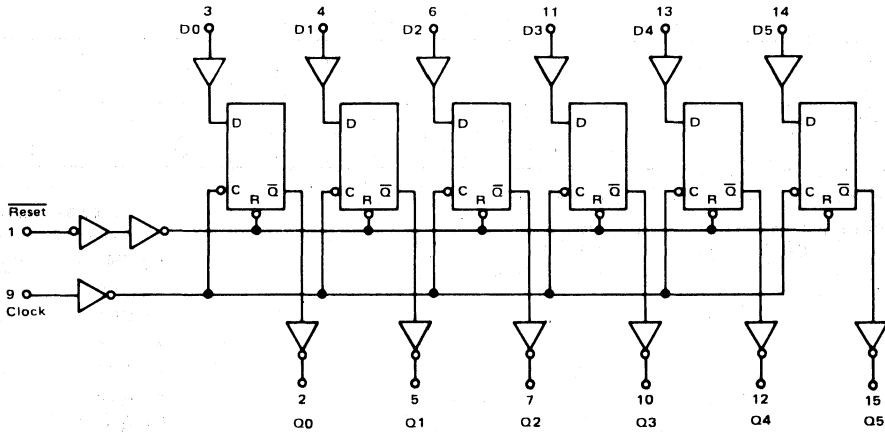


MC14174B

TIMING DIAGRAM



FUNCTIONAL BLOCK DIAGRAM



6



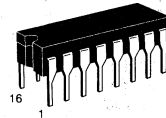
MOTOROLA

MC14175B

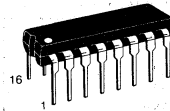
QUAD TYPE D FLIP-FLOP

The MC14175B quad type D flip-flop is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. Each of the four flip-flops is positive-edge triggered by a common clock input (C). An active-low reset input (\bar{R}) asynchronously resets all flip-flops. Each flip-flop has independent Data (D) inputs and complementary outputs (Q and \bar{Q}). These devices may be used as shift register elements or as type T flip-flops for counter and toggle applications.

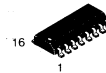
- Complementary Outputs
- Static Operation
- All Inputs and Outputs Buffered
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Output Compatible with Two Low-Power TTL Loads or One Low-Power Schottky TTL Load
- Functional Equivalent to TTL 74175



L SUFFIX
CERAMIC
CASE 620



P SUFFIX
PLASTIC
CASE 648



D SUFFIX
SOIC
CASE 751B

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	-0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	-0.5 to $V_{DD} + 0.5$	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	± 10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P and D/DW" Packages: -7.0 mW/°C From 65°C To 125°C
Ceramic "L" Packages: -12 mW/°C From 100°C To 125°C

ORDERING INFORMATION

MC14XXXBCP Plastic
MC14XXXBCL Ceramic
MC14XXXBD SOIC

$T_A = -55^\circ$ to 125° C for all packages.

TRUTH TABLE

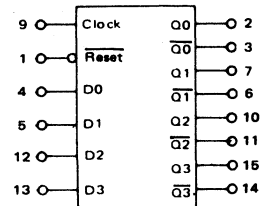
INPUTS			OUTPUTS		
Clock	Data	Reset	Q	\bar{Q}	
	0	1	0	1	No Change
	1	1	1	0	
	X	1	Q	\bar{Q}	
X	X	0	0	1	

X = Don't Care

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For

proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

BLOCK DIAGRAM



$V_{DD} = \text{Pin } 16$
 $V_{SS} = \text{Pin } 8$

MC14175B

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	VDD Vdc	-55°C		25°C			125°C		Unit
			Min	Max	Min	Typ #	Max	Min	Max	
Output Voltage V _{in} = V _{DD} or 0	V _{OL}	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
		10	—	0.05	—	0	0.05	—	0.05	
V _{in} = 0 or V _{DD}	V _{OH}	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc
		10	9.95	—	9.95	10	—	9.95	—	
Input Voltage (V _O = 4.5 or 0.5 Vdc) (V _O = 9.0 or 1.0 Vdc) (V _O = 13.5 or 1.5 Vdc)	V _{IL}	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc
		10	—	3.0	—	4.50	3.0	—	3.0	
(V _O = 0.5 or 4.5 Vdc) (V _O = 1.0 or 9.0 Vdc) (V _O = 1.5 or 13.5 Vdc)	V _{IH}	5.0	3.5	—	3.5	2.75	—	3.5	—	Vdc
		10	7.0	—	7.0	5.50	—	7.0	—	
Output Drive Current (V _{OH} = 2.5 Vdc) (V _{OH} = 4.6 Vdc) (V _{OH} = 9.5 Vdc) (V _{OH} = 13.5 Vdc)	Source I _{OH}	5.0	-3.0	—	-2.4	-4.2	—	-1.7	—	mAdc
		5.0	-0.64	—	-0.51	-0.88	—	-0.36	—	
(V _{OL} = 0.4 Vdc) (V _{OL} = 0.5 Vdc) (V _{OL} = 1.5 Vdc)	Sink I _{OL}	5.0	0.64	—	0.51	0.88	—	0.36	—	mAdc
		10	1.6	—	1.3	2.25	—	0.9	—	
		15	4.2	—	3.4	8.8	—	2.4	—	
Input Current	I _{in}	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	μAdc
Input Capacitance (V _{in} = 0)	C _{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)	I _{DD}	5.0	—	5.0	—	0.005	5.0	—	150	μAdc
		10	—	10	—	0.010	10	—	300	
		15	—	20	—	0.015	20	—	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C _L = 50 pF on all outputs, all buffers switching)	I _T	5.0	I _T = (1.7 μA/kHz) f + I _{DD}							μAdc
		10	I _T = (3.4 μA/kHz) f + I _{DD}							
		15	I _T = (5.0 μA/kHz) f + I _{DD}							

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

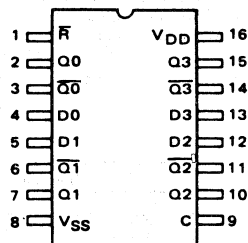
**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) V/k$$

where: I_T is in μA (per package), C_L in pF, V = (V_{DD} - V_{SS}) in volts, f in kHz is input frequency, and k = 0.004.

PIN ASSIGNMENT



MC14175B

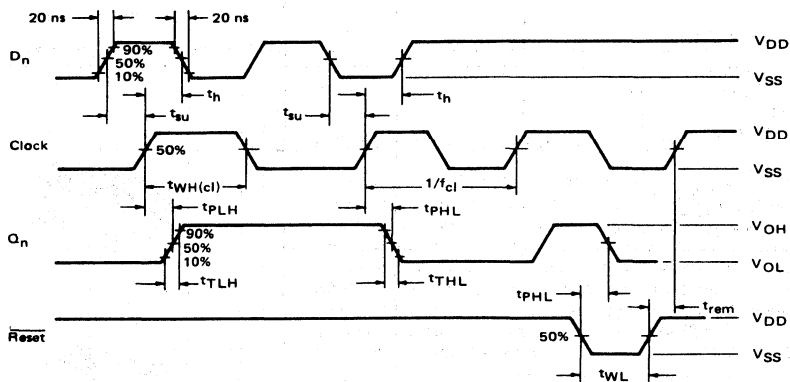
SWITCHING CHARACTERISTICS* ($C_L = 50 \text{ pF}$, $T_A = 25^\circ\text{C}$)

Characteristic	Symbol	VDD Vdc	All Types			Unit
			Min	Typ #	Max	
Output Rise and Fall Time $t_{TLH}, t_{THL} = (1.35 \text{ ns/pF}) C_L + 32 \text{ ns}$ $t_{TLH}, t_{THL} = (0.6 \text{ ns/pF}) C_L + 20 \text{ ns}$ $t_{TLH}, t_{THL} = (0.4 \text{ ns/pF}) C_L + 20 \text{ ns}$	t_{TLH}, t_{THL}	5.0 10 15	— — —	100 50 40	200 100 80	ns
Propagation Delay Time — Clock to Q, \bar{Q} $t_{PLH}, t_{PHL} = (0.9 \text{ ns/pF}) C_L + 175 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.36 \text{ ns/pF}) C_L + 72 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.26 \text{ ns/pF}) C_L + 57 \text{ ns}$	t_{PLH}, t_{PHL}	5.0 10 15	— — —	220 90 70	400 160 120	ns
Propagation Delay Time — Reset to Q, \bar{Q} $t_{PHL} = (0.9 \text{ ns/pF}) C_L + 280 \text{ ns}$ $t_{PHL} = (0.36 \text{ ns/pF}) C_L + 112 \text{ ns}$ $t_{PHL} = (0.26 \text{ ns/pF}) C_L + 87 \text{ ns}$	t_{PHL}, t_{PLH}	5.0 10 15	— — —	325 130 100	500 200 150	ns
Clock Pulse Width	t_{WH}	5.0 10 15	250 100 75	110 45 35	— — —	ns
Reset Pulse Width	t_{WL}	5.0 10 15	200 80 60	100 40 30	— — —	ns
Clock Pulse Frequency	f_{cl}	5.0 10 15	— — —	4.5 11 14	2.0 5.0 6.5	MHz
Clock Pulse Rise and Fall Time	t_{TLH}, t_{THL}	5.0 10 15	— — —	— — —	15 5 4	μs
Data Setup Time	t_{su}	5.0 10 15	120 50 40	60 25 20	— — —	ns
Data Hold Time	t_h	5.0 10 15	80 40 30	40 20 15	— — —	ns
Reset Removal Time	t_{rem}	5.0 10 15	250 100 80	125 50 40	— — —	ns

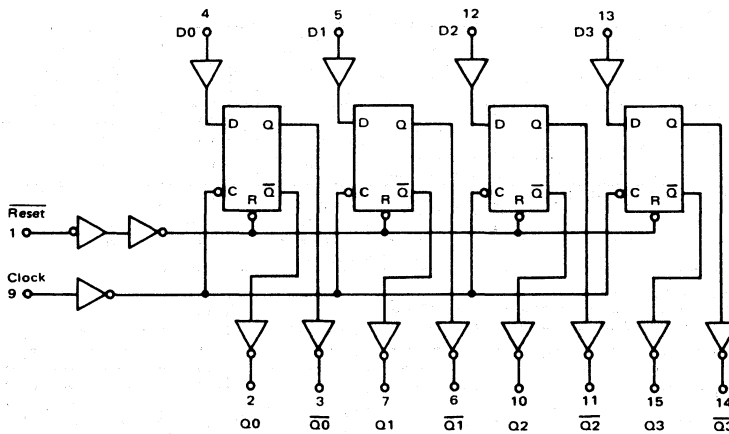
*The formulas given are for the typical characteristics only at 25°C.
#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

MC14175B

TIMING DIAGRAM



FUNCTIONAL BLOCK DIAGRAM



6



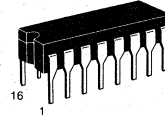
MOTOROLA

MC14194B

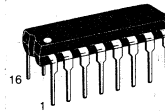
4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTER

The MC14194B is a 4-bit static shift register capable of operating in the parallel load, serial shift left, serial shift right, or hold mode. The asynchronous Reset input, when at a low level, overrides all other inputs, resets all stages, and forces all outputs low. When Reset is at a logic 1 level, the two mode control inputs, S0 and S1, control the operating mode as shown in the truth table. Both serial and parallel operation are triggered on the positive-going transition of the Clock input. The Parallel Data, Data Shift, and mode control inputs must be stable for the specified setup and hold times before and after the positive-going Clock transition.

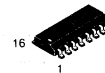
- Synchronous Right/Left Serial Operation
- Synchronous Parallel Load
- Asynchronous Hold (Do Nothing) Mode
- Functional Pin for Pin Equivalent of LS194



L SUFFIX
CERAMIC
CASE 620



P SUFFIX
PLASTIC
CASE 648



D SUFFIX
SOIC
CASE 751B

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V _{DD}	DC Supply Voltage	-0.5 to +18.0	V
V _{in} , V _{out}	Input or Output Voltage (DC or Transient)	-0.5 to V _{DD} + 0.5	V
I _{in} , I _{out}	Input or Output Current (DC or Transient), per Pin	± 10	mA
P _D	Power Dissipation, per Package†	500	mW
T _{stg}	Storage Temperature	-65 to +150	°C
T _L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.

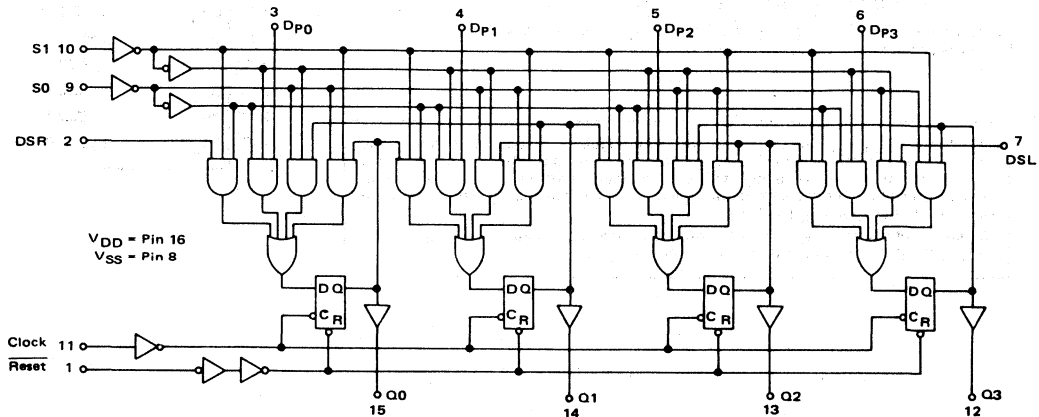
†Temperature Derating: Plastic "P and D/DW" Packages: -7.0 mW/°C From 65°C To 125°C
Ceramic "L" Packages: -12 mW/°C From 100°C To 125°C

ORDERING INFORMATION

MC14XXXBCP Plastic
MC14XXXBCL Ceramic
MC14XXXBD SOIC

T_A = -55° to 125°C for all packages.

LOGIC DIAGRAM



MC14194B

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V _{DD} Vdc	-55°C		25°C			125°C		Unit	
			Min	Max	Min	Typ #	Max	Min	Max		
Output Voltage V _{in} = V _{DD} or 0	V _{OL}	5.0	—	0.05	—	0	0.05	—	0.05	Vdc	
		10	—	0.05	—	0	0.05	—	0.05		
		15	—	0.05	—	0	0.05	—	0.05		
	V _{in} = 0 or V _{DD}	V _{OH}	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc
10			9.95	—	9.95	10	—	9.95	—		
15			14.95	—	14.95	15	—	14.95	—		
Input Voltage (V _O = 4.5 or 0.5 Vdc) (V _O = 9.0 or 1.0 Vdc) (V _O = 13.5 or 1.5 Vdc)	V _{IL}	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc	
		10	—	3.0	—	4.50	3.0	—	3.0		
		15	—	4.0	—	6.75	4.0	—	4.0		
	V _O = 0.5 or 4.5 Vdc) (V _O = 1.0 or 9.0 Vdc) (V _O = 1.5 or 13.5 Vdc)	V _{IH}	5.0	3.5	—	3.5	2.75	—	3.5	—	Vdc
			10	7.0	—	7.0	5.50	—	7.0	—	
			15	11	—	11	8.25	—	11	—	
Output Drive Current (V _{OH} = 2.5 Vdc) (V _{OH} = 4.6 Vdc) (V _{OH} = 9.5 Vdc) (V _{OH} = 13.5 Vdc)	Source I _{OH}	5.0	-3.0	—	-2.4	-4.2	—	-1.7	—	mAdc	
		5.0	-0.64	—	-0.51	-0.88	—	-0.36	—		
		10	-1.6	—	-1.3	-2.25	—	-0.9	—		
	Sink I _{OL}	5.0	0.64	—	0.51	0.88	—	0.36	—	mAdc	
		10	1.6	—	1.3	2.25	—	0.9	—		
		15	4.2	—	3.4	8.8	—	2.4	—		
Input Current	I _{in}	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	μAdc	
Input Capacitance (V _{in} = 0)	C _{in}	—	—	—	—	5.0	7.5	—	—	pF	
Quiescent Current (Per Package)	I _{DD}	5.0	—	5.0	—	0.005	5.0	—	150	μAdc	
		10	—	10	—	0.010	10	—	300		
		15	—	20	—	0.015	20	—	600		
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C _L = 50 pF on all outputs, all buffers switching)	I _T	5.0	I _T = (0.95 μA/kHz) f + I _{DD}						μAdc		
		10	I _T = (1.90 μA/kHz) f + I _{DD}								
		15	I _T = (2.90 μA/kHz) f + I _{DD}								

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

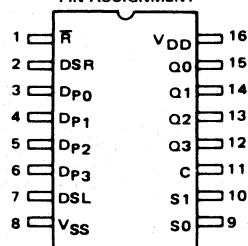
$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) V/k$$

where: I_T is in μA (per package), C_L in pF, V = (V_{DD} - V_{SS}) in volts, f in kHz is input frequency, and k = 0.002.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range V_{SS} ≤ (V_{in} or V_{out}) ≤ V_{DD}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

PIN ASSIGNMENT



MC14194B

TRUTH TABLE

OPERATING MODE	INPUTS (Reset = 1)					OUTPUTS (@ t_{n+1})			
	S1	S0	DSR	DSL	Dp0-3	Q0	Q1	Q2	Q3
Hold	0	0	X	X	X	Q0	Q1	Q2	Q3
Shift Left	1	0	X	0	X	Q1	Q2	Q3	0
	1	0	X	1	X	Q1	Q2	Q3	1
Shift Right	0	1	0	X	X	0	Q0	Q1	Q2
	0	1	1	X	X	1	Q0	Q1	Q2
Parallel	1	1	X	X	0	0	0	0	0
	1	1	X	X	1	1	1	1	1

X = Don't Care

t_{n+1} = State after the next positive-going transition of the clock.

SWITCHING CHARACTERISTICS* ($C_L = 50$ pF, $T_A = 25^\circ\text{C}$)

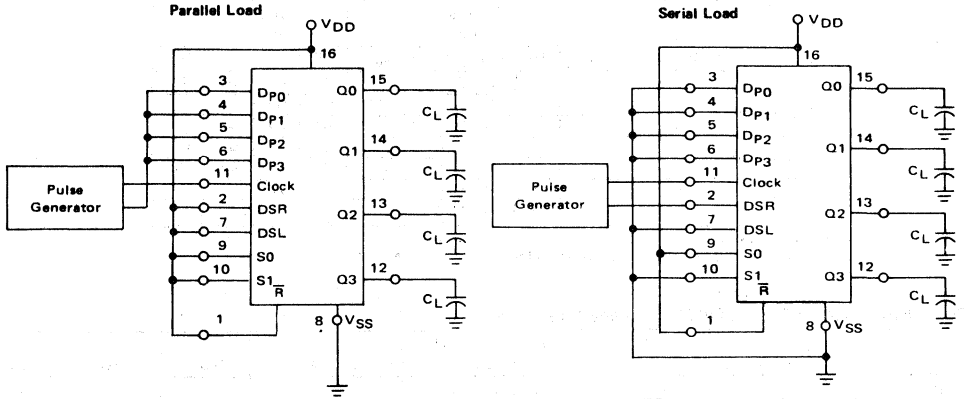
Characteristic	Symbol	VDD Vdc	Min	Typ #	Max	Unit
Output Rise and Fall Time $t_{TLH}, t_{THL} = (1.35 \text{ ns/pF}) C_L + 32 \text{ ns}$ $t_{TLH}, t_{THL} = (0.6 \text{ ns/pF}) C_L + 20 \text{ ns}$ $t_{TLH}, t_{THL} = (0.4 \text{ ns/pF}) C_L + 20 \text{ ns}$	t_{TLH}, t_{THL}	5.0 10 15	— — —	100 50 40	200 100 80	ns
Propagation Delay Time Clock to Q $t_{PLH}, t_{PHL} = (0.9 \text{ ns/pF}) C_L + 230 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.36 \text{ ns/pF}) C_L + 92 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.26 \text{ ns/pF}) C_L + 72 \text{ ns}$ Reset to Q $t_{PHL} = (0.9 \text{ ns/pF}) C_L + 305 \text{ ns}$ $t_{PHL} = (0.36 \text{ ns/pF}) C_L + 122 \text{ ns}$ $t_{PHL} = (0.26 \text{ ns/pF}) C_L + 97 \text{ ns}$	t_{PLH}, t_{PHL} t_{PHL}	5.0 10 15 5.0 10 15	— — — — — —	275 110 85 350 140 110	550 220 170 700 280 220	ns ns
Clock Pulse Width	t_{WH}	5.0 10 15	280 110 85	140 55 40	— — —	ns
Reset Pulse Width	t_{WH}	5.0 10 15	180 70 50	90 35 26	— — —	ns
Clock Pulse Frequency (Shift Right or Left Mode)	f_{cl}	5.0 10 15	— — —	3.6 9.0 12	1.8 4.5 6.0	MHz
Clock Pulse Rise and Fall Time	t_{TLH}, t_{THL}	5.0 10 15	— — —	— — —	15 5 4	μs
Setup Time Data to Clock	t_{su}	5.0 10 15	10 20 40	-8.0 0 9.0	— — —	ns
Mode Control (S) to Clock		5.0 10 15	200 75 55	100 36 27	— — —	ns
Hold Time Data to Clock	t_h	5.0 10 15	180 50 35	90 25 10	— — —	ns
Mode Control (S) to Clock		5.0 10 15	0 0 0	-40 -27 -20	— — —	ns
Reset Removal Time	t_{rem}	5.0 10 15	300 110 80	150 55 40	— — —	ns

**The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

MC14194B

FIGURE 1 – SWITCHING TIME TEST CIRCUITS AND WAVEFORMS



NOTE: Interchange DSR with DSL and S0 with S1 for testing shift left.

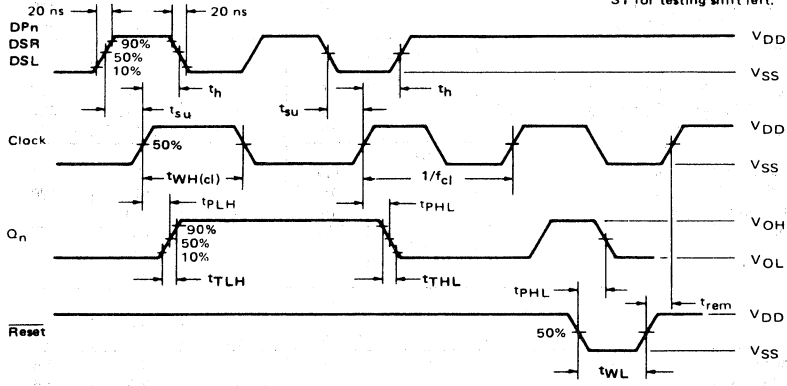
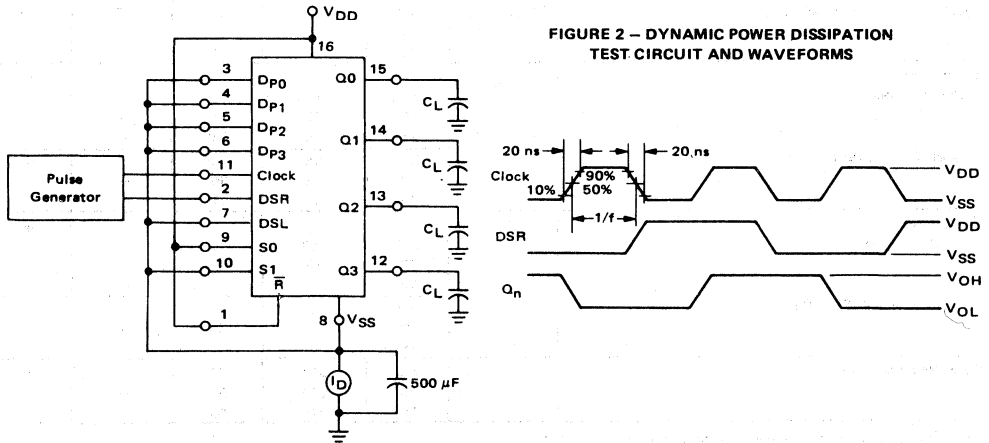


FIGURE 2 – DYNAMIC POWER DISSIPATION TEST CIRCUIT AND WAVEFORMS



6



MOTOROLA

QUAD PRECISION TIMER/DRIVER

MC14415 quad timer/driver is constructed with complementary MOS enhancement mode devices. The output pulse width of each digital timer is a function of the input clock frequency. Once the proper input sequence is detected the output buffer is set (turned on), and after 100 clock pulses are counted, the output buffer is reset (turned off).

The MC14415 was designed specifically for application in high speed line printers to provide the critical timing of the hammer drivers, but may be used in many applications requiring precision pulse widths.

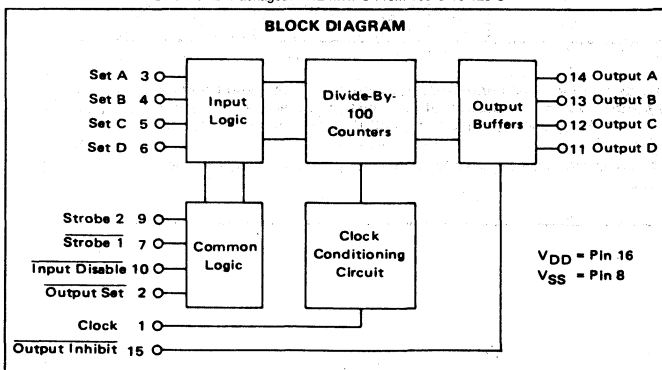
- Four Precision Digital Time Delays
- Schmitt Trigger Clock Conditioning
- NPN Bipolar Output Drivers
- Timing Disable Capability Using Inhibit Output
- Positive or Negative Edge Strobing on the Inputs
- Synchronous Polynomial Counters Used for Delay Counting

MAXIMUM RATINGS* (Voltages referenced to V_{SS})

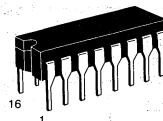
Rating	Symbol	Value	Unit
DC Supply Voltage MC14415FL, FP, DW MC14415VL, VP	V _{DD}	-0.5 to +18 -0.5 to +6.0	V
Input or Output Voltage (DC or Transient)	V _{in} , V _{out}	-0.5 to V _{DD} + 0.5	V
Input Current (DC or Transient), per Pin	I _{in}	±10	mA
Output Current (DC or Transient), per Pin	I _{out}	±20	mA
Power Dissipation, per Package†	P _D	500	mW
Storage Temperature	T _{stg}	-65 to +150	°C
Lead Temperature (8-Second Soldering)	T _L	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.

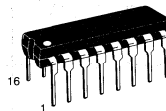
†Temperature Derating: Plastic "P and D/DW" Packages: -7.0 mW/°C From 65°C To 125°C
Ceramic "L" Packages: -12 mW/°C From 100°C To 125°C



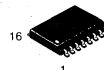
MC14415



L SUFFIX
CERAMIC
CASE 620



P SUFFIX
PLASTIC
CASE 648



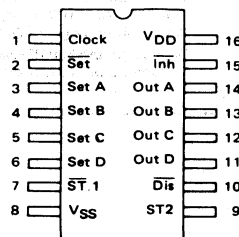
DW SUFFIX
SOIC
CASE 751G

ORDERING INFORMATION

MC14415FP (3.0 V-18 V)	Plastic
MC14415VP (3.0 V-6.0 V)	Plastic
MC14415FL (3.0 V-18 V)	Ceramic
MC14415VL (3.0 V-6.0 V)	Ceramic
MC14415DW (3.0 V-18 V)	SOIC

T_A = -55° to 125°C for all packages.

PIN ASSIGNMENT



MC14415

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V _{DD} Vdc	-55°C		25°C			125°C		Unit
			Min	Max	Min	Typ #	Max	Min	Max	
Output Voltage (No Load)	V _{OL}	5.0 10 15	—	0.01	—	0	0.01	—	0.05	Vdc
			—	0.01	—	0	0.01	—	0.05	
"1" Level	V _{OH}		5.0	—	—	3.0	4.14	—	—	
		10	—	—	8.0	9.09	—	—		
Noise Immunity ($\Delta V_{out} \leq 1.5$ Vdc) ($\Delta V_{out} \leq 3.0$ Vdc) ($\Delta V_{out} \leq 4.5$ Vdc)	V _{NL}	5.0	1.5	—	1.5	2.25	—	1.4	Vdc	
		10	3.0	—	3.0	4.50	—	2.9		
		15	—	—	—	6.75	—	—		
Noise Immunity ($\Delta V_{out} \leq 1.5$ Vdc) ($\Delta V_{out} \leq 3.0$ Vdc) ($\Delta V_{out} \leq 4.5$ Vdc)	V _{NH}	5.0	1.4	—	1.5	2.25	—	1.5	Vdc	
		10	2.9	—	3.0	4.50	—	3.0		
		15	—	—	—	6.75	—	—		
Output Drive Voltage (NPN Driver) Source (I _{OH} = 0 mA) (I _{OH} = 5.0 mA) (I _{OH} = 10 mA) (I _{OH} = 15 mA)	V _{OH}	5.0	—	—	3.0	4.14	—	—	Vdc	
			—	—	2.7	3.44	—	—		
			—	—	2.5	3.30	—	—		
	Output Drive Voltage (NPN Driver) Source (I _{OH} = 0 mA) (I _{OH} = 5.0 mA) (I _{OH} = 10 mA) (I _{OH} = 15 mA)	V _{OH}	10	—	—	8.0	9.09	—	—	Vdc
				—	—	7.7	8.45	—	—	
				—	—	7.5	8.30	—	—	
	Output Drive Voltage (NPN Driver) Source (I _{OH} = 0 mA) (I _{OH} = 5.0 mA) (I _{OH} = 10 mA) (I _{OH} = 15 mA)	V _{OH}	15	—	—	—	14.12	—	—	Vdc
				—	—	—	13.81	—	—	
				—	—	—	13.70	—	—	
Output Drive Current (V _{OL} = 0.4 Vdc) (V _{OL} = 0.5 Vdc) (V _{OL} = 1.5 Vdc)	I _{OL}	5.0	0.23	—	0.2	0.78	—	0.16	mAdc	
		10	0.60	—	0.5	2.0	—	0.40		
		15	—	—	—	7.8	—	—		
Input Leakage Current	I _{IN}	15	—	±0.3	—	±0.00001	±0.3	—	±1.0	μAdc
Input Capacitance (V _{IN} = 0)	C _{in}	—	—	—	—	5.0	—	—	—	pF
Quiescent Dissipation	P _Q	5.0	—	0.25	—	0.00005	0.25	—	3.5	mW
		10	—	1.0	—	0.00022	1.0	—	14	
		15	—	—	—	0.00050	—	—	—	
Power Dissipation** (Dynamic plus Quiescent) (C _L = 15 pF)	P _D	5.0	P _D = (56 mW/MHz) f + P _Q							mW
		10	P _D = (225 mW/MHz) f + P _Q							
		15	P _D = (510 mW/MHz) f + P _Q							

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range V_{SS} ≤ (V_{IN} or V_{OUT}) ≤ V_{DD}.
 Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).
 Unused outputs must be left open.

6

MC14415

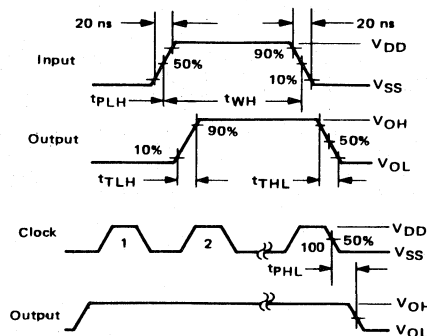
SWITCHING CHARACTERISTICS* ($C_L = 15 \text{ pF}$, $T_A = 25^\circ\text{C}$)

Characteristic	Symbol	VDD Vdc	Min	Typ #	Max	Unit
Output Rise Time $t_{TLH} = (2.0 \text{ ns/pF}) C_L + 10 \text{ ns}$ $t_{TLH} = (1.25 \text{ ns/pF}) C_L + 6 \text{ ns}$ $t_{TLH} = (1.10 \text{ ns/pF}) C_L + 3 \text{ ns}$	t_{TLH}	5.0 10 15	— — —	40 25 20	85 60 —	ns
Output Fall Time $t_{THL} = (1.5 \text{ ns/pF}) C_L + 47 \text{ ns}$ $t_{THL} = (0.75 \text{ ns/pF}) C_L + 24 \text{ ns}$ $t_{THL} = (0.55 \text{ ns/pF}) C_L + 17 \text{ ns}$	t_{THL}	5.0 10 15	— — —	70 35 25	150 80 —	ns
Turn-Off Delay Time $t_{PLH} = (2.7 \text{ ns/pF}) C_L + 560 \text{ ns}$ $t_{PHL} = (1.2 \text{ ns/pF}) C_L + 282 \text{ ns}$ $t_{PLH} = (0.91 \text{ ns/pF}) C_L + 286 \text{ ns}$	t_{PLH}	5.0 10 15	— — —	600 300 150	1200 600 —	ns
Turn-On Delay Time $t_{pHL} = (2.4 \text{ ns/pF}) C_L + 564 \text{ ns}$ $t_{pHL} = (1.0 \text{ ns/pF}) C_L + 285 \text{ ns}$ $t_{pHL} = (0.75 \text{ ns/pF}) C_L + 289 \text{ ns}$	t_{pHL}	5.0 10 15	— — —	600 300 150	1200 600 —	ns
Turn-On Delay Time (Inhibit to Output)	t_{pHL}	5.0 10 15	— — —	300 225 110	550 425 —	ns
Turn-Off Delay Time (Inhibit to Output)	t_{PLH}	5.0 10 15	— — —	300 225 110	550 425 —	ns
Input Pulse Coincidence (Figure 3)	PC_{min}	5.0 10 15	500 450 —	450 350 —	— — —	ns
Input Pulse Width (Figure 1)	t_{WH}	5.0 10 15	500 450 —	450 350 —	— — —	ns
Input Clock Frequency	f_{cl}	5.0 10 15	— — —	0.7 1.0 1.5	— — —	MHz
Clock Input Rise and Fall Times (Figure 1)	t_{TLH}, t_{THL}	5.0 10 15	— — —	— — —	15 5.0 4.0	μs

*The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

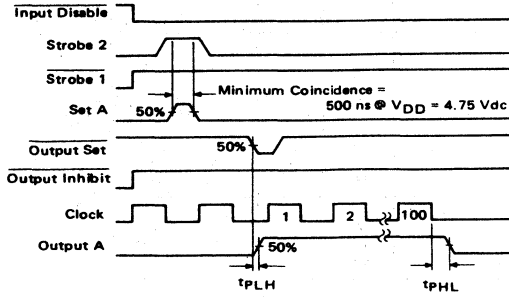
FIGURE 1 — SWITCHING CHARACTERISTICS — WAVEFORM RELATIONSHIPS



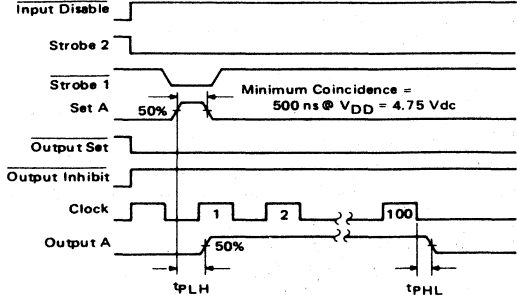
MC14415

FIGURE 2 — TYPICAL OPERATION MODES AND FUNCTIONAL TIMING DIAGRAM

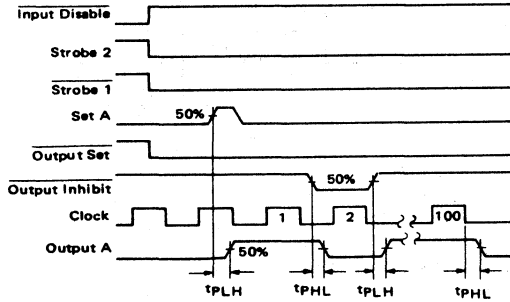
MODE 1 — OUTPUT SET INITIATES TIME DELAY



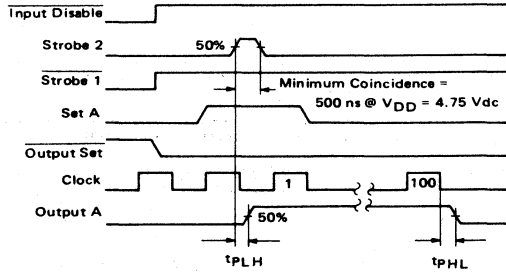
MODE 2 : SET A INITIATES TIME DELAY



MODE 3: OUTPUT INHIBIT DISABLES TIME DELAY

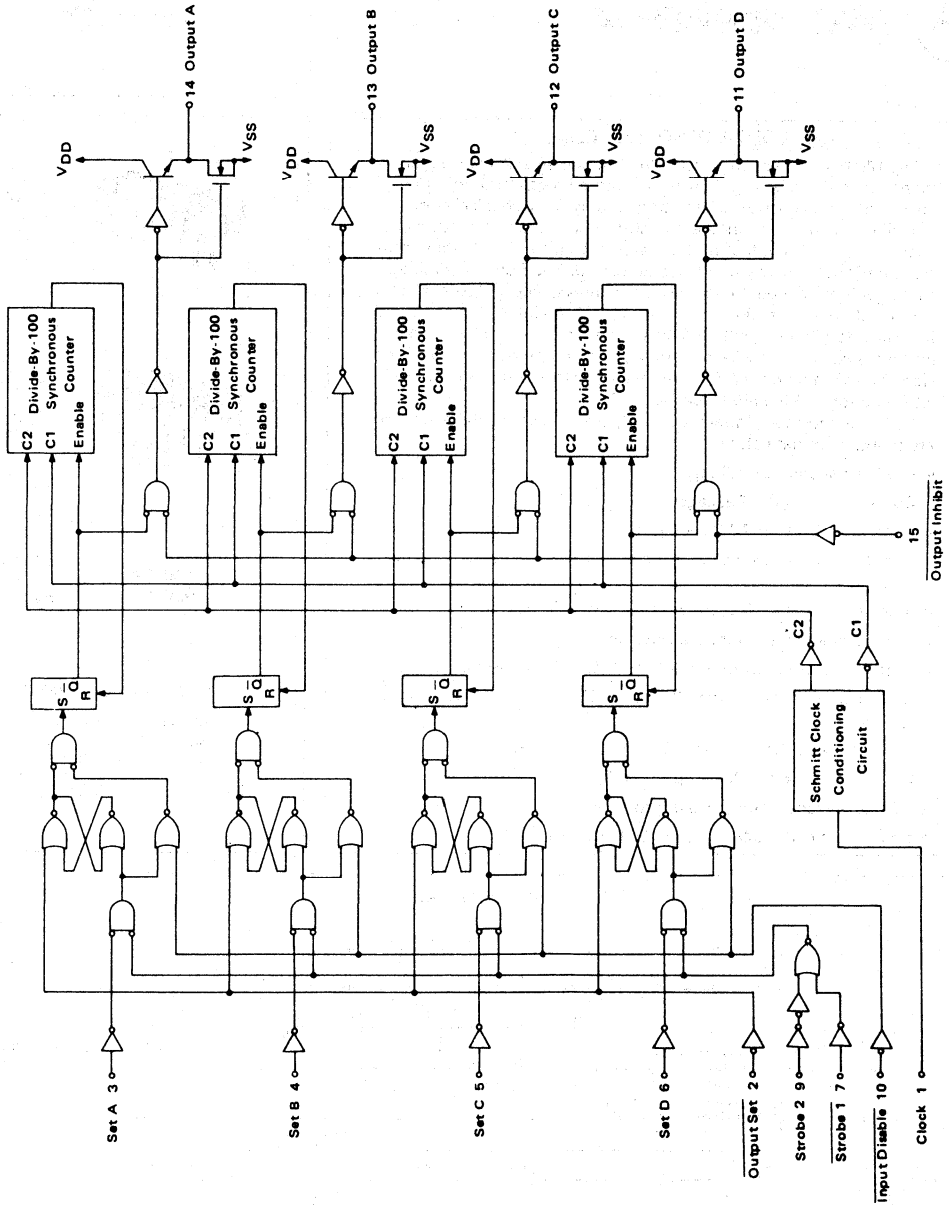


MODE 4: POSITIVE-EDGE STROBE (ST2) INITIATES TIME DELAY



MC14415

LOGIC DIAGRAM





MOTOROLA

MC14490

HEX CONTACT BOUNCE ELIMINATOR

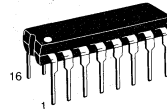
The MC14490 is constructed with complementary MOS enhancement mode devices, and is used for the elimination of extraneous level changes that result when interfacing with mechanical contacts. The digital contact bounce eliminator circuit takes an input signal from a bouncing contact and generates a clean digital signal four clock periods after the input has stabilized. The bounce eliminator circuit will remove bounce on both the "make" and the "break" of a contact closure. The clock for operation of the MC14490 is derived from an internal R-C oscillator which requires only an external capacitor to adjust for the desired operating frequency (bounce delay). The clock may also be driven from an external clock source or the oscillator of another MC14490 (see Figure 5).

NOTE: Immediately after power-up, the outputs of the MC14490 are in indeterminate states.

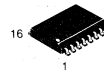
- Diode Protection on All Inputs
- Six Debouncers Per Package
- Internal Pullups on All Data Inputs
- Can Be Used as a Digital Integrator, System Synchronizer, or Delay Line
- Internal Oscillator (R-C), or External Clock Source
- TTL Compatible Data Inputs/Outputs
- Single Line Input, Debounces Both "Make" and "Break" Contacts
- Does Not Require "Form C" (Single Pole Double Throw) Input Signal
- Cascadable for Longer Time Delays
- Schmitt Trigger on Clock Input (Pin 7)
- Supply Voltage Range = 3.0 V to 18 V
- Chip Complexity: 546 FETs or 136.5 Equivalent Gates



L SUFFIX
CERAMIC
CASE 620



P SUFFIX
PLASTIC
CASE 648



DW SUFFIX
SOIC
CASE 751G

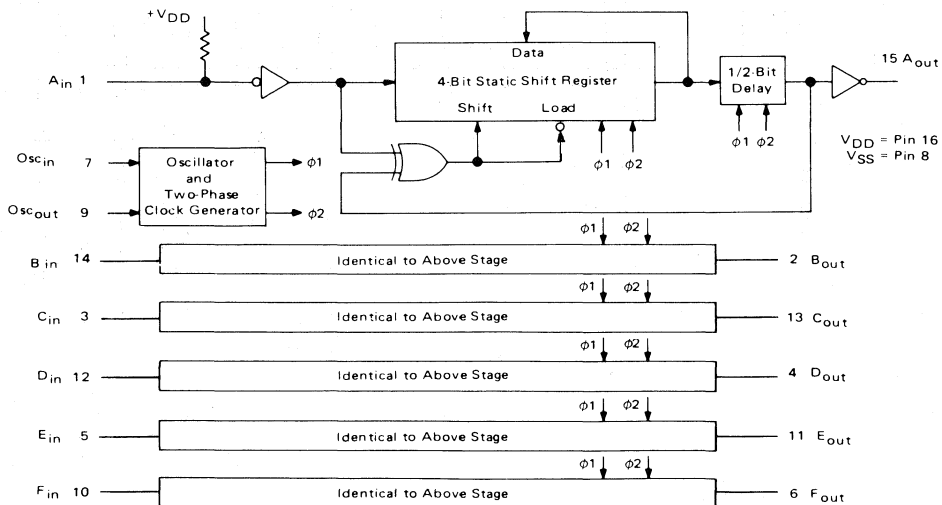
ORDERING INFORMATION

MC14490P	Plastic
MC14490L	Ceramic
MC14490DW	SOIC

T_A = -55° to 125°C for all packages.

6

BLOCK DIAGRAM



MC14490

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

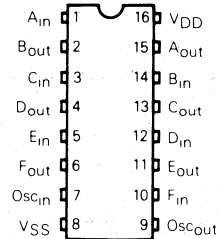
Symbol	Parameter	Value	Unit
V _{DD}	DC Supply Voltage	-0.5 to +18.0	V
V _{in} , V _{out}	Input or Output Voltage (DC or Transient)	-0.5 to V _{DD} + 0.5	V
I _{in}	Input Current (DC or Transient), per Pin	±10	mA
P _D	Power Dissipation, per Package†	500	mW
T _{stg}	Storage Temperature	-65 to +150	°C
T _L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.

†Temperature Derating: Plastic "P and D/DW" Packages: -7.0 mW/°C From 65°C To 125°C

Ceramic "L" Packages: -12 mW/°C From 100°C To 125°C

PIN ASSIGNMENT



ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V _{DD} V _{dc}	-55°C		25°C			125°C		Unit	
			Min	Max	Min	Typ #	Max	Min	Max		
Output Voltage V _{in} = V _{DD} or 0	V _{OL}	5.0	—	0.05	—	0	0.05	—	0.05	V _{dc}	
		10	—	0.05	—	0	0.05	—	0.05		
		15	—	0.05	—	0	0.05	—	0.05		
	V _{in} = 0 or V _{DD}	V _{OH}	5.0	4.95	—	4.95	5.0	—	4.95	—	V _{dc}
			10	9.95	—	9.95	10	—	9.95	—	
			15	14.95	—	14.95	15	—	14.95	—	
Input Voltage (V _O = 4.5 or 0.5 V _{dc}) (V _O = 9.0 or 1.0 V _{dc}) (V _O = 13.5 or 1.5 V _{dc})	V _{IL}	5.0	—	1.5	—	2.25	1.5	—	1.5	V _{dc}	
		10	—	3.0	—	4.50	3.0	—	3.0		
		15	—	4.0	—	6.75	4.0	—	4.0		
	(V _O = 0.5 or 4.5 V _{dc}) (V _O = 1.0 or 9.0 V _{dc}) (V _O = 1.5 or 13.5 V _{dc})	V _{IH}	5.0	3.5	—	3.5	2.75	—	3.5	—	V _{dc}
			10	7.0	—	7.0	5.50	—	7.0	—	
			15	11	—	11	8.25	—	11	—	
Output Drive Current Source Oscillator Output (V _{OH} = 2.5 V) (V _{OH} = 4.6 V) (V _{OH} = 9.5 V) (V _{OH} = 13.5 V) Debounce Outputs (V _{OH} = 2.5 V) (V _{OH} = 4.6 V) (V _{OH} = 9.5 V) (V _{OH} = 13.5 V) Sink Oscillator Output (V _{OL} = 0.4 V) (V _{OL} = 0.5 V) (V _{OL} = 1.5 V) Debounce Outputs (V _{OL} = 0.4 V) (V _{OL} = 0.5 V) (V _{OL} = 1.5 V)	I _{OH}	5.0	-0.6	—	-0.5	-1.5	—	-0.4	—	mAdc	
		5.0	-0.12	—	-0.1	-0.3	—	-0.08	—		
		10	-0.23	—	-0.2	-0.8	—	-0.16	—		
		15	-1.4	—	-1.2	-3.0	—	-1.0	—		
		5.0	-0.9	—	-0.75	2.2	—	-0.6	—		
		5.0	-0.19	—	-0.16	-0.46	—	-0.12	—		
		10	-0.6	—	-0.5	-1.2	—	-0.4	—		
		15	-1.8	—	-1.5	-4.5	—	-1.2	—		
		5.0	0.36	—	0.3	0.9	—	0.24	—		
		10	0.9	—	0.75	2.3	—	0.6	—		
		15	4.2	—	3.5	10	—	2.8	—		
		5.0	2.6	—	2.2	4.0	—	1.8	—		
		10	4.0	—	3.3	9.0	—	2.7	—		
		15	12	—	10	35	—	8.1	—		
		Input Current Debounce Inputs (V _{in} = V _{DD})	I _{IH}	15	—	2.0	—	0.2	2.0		—
Input Current Oscillator — Pin 7 (V _{in} = V _{SS} or V _{DD})	I _{in}	15	—	±620	—	±255	±400	—	±250	μAdc	
Pullup Resistor Source Current Debounce Inputs (V _{in} = V _{SS})	I _{IL}	5.0	175	375	140	190	255	70	225	μAdc	
		10	340	740	280	380	500	145	440		
		15	505	1100	415	570	750	215	660		
Input Capacitance	C _{in}	—	—	—	—	5.0	7.5	—	—	pF	
Quiescent Current (V _{in} = V _{SS} or V _{DD} , I _{out} = 0 μA)	I _{SS}	5.0	—	150	—	40	100	—	90	μAdc	
		10	—	280	—	90	225	—	180		
		15	—	840	—	225	650	—	550		

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

MC14490

SWITCHING CHARACTERISTICS ($C_L = 50 \text{ pF}$, $T_A = 25^\circ\text{C}$)

Characteristic	Symbol	VDD Vdc	Min	Typ #	Max	Unit
Output Rise Time All Outputs	t_{TLH}	5.0	—	180	360	ns
		10	—	90	180	
		15	—	65	130	
Output Fall Time Oscillator Output	t_{THL}	5.0	—	100	200	ns
		10	—	50	100	
		15	—	40	80	
Debounce Outputs	t_{THL}	5.0	—	60	120	ns
		10	—	30	60	
		15	—	20	40	
Propagation Delay Time Oscillator Input to Debounce Outputs	t_{PHL}	5.0	—	285	570	ns
		10	—	120	240	
		15	—	95	190	
	t_{PLH}	5.0	—	370	740	
		10	—	160	320	
		15	—	120	240	
Clock Frequency (50% Duty Cycle) (External Clock)	f_{cl}	5.0	—	2.8	1.4	MHz
		10	—	6	3.0	
		15	—	9	4.5	
Setup Time (See Figure 1)	t_{su}	5.0	100	50	—	ns
		10	80	40	—	
		15	60	30	—	
Maximum External Clock Input Rise and Fall Time Oscillator Input	t_r, t_f	5.0	No Limit		ns	
		10				
		15				
Oscillator Frequency OSC_{out} $C_{\text{ext}} \geq 100 \text{ pF}^*$	$f_{\text{osc, typ}}$	5.0	$\frac{1.5}{C_{\text{ext}} \text{ (in } \mu\text{F)}}$		Hz	
		10	$\frac{4.5}{C_{\text{ext}} \text{ (in } \mu\text{F)}}$			
		15	$\frac{6.5}{C_{\text{ext}} \text{ (in } \mu\text{F)}}$			
			$\frac{6.5}{C_{\text{ext}} \text{ (in } \mu\text{F)}}$			

*The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

*POWER-DOWN CONSIDERATIONS

Large values of C_{ext} may cause problems when powering down the MC14490 because of the amount of energy stored in the capacitor. When a system containing this device is powered down, the capacitor may discharge through the input protection diodes at Pin 7 or the parasitic diodes at Pin 9. Current through these internal diodes must be limited to 10 mA; therefore the turn-off time of the power supply must not be faster than $t = (V_{\text{DD}} - V_{\text{SS}}) \cdot C_{\text{ext}} / (10 \text{ mA})$. For example, if $V_{\text{DD}} - V_{\text{SS}} = 15 \text{ V}$ and $C_{\text{ext}} = 1 \mu\text{F}$, the power supply must turn off no faster than $t = (15 \text{ V}) \cdot (1 \mu\text{F}) / 10 \text{ mA} = 1.5 \text{ ms}$. This is usually not a problem because power supplies are heavily filtered and cannot discharge at this rate.

When a more rapid decrease of the power supply to zero volts occurs, the MC14490 may sustain damage. To avoid this possibility, use external clamping diodes, D1 and D2, connected as shown in Figure 2.

FIGURE 1 — SWITCHING WAVEFORMS

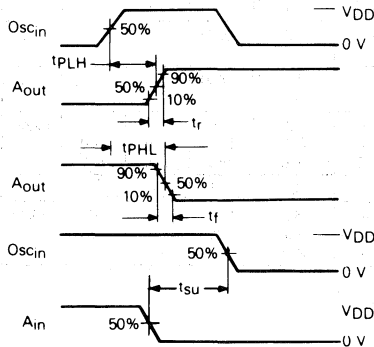
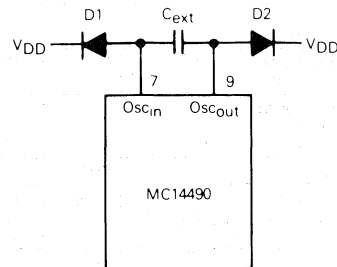


FIGURE 2 — DISCHARGE PROTECTION DURING POWER DOWN



MC14490

THEORY OF OPERATION

The MC14490 Hex Contact Bounce Eliminator is basically a digital integrator. The circuit can integrate both up and down. This enables the circuit to eliminate bounce on both the leading and trailing edges of the signal, shown in the timing diagram of Figure 3.

Each of the six Bounce Eliminators is composed of a $4\frac{1}{2}$ -bit register (the integrator) and logic to compare the input with the contents of the shift register, as shown in Figure 4. The shift register requires a series of timing pulses in order to shift the input signal into each shift register location. These timing pulses (the clock signal) are represented in the upper waveform of Figure 3. Each of the six Bounce Eliminator circuits has an internal resistor as shown in Figure 4. A pullup resistor was incorporated rather than a pulldown resistor in order to implement switched ground input signals, such as those coming from relay contacts and push buttons. By switching ground, rather than a power supply lead, system faults (such as shorts to ground on the signal input leads) will not cause excessive currents in the wiring and contacts. Signal lead shorts to ground are much more probable than shorts to a power supply lead.

When the relay contact is closed, (see Figure 4) the low level is inverted, and the shift register is loaded with a high on each positive edge of the clock signal. To understand the operation, we assume all bits of the shift register are loaded with lows and the output is at a high level.

At clock edge 1 (Figure 3) the input has gone low and a high has been loaded into the first bit or storage location of the shift register. Just after the positive edge of clock 1, the input signal has bounced back to a high. This causes the shift register to be reset to lows in all four bits — thus starting the timing sequence over again.

During clock edges 3 to 6 the input signal has stayed low. Thus, a high has been shifted into all four shift register bits and, as shown, the output goes low during the positive edge of clock pulse 6.

It should be noted that there is a $3\frac{1}{2}$ to $4\frac{1}{2}$ clock period delay between the clean input signal and output signal. In this example there is a delay of 3.8 clock periods from the beginning of the clean input signal.

After some time period of N clock periods, the contact is opened and at $N + 1$ a low is loaded into the first bit. Just after $N + 1$, when the input bounces low, all bits are set to a high. At $N + 2$ nothing happens because the input and output are low and all bits of the shift register are high. At time $N + 3$ and thereafter the input signal is a high, clean signal. At the positive edge of $N + 6$ the output goes high as a result of four lows being shifted into the shift register.

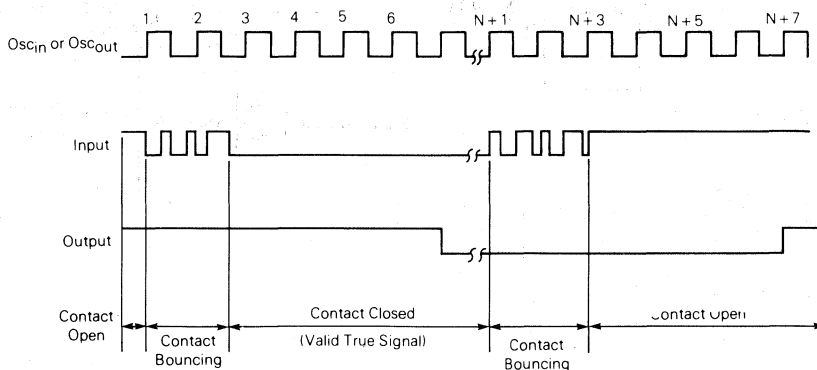
Assuming the input signal is long enough to be clocked through the Bounce Eliminator, the output signal will be no longer or shorter than the clean input signal plus or minus one clock period.

The amount of time distortion between the input and output signals is a function of the difference in bounce characteristics on the edges of the input signal and the clock frequency. Since most relay contacts have more bounce when making as compared to breaking, the overall delay, counting bounce period, will be greater on the leading edge of the input signal than on the trailing edge. Thus, the output signal will be shorter than the input signal — if the leading edge bounce is included in the overall timing calculation.

The only requirement on the clock frequency in order to obtain a bounce free output signal is that four clock periods do not occur while the input signal is in a false state. Referring to Figure 3, a false state is seen to occur three times at the beginning of the input signal. The input signal goes low three times before it finally settles down to a valid low state. The first three low pulses are referred to as false states.

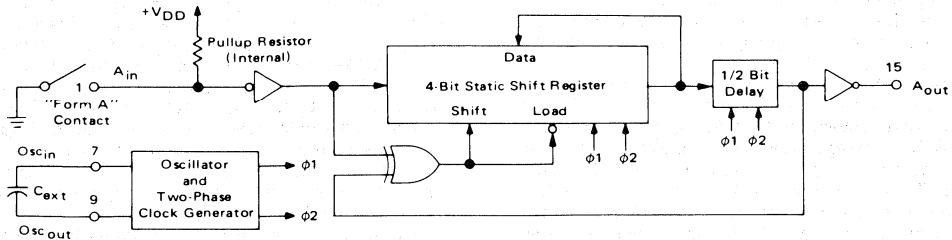
If the user has an available clock signal of the proper frequency, it may be used by connecting it to the oscillator input (pin 7). However, if an external clock is not available the user can place a small capacitor across the oscillator input and output pins in order to start up an internal clock source (as shown in Figure 4). The clock signal at the oscillator output pin may then be used to clock other MC14490 Bounce Eliminator packages. With the use of the MC14490, a large number of signals can be cleaned up, with the requirement of only one small capacitor external to the Hex Bounce Eliminator packages.

FIGURE 3 — TIMING DIAGRAM



MC14490

FIGURE 4 – TYPICAL "FORM A" CONTACT DEBOUNCE CIRCUIT
(Only One Debouncer Shown)



OPERATING CHARACTERISTICS

The single most important characteristic of the MC14490 is that it works with a single signal lead as an input, making it directly compatible with mechanical contacts (Form A and B).

The circuit has a built in pullup resistor on each input. The worst case value of the pullup resistor (determined from the Electrical Characteristics table) is used to calculate the contact wetting current. If more contact current is required, an external resistor may be connected between V_{DD} and the input.

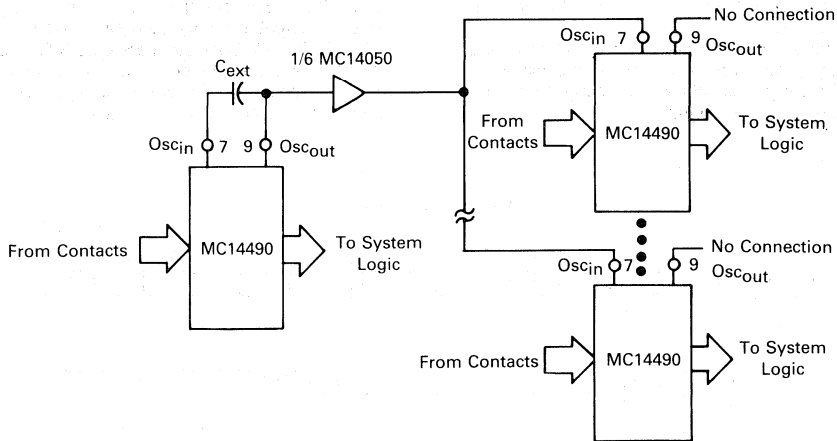
Because of the built-in pullup resistors, the inputs cannot be driven with a single standard CMOS gate when V_{DD} is below 5 V. At this voltage, the input should be driven with

paralleled standard gates or by the MC14049 or MC14050 buffers.

The clock input circuit (pin 7) has Schmitt trigger shaping such that proper clocking will occur even with very slow clock edges, eliminating any need for clock preshaping. In addition, other MC14490 oscillator inputs can be driven from a single oscillator output buffered by an MC14050 (see Figure 5). Up to six MC14490s may be driven by a single buffer.

The MC14490 is TTL compatible on both the inputs and the outputs. When V_{DD} is at 4.5 V, the buffered outputs can sink 1.6 mA at 0.4 V. The inputs can be driven with TTL as a result of the internal input pullup resistors.

FIGURE 5 – TYPICAL SINGLE OSCILLATOR DEBOUNCE SYSTEM



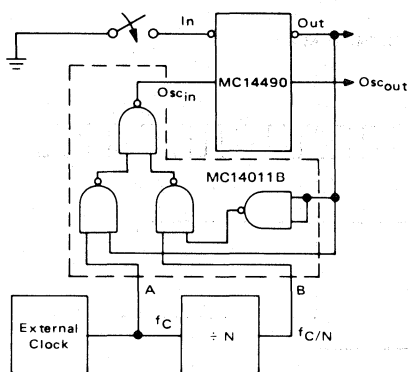
MC14490

TYPICAL APPLICATIONS

ASYMMETRICAL TIMING

In applications where different leading and trailing edge delays are required (such as a fast attack/slow release timer.) Clocks of different frequencies can be gated into the MC14490 as shown in Figure 6. In order to produce a slow attack/fast release circuit leads A and B should be interchanged. The clock out lead can then be used to feed clock signals to the other MC14490 packages where the asymmetrical input/output timing is required.

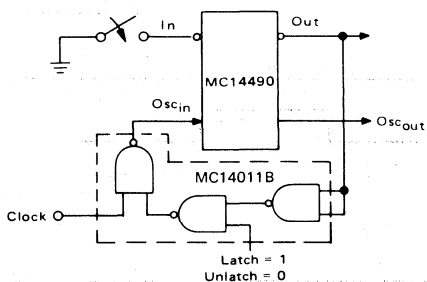
FIGURE 6 - FAST ATTACK/SLOW RELEASE CIRCUIT



LATCHED OUTPUT

The contents of the Bounce Eliminator can be latched by using several extra gates as shown in Figure 7. If the latch lead is high the clock will be stopped when the output goes low. This will hold the output low even though the input has returned to the high state. Any time the clock is stopped the outputs will be representative of the input signal four clock periods earlier.

FIGURE 7 - LATCHED OUTPUT CIRCUIT

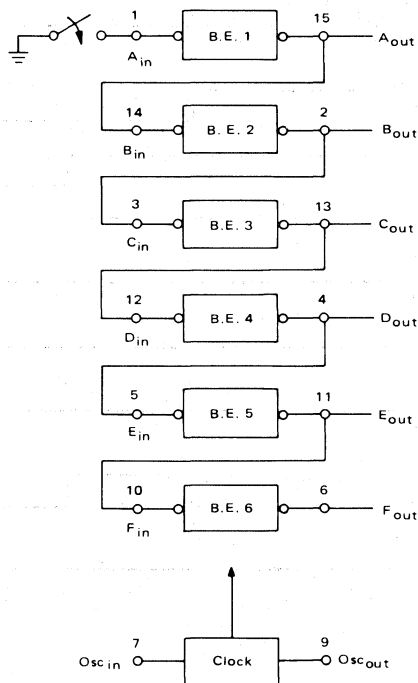


MULTIPLE TIMING SIGNALS

As shown in Figure 8, the Bounce Eliminator circuits can be connected in series. In this configuration each output is delayed by four clock periods relative to its respective input. This configuration may be used to generate multiple timing signals such as a delay line, for programming other timing operations.

One application of the above is shown in Figure 9, where it is required to have a single pulse output for a single operation (make) of the push button or relay contact. This only requires the series connection of two Bounce Eliminator circuits, one inverter, and one NOR gate in order to generate the signal \overline{AB} as shown in Figures 9 and 10. The signal \overline{AB} is four clock periods in length. If the inverter is switched to the A output, the pulse \overline{AB} will be generated upon release or break of the contact. With the use of a few additional parts many different pulses and waveshapes may be generated.

FIGURE 8 - MULTIPLE TIMING CIRCUIT CONNECTIONS



MC14490

FIGURE 9 – SINGLE PULSE OUTPUT CIRCUIT

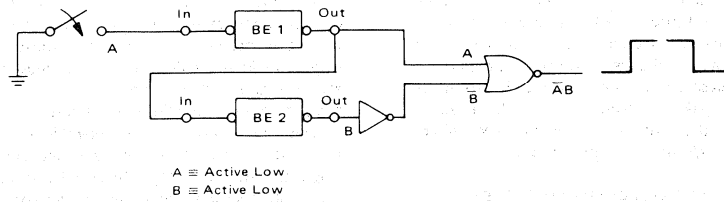
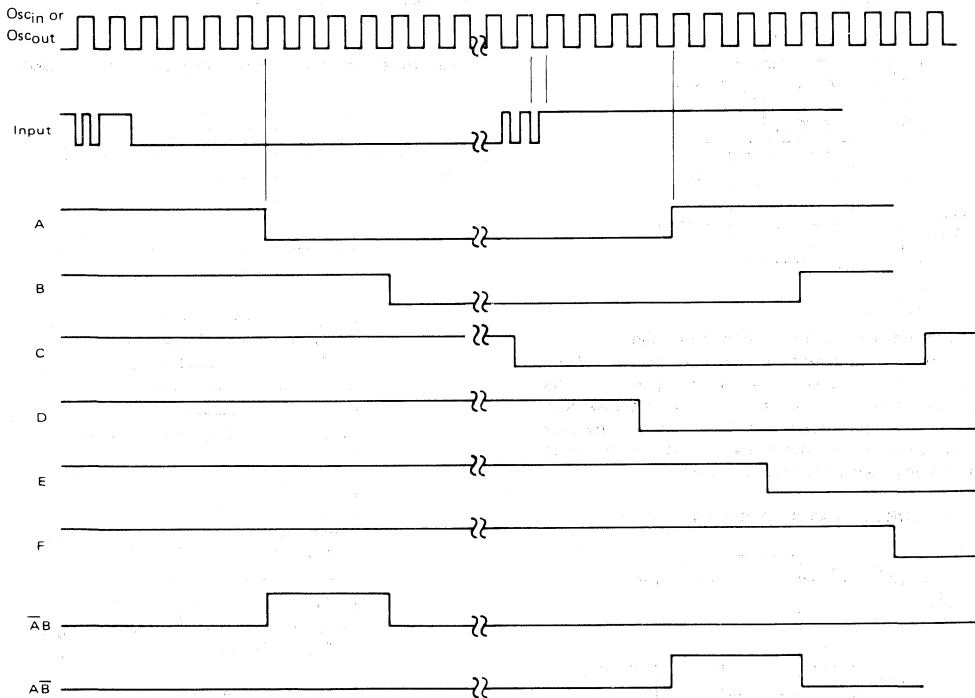


FIGURE 10 – MULTIPLE OUTPUT SIGNAL TIMING DIAGRAM



This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.



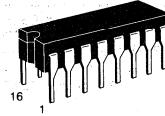
MOTOROLA

MC14500B

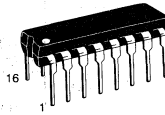
INDUSTRIAL CONTROL UNIT

The MC14500B Industrial Control Unit (ICU) is a single-bit CMOS processor. The ICU is designed for use in systems requiring decisions based on successive single-bit information. An external ROM stores the control program. With a program counter (and output latches and input multiplexers, if required) the ICU in a system forms a stored-program controller that replaces combinatorial logic. Applications include relay logic processing, serial data manipulation and control. The ICU also may control an MPU or be controlled by an MPU.

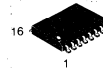
- 16 Instructions
- DC to 1.0 MHz Operation at $V_{DD} = 5\text{ V}$
- On-Chip Clock (Oscillator)
- Executes One Instruction per Clock Cycle
- 3 to 18 V Operation
- Low Quiescent Current Characteristic of CMOS Devices
- Capable of Driving One Low-Power Schottky Load or Two Low-Power TTL Loads over Full Temperature Range



**L SUFFIX
CERAMIC
CASE 620**



**P SUFFIX
PLASTIC
CASE 648**



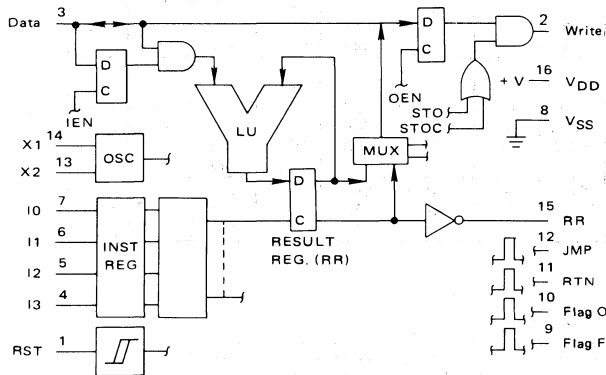
**DW SUFFIX
SOIC
CASE 751G**

ORDERING INFORMATION

MC14XXXBCP Plastic
MC14XXXBCL Ceramic
MC14XXXBDW SOIC

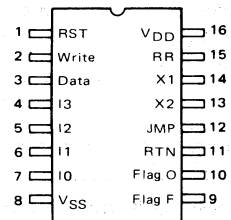
$T_A = -55^\circ\text{C}$ to 125°C for all packages.

BLOCK DIAGRAM



X1 — Oscillator Output
X2 — Oscillator Input

PIN ASSIGNMENT



MC14500B

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V _{DD}	DC Supply Voltage	-0.5 to +18.0	V
V _{in} , V _{out}	Input or Output Voltage (DC or Transient)	-0.5 to V _{DD} + 0.5	V
I _{in} , I _{out}	Input or Output Current (DC or Transient), per Pin	± 10	mA
P _D	Power Dissipation, per Package†	500	mW
T _{stg}	Storage Temperature	-65 to +150	°C
T _L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.

†Temperature Derating: Plastic "P" and D/DW" Packages: -7.0 mW/°C From 65°C To 125°C

Ceramic "L" Packages: -12 mW/°C From 100°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range V_{SS} ≤ (V_{in} or V_{out}) ≤ V_{DD}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V _{DD} Vdc	-55°C		25°C			125°C		Unit	
			Min	Max	Min	Typ #	Max	Min	Max		
Output Voltage "0" Level V _{in} = V _{DD} or 0	V _{OL}	5.0	—	0.05	—	0	0.05	—	0.05	Vdc	
		10	—	0.05	—	0	0.05	—	0.05		
		15	—	0.05	—	0	0.05	—	0.05		
	"1" Level V _{in} = 0 or V _{DD}	V _{OH}	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc
			10	9.95	—	9.95	10	—	9.95	—	
			15	14.95	—	14.95	15	—	14.95	—	
Input Voltage RST, D, X2 (V _O = 4.5 or 0.5 Vdc) (V _O = 9.0 or 1.0 Vdc) (V _O = 13.5 or 1.5 Vdc)	V _{IL}	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc	
		10	—	3.0	—	4.50	3.0	—	3.0		
		15	—	4.0	—	6.75	4.0	—	4.0		
	"1" Level (V _O = 0.5 or 4.5 Vdc) (V _O = 1.0 or 9.0 Vdc) (V _O = 1.5 or 13.5 Vdc)	V _{IH}	5.0	3.5	—	3.5	2.75	—	3.5	—	Vdc
			10	7.0	—	7.0	5.50	—	7.0	—	
			15	11	—	11	8.25	—	11	—	
Input Voltage # I0, I1, I2, I3 (V _O = 4.5 or 0.5 Vdc) (V _O = 9.0 or 1.0 Vdc) (V _O = 13.5 or 1.5 Vdc)	V _{IL}	5.0	—	0.8	—	1.1	0.8	—	0.8	Vdc	
		10	—	1.6	—	2.2	1.6	—	1.6		
		15	—	2.4	—	3.4	2.4	—	2.4		
	"1" Level (V _O = 0.5 or 4.5 Vdc) (V _O = 1.0 or 9.0 Vdc) (V _O = 1.5 or 13.5 Vdc)	V _{IH}	5.0	2.0	—	2.0	1.9	—	2.0	—	Vdc
			10	6.0	—	6.0	3.1	—	6.0	—	
			15	10	—	10	4.3	—	10	—	
Output Drive Current Data, Write (V _{OH} = 4.6 Vdc) (V _{OH} = 9.5 Vdc) (V _{OH} = 13.5 Vdc)	Source I _{OH}	5.0	-1.2	—	-1.0	-2.0	—	-0.7	—	mA _{dc}	
		10	-3.6	—	-3.0	-6.0	—	-2.1	—		
		15	-7.2	—	-6.0	-12	—	-4.2	—		
	Sink (V _{OL} = 0.4 Vdc) (V _{OL} = 0.5 Vdc) (V _{OL} = 1.5 Vdc)	I _{OL}	5.0	1.9	—	1.6	3.2	—	1.1	—	mA _{dc}
			10	3.6	—	3.0	6.0	—	2.1	—	
			15	7.2	—	6.0	12	—	4.2	—	
Output Drive Current Other Outputs (V _{OH} = 2.5 Vdc) (V _{OH} = 4.6 Vdc) (V _{OH} = 9.5 Vdc) (V _{OH} = 13.5 Vdc)	Source I _{OH}	5.0	-3.0	—	-2.4	-4.2	—	-1.7	—	mA _{dc}	
		5.0	-0.64	—	-0.51	-0.88	—	-0.36	—		
		10	-1.6	—	-1.3	-2.25	—	-0.9	—		
	Sink (V _{OL} = 0.4 Vdc) (V _{OL} = 0.5 Vdc) (V _{OL} = 1.5 Vdc)	I _{OL}	5.0	0.64	—	0.51	0.88	—	0.36	—	mA _{dc}
			10	1.6	—	1.3	2.25	—	0.9	—	
			15	4.2	—	3.4	8.8	—	2.4	—	

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

MC14500B

ELECTRICAL CHARACTERISTICS — continued (Voltages Referenced to V_{SS})

Characteristic	Symbol	V _{DD} V	-55°C		25°C			125°C		Unit
			Min	Max	Min	Typ #	Max	Min	Max	
Input Current, RST	I _{in}	15	25	—	—	150	—	—	250	μAdc
Input Current	I _{in}	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	μAdc
Input Capacitance (Data)	C _{in}	—	—	—	—	15	—	—	—	pF
Input Capacitance (All Other Inputs)	C _{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package) I _{out} = 0 μA, V _{in} = 0 or V _{DD}	I _{DD}	5.0	—	5.0	—	0.005	5.0	—	150	μAdc
		10	—	10	—	0.010	10	—	300	
		15	—	20	—	0.015	20	—	600	
**Total Supply Current at an External Load Capacitance (C _L) on All Outputs	I _T	—	$I_T = (1.5 \mu\text{A/kHz}) f + I_{DD}$ $I_T = (3.0 \mu\text{A/kHz}) f + I_{DD}$ $I_T = (4.5 \mu\text{A/kHz}) f + I_{DD}$						μAdc	

**The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

SWITCHING CHARACTERISTICS (T_A = 25°C; t_r = t_f = 20 ns for X and I inputs; C_L = 50 pF for JMP, X1, RR, Flag O, Flag F; C_L = 130 pF + 1 TTL load for Data and Write.)

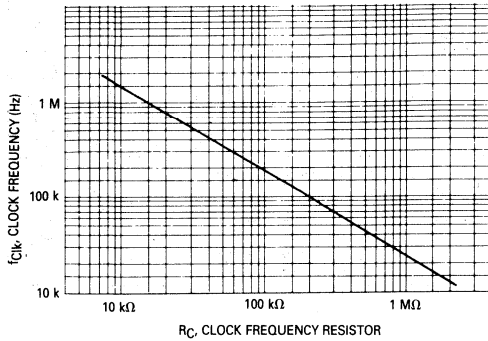
Characteristic	Symbol	V _{DD} Vdc	All Types			Unit	
			Min	Typ #	Max		
Propagation Delay Time, X1 to RR	t _{PLH} , t _{PHL}	5.0	—	250	500	ns	
		10	—	125	250		
		15	—	100	200		
X1 to Flag F, Flag O, RTN, JMP		5.0	—	200	400		
		10	—	100	200		
		15	—	85	170		
X1 to Write		5.0	—	225	450		
		10	—	125	250		
		15	—	100	200		
X1 to Data		5.0	—	250	500		
		10	—	120	240		
		15	—	100	200		
RST to RR		5.0	—	250	500		
		10	—	125	250		
		15	—	100	200		
RST to X1		5.0	—	450	Note 1		
		10	—	200			
		15	—	150			
RST to Flag F, Flag O, RTN, JMP		5.0	—	400	800		
		10	—	200	400		
		15	—	150	300		
RST to Write, Data		5.0	—	450	900		
		10	—	225	450		
		15	—	175	350		
Clock Pulse Width, X1	t _{W(c)}	5.0	400	200	—	ns	
		10	200	100	—		
		15	180	90	—		
Reset Pulse Width, RST	t _{W(R)}	5.0	500	250	—	ns	
		10	250	125	—		
		15	200	100	—		
Setup Time — Instruction	t _{su(I)}	5.0	400	200	—	ns	
		10	250	125	—		
		15	180	90	—		
	Data	t _{su(D)}	5.0	200	100		—
			10	100	50		—
			15	80	40		—
Hold Time — Instruction	t _{h(I)}	5.0	100	0	—	ns	
		10	50	0	—		
		15	50	0	—		
	Data	t _{h(D)}	5.0	200	100		—
			10	100	50		—
			15	100	50		—

NOTE 1. Maximum Reset Delay may extend to one-half clock period.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

MC14500B

FIGURE 1 – TYPICAL CLOCK FREQUENCY versus RESISTOR (R_C)



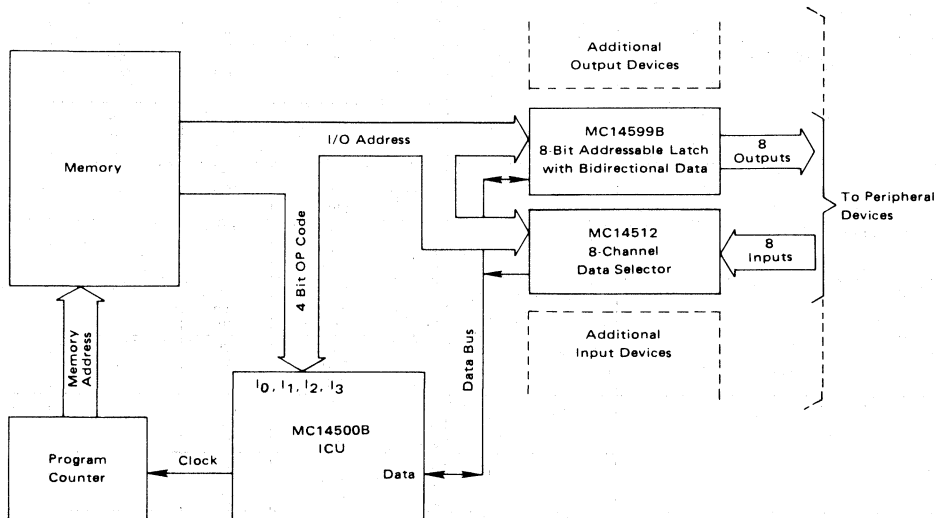
Pin No.	Function	Symbols
1	Chip Reset	RST
2	Write Pulse	Write
3	Data In/Out	Data
4	MSB Instruction Word	I ₃
5	Bit 2 Instruction Word	I ₂
6	Bit 1 Instruction Word	I ₁
7	LSB Instruction Word	I ₀
8	Negative Supply (Ground)	V _{SS}
9	Flag on NOP F	Flag F
10	Flag on NOP O	Flag O
11	Subroutine Return Flag	RTN
12	Jump Instruction Flag	JMP
13	Oscillator Input	X2
14	Oscillator Output	X1
15	Result Register	RR
16	Positive Supply	V _{DD}

TABLE 1. MC14500B INSTRUCTION SET

Instruction Code	Mnemonic	Action
0 0000	NOPO	No change in registers. RR → RR, Flag O → $\bar{1}$
1 0001	LD	Load result register. Data → RR
2 0010	LDC	Load complement. $\overline{\text{Data}}$ → RR
3 0011	AND	Logical AND. RR · Data → RR
4 0100	ANDC	Logical AND complement. RR · $\overline{\text{Data}}$ → RR
5 0101	OR	Logical OR. RR + Data → RR
6 0110	ORC	Logical OR complement. RR + $\overline{\text{Data}}$ → RR
7 0111	XNOR	Exclusive NOR. If RR = Data, RR → 1
8 1000	STO	Store. RR → Data Pin, Write → $\bar{1}$
9 1001	STOC	Store complement. $\overline{\text{RR}}$ → Data Pin, Write → $\bar{1}$
A 1010	IEN	Input enable. Data → IEN Register
B 1011	OEN	Output enable. Data → OEN Register
C 1100	JMP	Jump. JMP Flag → $\bar{1}$
D 1101	RTN	Return. RTN Flag → $\bar{1}$ and skip next instruction
E 1110	SKZ	Skip next instruction if RR = 0
F 1111	NOFP	No change in registers. RR → RR, Flag F → $\bar{1}$

6

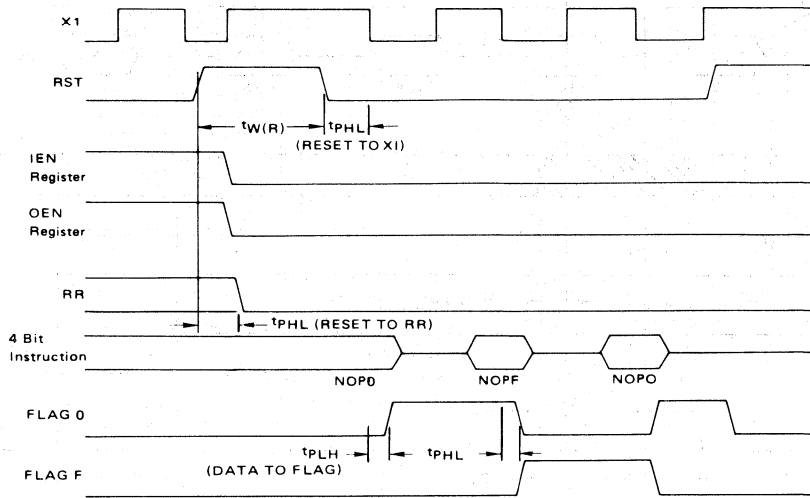
FIGURE 2 – OUTLINE OF A TYPICAL ORGANIZATION FOR A MC14500B-BASED SYSTEM



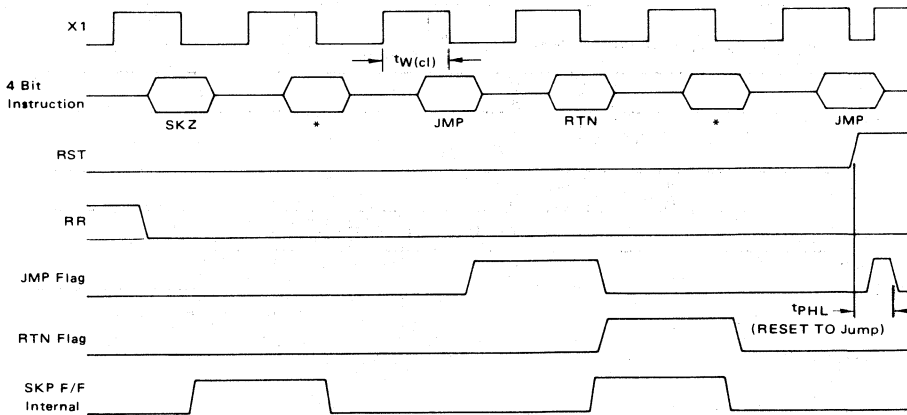
MC14500B

TIMING WAVEFORMS

Instructions **NOPO, NOPF**
RR, IEN, OEN remain unaffected



Instructions **SKZ, JMP, RTN**
RR, IEN, OEN remain unaffected

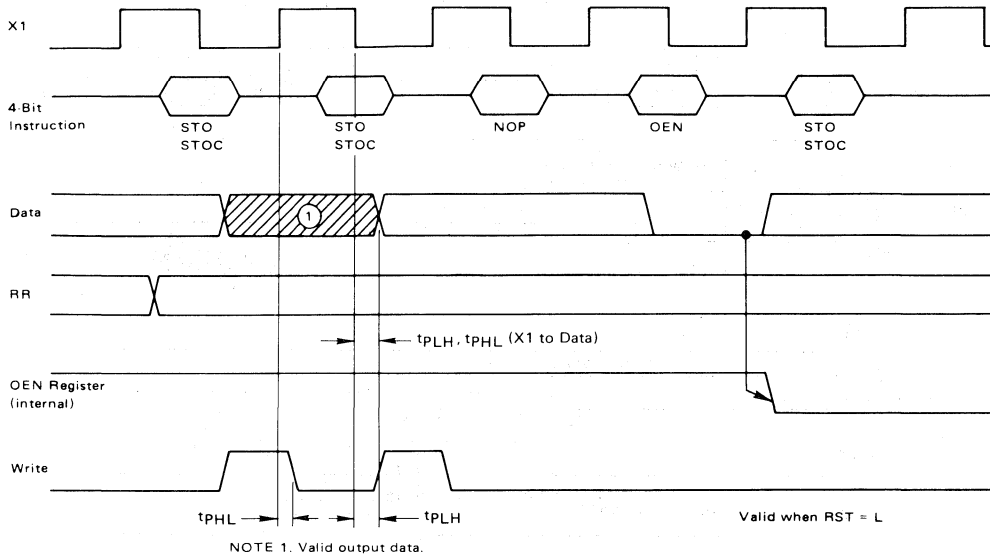


* Instructions Ignored.

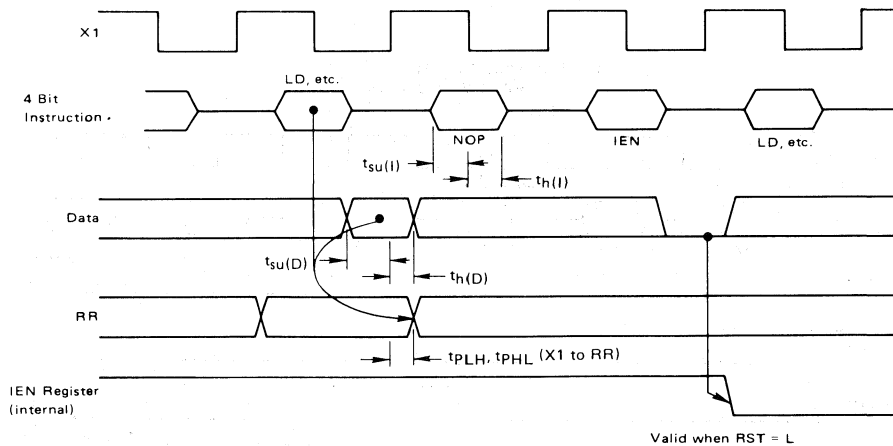
MC14500B

TIMING WAVEFORMS

Instructions STO, STOC, OEN



Instructions LD, LDC, AND, ANDC, OR, ORC, XNOR, IEN





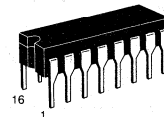
MOTOROLA

MC14501UB

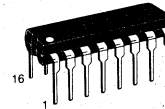
**TRIPLE GATE
DUAL 4-INPUT "NAND" GATE
2-INPUT "NOR/OR" GATE
8-INPUT "AND/NAND" GATE**

The MC14501UB is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These complementary MOS logic gates find primary use where low power dissipation and/or high noise immunity is desired. Additional characteristics can be found on the Family Data Sheet.

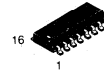
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Logic Swing Independent of Fanout
- Capable of Driving Two Low-Power TTL Loads or One Low-Power Schottky TTL Load Over the Rated Temperature Range



**L SUFFIX
CERAMIC
CASE 620**



**P SUFFIX
PLASTIC
CASE 648**



**D SUFFIX
SOIC
CASE 751B**

ORDERING INFORMATION

MC14XXXBCP Plastic
MC14XXXBCL Ceramic
MC14XXXBD SOIC

T_A = -55° to 125°C for all packages.

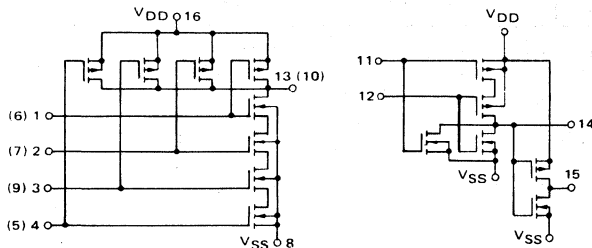
MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V _{DD}	DC Supply Voltage	-0.5 to +18.0	V
V _{in} , V _{out}	Input or Output Voltage (DC or Transient)	-0.5 to V _{DD} + 0.5	V
I _{in} , I _{out}	Input or Output Current (DC or Transient), per Pin	± 10	mA
P _D	Power Dissipation, per Package†	500	mW
T _{stg}	Storage Temperature	-65 to +150	°C
T _L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.

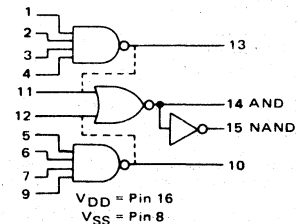
†Temperature Derating: Plastic "P and D/DW" Packages: -7.0 mW/°C From 65°C To 125°C
Ceramic "L" Packages: -12 mW/°C From 100°C To 125°C

CIRCUIT SCHEMATIC



Numbers in parenthesis are for second 4-input gate.

**LOGIC DIAGRAM
(POSITIVE LOGIC)**



Use Dotted Connection Externally to Obtain 8-Input AND/NAND

Note: Pin 14 must not be used as an input to the inverter.

6

MC14501UB

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V _{DD} Vdc	-55°C		25°C			125°C		Unit				
			Min	Max	Min	Typ #	Max	Min	Max					
Output Voltage V _{in} = V _{DD} or 0	V _{OL}	5.0 10 15	—	0.05	—	0	0.05	—	0.05	Vdc				
			—	0.05	—	0	0.05	—	0.05					
			—	0.05	—	0	0.05	—	0.05					
	V _{OH}	5.0 10 15	4.95	—	4.95	5.0	—	4.95	—	Vdc				
			9.95	—	9.95	10	—	9.95	—					
			14.95	—	14.95	15	—	14.95	—					
Input Voltage (V _O = 3.6 or 1.4 Vdc) (V _O = 7.2 or 2.8 Vdc) (V _O = 11.5 or 3.5 Vdc)	V _{IL}	5.0 10 15	—	1.5	—	2.25	1.5	—	1.4	Vdc				
			—	3.0	—	4.50	3.0	—	2.9					
			—	3.75	—	6.75	3.75	—	3.6					
	V _{IH}	5.0 10 15	3.6	—	3.5	2.75	—	3.5	—	Vdc				
			7.1	—	7.0	5.50	—	7.0	—					
			11.4	—	11.25	8.25	—	11	—					
Output Drive Current (V _{OH} = 2.5 Vdc) Source (V _{OH} = 4.6 Vdc) (V _{OH} = 9.5 Vdc) NAND* (V _{OH} = 13.5 Vdc) (V _{OH} = 2.5 Vdc) NOR (V _{OH} = 4.6 Vdc) (V _{OH} = 9.5 Vdc) (V _{OH} = 13.5 Vdc) (V _{OH} = 2.5 Vdc) NOR- (V _{OH} = 4.6 Vdc) (V _{OH} = 9.5 Vdc) Inverter (V _{OH} = 13.5 Vdc) (V _{OL} = 0.4 Vdc) Sink (V _{OL} = 0.5 Vdc) NAND* (V _{OL} = 1.5 Vdc) (V _{OL} = 0.4 Vdc) NOR (V _{OL} = 0.5 Vdc) (V _{OL} = 1.5 Vdc) (V _{OL} = 0.4 Vdc) NOR- (V _{OL} = 0.5 Vdc) Inverter (V _{OL} = 1.5 Vdc)	I _{OH}	5.0 5.0 10 15	-1.2	—	-1.0	-1.7	—	-0.7	—	mAdc				
			-0.25	—	-0.2	-0.36	—	-0.14	—					
			-0.62	—	-0.5	-0.9	—	-0.35	—					
			-1.8	—	-1.5	-3.5	—	-1.1	—					
			-2.1	—	-1.75	-3.0	—	-1.22	—					
			-0.42	—	-0.35	-0.63	—	-0.24	—					
			-1.06	—	-0.88	-1.58	—	-0.62	—					
			-3.1	—	-2.63	-6.12	—	-1.84	—					
			-3.6	—	-3.0	-5.1	—	-2.1	—					
			-0.72	—	-0.6	-1.08	—	-0.42	—					
			-1.8	—	-1.5	-2.7	—	-1.05	—					
			-5.4	—	-4.5	-10.5	—	-3.15	—					
	I _{OL}	5.0 10 15	0.64	—	0.51	0.88	—	0.36	—	mAdc				
			1.6	—	1.3	2.25	—	0.9	—					
			4.2	—	3.4	8.8	—	2.4	—					
			0.92	—	0.77	1.32	—	0.54	—					
			2.34	—	1.95	3.37	—	1.36	—					
			6.12	—	5.1	13.2	—	3.57	—					
			1.54	—	1.28	2.2	—	0.90	—					
			3.90	—	3.25	5.63	—	2.27	—					
			10.2	—	8.5	22	—	5.95	—					
			Input Current	I _{in}	15	—	±0.1	—	±0.00001		±0.1	—	±1.0	μAdc
						—	—	—	5.0		7.5	—	—	
						—	—	—	—		—	—	—	
Input Capacitance (V _{in} = 0)	C _{in}	—	—	—	—	5.0	7.5	—	—	pF				
			—	—	—	—	—	—	—					
			—	—	—	—	—	—	—					
Quiescent Current (Per Package)	I _{DD}	5.0 10 15	—	0.25	—	0.0005	0.25	—	7.5	μAdc				
			—	0.5	—	0.0010	0.5	—	15					
			—	1.0	—	0.0015	1.0	—	30					
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C _L = 50 pF on all outputs, all buffers switching)	I _T	5.0 10 15	I _T = (1.2 μA/kHz) f + I _{DD} I _T = (2.4 μA/kHz) f + I _{DD} I _T = (3.6 μA/kHz) f + I _{DD}							μAdc				

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) \text{ V/k}$$

where: I_T is in μA (per package), C_L in pF, V = (V_{DD} - V_{SS}) in volts, f in kHz is input frequency, and k = 0.004.

MC14501UB

SWITCHING CHARACTERISTICS** ($C_L = 50 \text{ pF}$, $T_A = 25^\circ\text{C}$)

Characteristic	Figure	Symbol	VDD	Typ #	Max	Unit
Output Rise Time $t_{TLH} = (3.0 \text{ ns/pF}) C_L + 30 \text{ ns}$ $t_{TLH} = (1.5 \text{ ns/pF}) C_L + 15 \text{ ns}$ $t_{TLH} = (1.1 \text{ ns/pF}) C_L + 10 \text{ ns}$	2, 3	t_{TLH}	5.0 10 15	180 90 65	360 180 130	ns
Output Fall Time $t_{THL} = (1.5 \text{ ns/pF}) C_L + 25 \text{ ns}$ $t_{THL} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$ $t_{THL} = (0.55 \text{ ns/pF}) C_L + 9.5 \text{ ns}$	2, 3	t_{THL}	5.0 10 15	100 50 40	200 100 80	ns
Output Rise Time $t_{TLH} = (1.35 \text{ ns/pF}) C_L + 32.5 \text{ ns}$ $t_{TLH} = (0.60 \text{ ns/pF}) C_L + 20 \text{ ns}$ $t_{TLH} = (0.40 \text{ ns/pF}) C_L + 17 \text{ ns}$	3	t_{TLH}	5.0 10 15	100 50 40	200 100 80	ns
Output Fall Time $t_{THL} = (0.67 \text{ ns/pF}) C_L + 26.5 \text{ ns}$ $t_{THL} = (0.45 \text{ ns/pF}) C_L + 17.5 \text{ ns}$ $t_{THL} = (0.37 \text{ ns/pF}) C_L + 11.5 \text{ ns}$	3	t_{THL}	5.0 10 15	60 40 30	120 80 60	ns
Propagation Delay Time $t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 45 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 37 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 25 \text{ ns}$	2	t_{PLH}, t_{PHL}	5.0 10 15	130 70 50	260 140 100	ns
$t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 30 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 32 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 20 \text{ ns}$	3	t_{PLH}, t_{PHL}	5.0 10 15	115 65 45	230 130 90	ns
$t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 45 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 37 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 25 \text{ ns}$	3	t_{PLH}, t_{PHL}	5.0 10 15	130 70 50	260 140 100	ns

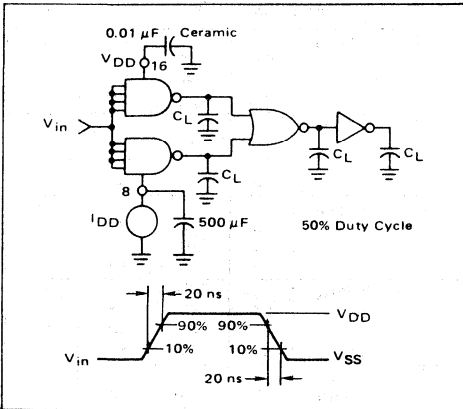
**The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

MC14501UB

FIGURE 1 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM



PIN ASSIGNMENT

1	In 1A	V _{DD}	16
2	In 2A	Out _B	15
3	In 3A	Out _B	14
4	In 4A	Out _A	13
5	In 1C	In 2B	12
6	In 2C	In 1B	11
7	In 3C	Out _C	10
8	V _{SS}	In 4C	9

FIGURE 2 – 4-INPUT “NAND” GATE SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

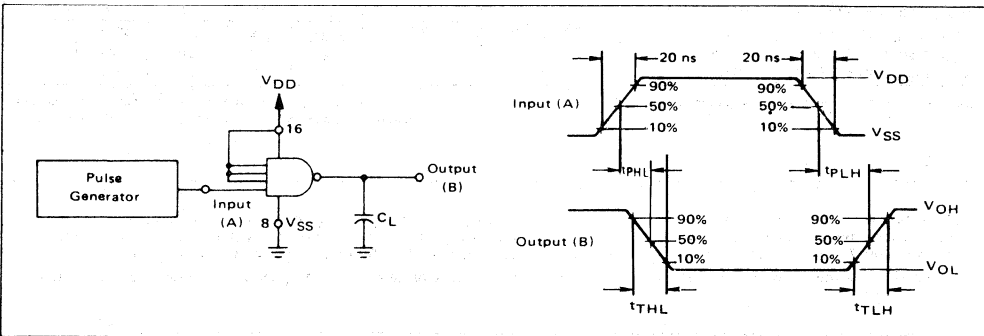
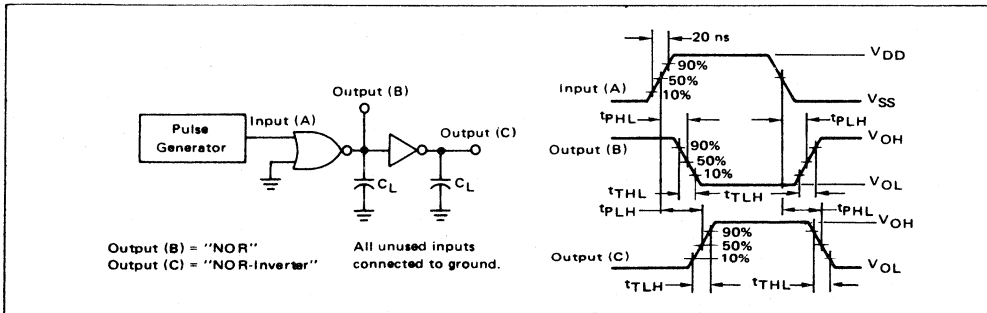


FIGURE 3 – “NOR” GATE and “NOR-INVERTER” SWITCHING TIME TEST CIRCUIT AND WAVEFORMS





MOTOROLA

MC14502B

STROBED HEX INVERTER/BUFFER

The MC14502B is a strobed hex buffer/inverter with 3-state outputs, an inhibit control, and guaranteed TTL drive over the temperature range. The 3-state output simplifies design by allowing a common bus.

- Separate Output Disable Control
- 3-State Output
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving 4LSTTL Loads Over the Rated Temperature Range

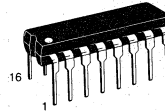
MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	-0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	-0.5 to $V_{DD} + 0.5$	V
I_{in}	Input Current (DC or Transient), per Pin	± 10	mA
I_{out}	Output Current (DC or Transient), per Pin	+30	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

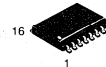
*Maximum Ratings are those values beyond which damage to the device may occur.
 †Temperature Derating: Plastic "P and D/DW" Packages: -7.0 mW/°C From 65°C To 125°C
 Ceramic "L" Packages: -12 mW/°C From 100°C To 125°C



L SUFFIX
 CERAMIC
 CASE 620



P SUFFIX
 PLASTIC
 CASE 648



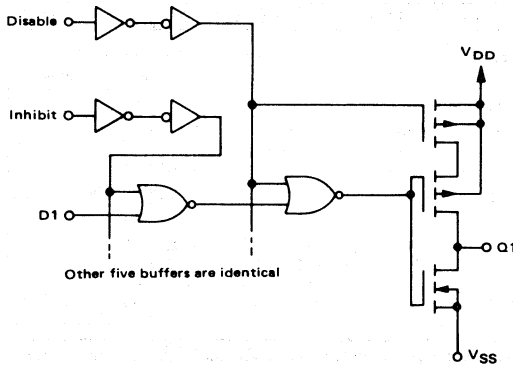
DW SUFFIX
 SOIC
 CASE 751G

ORDERING INFORMATION

MC14XXXBCP Plastic
 MC14XXXBCL Ceramic
 MC14XXXBDW SOIC

$T_A = -55^\circ\text{C}$ to 125°C for all packages.

CIRCUIT DIAGRAM

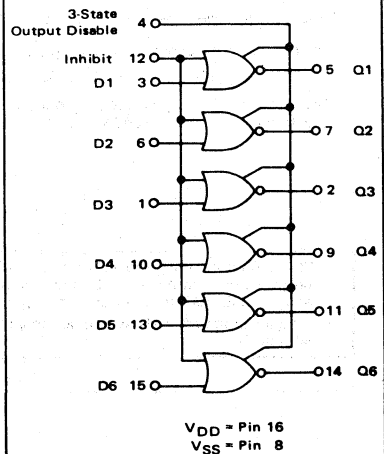


TRUTH TABLE

D_n	Inhibit	Disable	Q_n
0	0	0	1
1	0	0	0
X	1	0	0
X	X	1	High Impedance

X = Don't Care

LOGIC DIAGRAM



6

MC14502B

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V _{DD} Vdc	-55°C		25°C			125°C		Unit
			Min	Max	Min	Typ #	Max	Min	Max	
Output Voltage V _{in} = V _{DD} or 0	V _{OL}	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
		10	—	0.05	—	0	0.05	—	0.05	
V _{in} = 0 or V _{DD}	V _{OH}	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc
		10	9.95	—	9.95	10	—	9.95	—	
Input Voltage (V _O = 4.5 or 0.5 Vdc) (V _O = 9.0 or 1.0 Vdc) (V _O = 13.5 or 1.5 Vdc)	V _{IL}	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc
		10	—	3.0	—	4.50	3.0	—	3.0	
(V _O = 0.5 or 4.5 Vdc) (V _O = 1.0 or 9.0 Vdc) (V _O = 1.5 or 13.5 Vdc)	V _{IH}	5.0	3.5	—	3.5	2.75	—	3.5	—	Vdc
		10	7.0	—	7.0	5.50	—	7.0	—	
Output Drive Current (V _{OH} = 2.5 Vdc) (V _{OH} = 4.6 Vdc) (V _{OH} = 9.5 Vdc) (V _{OH} = 13.5 Vdc)	Source I _{OH}	5.0	-3.0	—	-2.4	-4.2	—	-1.7	—	mAdc
		5.0	-0.64	—	-0.51	-0.88	—	-0.36	—	
(V _{OL} = 0.4 Vdc) (V _{OL} = 0.5 Vdc) (V _{OL} = 1.5 Vdc)	Sink I _{OL}	5.0	3.5	—	2.8	6.6	—	2.0	—	mAdc
		10	7.8	—	6.3	17	—	4.4	—	
		15	29	—	24	66	—	16	—	
Input Current	I _{in}	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	μAdc
Input Capacitance (V _{in} = 0)	C _{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)	I _{DD}	5.0	—	1.0	—	0.002	1.0	—	30	μAdc
		10	—	2.0	—	0.004	2.0	—	60	
		15	—	4.0	—	0.006	4.0	—	120	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C _L = 50 pF on all outputs, all buffers switching)	I _T	5.0	I _T = (2.7 μA/kHz) f + I _{DD}							μAdc
		10	I _T = (5.3 μA/kHz) f + I _{DD}							
		15	I _T = (8.0 μA/kHz) f + I _{DD}							
Three-State Leakage Current	I _{TL}	15	—	±0.1	—	±0.00001	±0.1	—	±3.0	μAdc

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

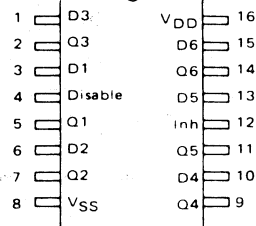
**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) V_{fk}$$

where: I_T is in μA (per package), C_L in pF, V = (V_{DD} - V_{SS}) in volts, f in kHz is input frequency, and k = 0.006.

PIN ASSIGNMENT



This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range V_{SS} ≤ (V_{in} or V_{out}) ≤ V_{DD}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

MC14502B

SWITCHING CHARACTERISTICS* ($C_L = 50 \text{ pF}$, $T_A = 25^\circ\text{C}$)

Characteristic	Symbol	VDD	All Types			Unit
			Min	Typ #	Max	
Output Rise Time	t_{TLH}	5.0	—	100	200	ns
		10	—	50	100	
		15	—	40	80	
Output Fall Time	t_{THL}	5.0	—	40	80	ns
		10	—	20	40	
		15	—	15	30	
Propagation Delay Time Data to Q	t_{PHL}	5.0	—	135	270	ns
		10	—	55	110	
		15	—	40	80	
Propagation Delay Time, Inhibit to Q	t_{PHL}	5.0	—	335	670	ns
		10	—	145	290	
		15	—	95	190	
Propagation Delay Time Data to Q, Inhibit to Q	t_{PLH}	5.0	—	295	590	ns
		10	—	130	260	
		15	—	95	190	
3-State Propagation Delay, Output "1" to High Impedance	t_{PHZ}	5.0	—	65	130	ns
		10	—	30	60	
		15	—	25	50	
3-State Propagation Delay, High Impedance to "1" Level	t_{PZH}	5.0	—	260	520	ns
		10	—	105	210	
		15	—	80	160	
3-State Propagation Delay, Output "0" to High Impedance	t_{PLZ}	5.0	—	150	300	ns
		10	—	70	140	
		15	—	55	110	
3-State Propagation Delay, High Impedance to "0" Level	t_{PZL}	5.0	—	160	320	ns
		10	—	65	130	
		15	—	50	100	

*The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

FIGURE 1 – TYPICAL OUTPUT SOURCE CURRENT TEST CIRCUIT (I_{OH})

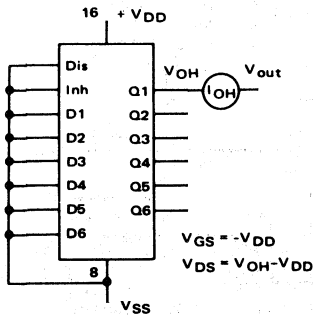
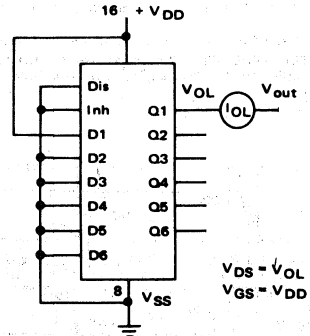


FIGURE 2 – TYPICAL OUTPUT SINK CURRENT TEST CIRCUIT (I_{OL})



MC14502B

FIGURE 3 — POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

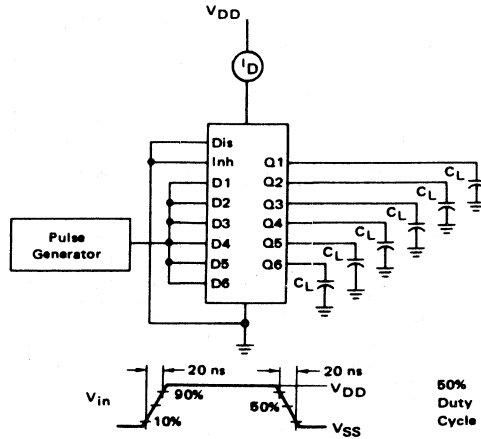
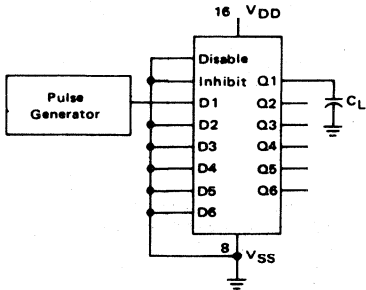


FIGURE 4 — AC TEST CIRCUIT AND WAVEFORMS (t_{TLH} , t_{THL} , t_{PLH} , and t_{PLL})



For all t_{TLH} , t_{THL} , t_{PLH} , and t_{PLL} measurements V_{in} may be applied to any other D_n input or to Inhibit.

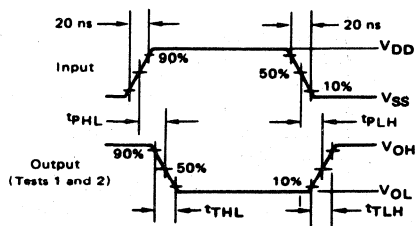
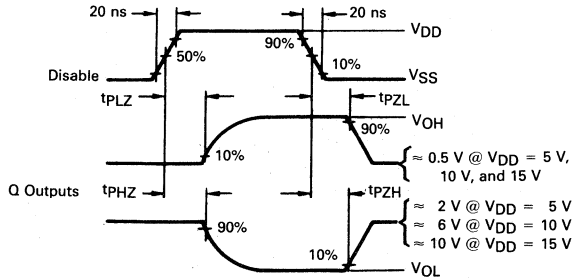
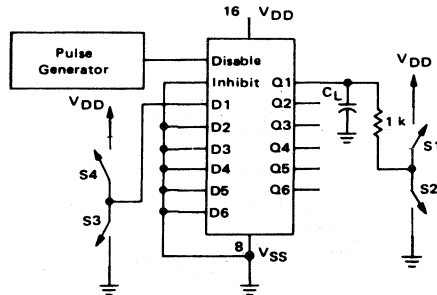


FIGURE 5 — 3-STATE AC TEST CIRCUIT AND WAVEFORMS (t_{PHZ} , t_{PLZ} , t_{PZH} , t_{PZL})

Switch Positions for 3-State Test

TEST	S1	S2	S3	S4
t_{PHZ}	Open	Closed	Closed	Open
t_{PLZ}	Closed	Open	Open	Closed
t_{PZL}	Closed	Open	Open	Closed
t_{PZH}	Open	Closed	Closed	Open





MOTOROLA

MC14503B

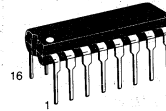
HEX NON-INVERTING 3-STATE BUFFER

The MC14503B is a hex non-inverting buffer with 3-state outputs, and a high current source and sink capability. The 3-state outputs make it useful in common bussing applications. Two disable controls are provided. A high level on the Disable A input causes the outputs of buffers 1 through 4 to go into a high impedance state and a high level on the Disable B input causes the outputs of buffers 5 and 6 to go into a high impedance state.

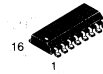
- 3-State Outputs
- TTL Compatible – Will Drive One TTL Load Over Full Temperature Range
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Two Disable Controls for Added Versatility
- Pin for Pin Replacement for MM80C97 and 340097



L SUFFIX
CERAMIC
CASE 620



P SUFFIX
PLASTIC
CASE 648



D SUFFIX
SOIC
CASE 751B

ORDERING INFORMATION

MC14XXXBCP Plastic
MC14XXXBCL Ceramic
MC14XXXBD SOIC

T_A = -55° to 125°C for all packages.

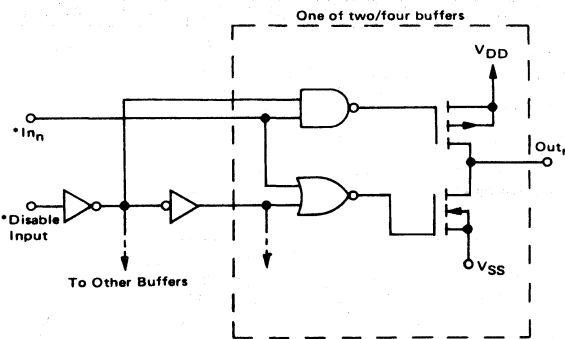
MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V _{DD}	DC Supply Voltage	-0.5 to +18.0	V
V _{in} , V _{out}	Input or Output Voltage (DC or Transient)	-0.5 to V _{DD} + 0.5	V
I _{in}	Input Current (DC or Transient), per Pin	±10	mA
I _{out}	Output Current (DC or Transient), per Pin	±25	mA
P _D	Power Dissipation, per Package†	500	mW
T _{stg}	Storage Temperature	-65 to +150	°C
T _L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.

†Temperature Derating: Plastic "P and D/DW" Packages: -7.0 mW/°C From 65°C To 125°C
Ceramic "L" Packages: -12 mW/°C From 100°C To 125°C

CIRCUIT DIAGRAM



*Diode protection on all inputs (not shown)

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,

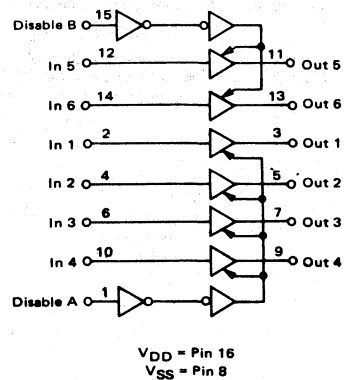
V_{in} and V_{out} should be constrained to the range V_{SS} ≤ (V_{in} or V_{out}) ≤ V_{DD}. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

TRUTH TABLE

In _n	Appropriate Disable Input	Out _n
0	0	0
1	0	1
X	1	High Impedance

X = Don't Care

LOGIC DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

MC14503B

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V _{DD} Vdc	-55°C		25°C			125°C		Unit	
			Min	Max	Min	Typ #	Max	Min	Max		
Output Voltage V _{in} = 0	V _{OL}	5.0	—	0.05	—	0	0.05	—	0.05	Vdc	
		10	—	0.05	—	0	0.05	—	0.05		
15		—	0.05	—	0	0.05	—	0.05			
V _{in} = V _{DD}	V _{OH}	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc	
		10	9.95	—	9.95	10	—	9.95	—		
		15	14.95	—	14.95	15	—	14.95	—		
Input Voltage (V _O = 3.6 or 1.4 Vdc) (V _O = 7.2 or 2.8 Vdc) (V _O = 11.5 or 3.5 Vdc)	V _{IL}	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc	
		10	—	3.0	—	4.50	3.0	—	3.0		
15		—	4.0	—	6.75	4.0	—	4.0			
(V _O = 1.4 or 3.6 Vdc) (V _O = 2.8 or 7.2 Vdc) (V _O = 3.5 or 11.5 Vdc)	V _{IH}	5.0	3.5	—	3.5	2.75	—	3.5	—	Vdc	
		10	7.0	—	7.0	5.50	—	7.0	—		
		15	11	—	11	8.25	—	11	—		
Output Drive Current (V _{OH} = 2.5 Vdc) (V _{OH} = 2.5 Vdc) (V _{OH} = 4.6 Vdc) (V _{OH} = 9.5 Vdc) (V _{OH} = 13.5 Vdc)	Source	I _{OH}	4.5	-4.3	—	-3.6	-5.0	—	-2.5	—	mAdc
			5.0	-5.8	—	-4.8	-6.1	—	-3.0	—	
5.0			-1.2	—	-1.02	-1.4	—	-0.7	—		
(V _{OL} = 0.4 Vdc) (V _{OL} = 0.4 Vdc) (V _{OL} = 0.5 Vdc) (V _{OL} = 1.5 Vdc)	Sink	I _{OL}	10	-3.1	—	-2.6	-3.7	—	-1.8	—	mAdc
			15	-8.2	—	-6.8	-14.1	—	-4.8	—	
			4.5	2.2	—	1.8	2.1	—	1.2	—	
(V _{OL} = 0.4 Vdc) (V _{OL} = 0.4 Vdc) (V _{OL} = 0.5 Vdc) (V _{OL} = 1.5 Vdc)		I _{OL}	5.0	2.6	—	2.1	2.3	—	1.3	—	mAdc
			10	6.5	—	5.5	6.2	—	3.8	—	
			10	6.5	—	5.5	6.2	—	3.8	—	
			15	19.2	—	16.1	25	—	11.2	—	
Input Current	I _{in}	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	μAdc	
Input Capacitance (V _{in} = 0)	C _{in}	—	—	—	—	5.0	7.5	—	—	pF	
Quiescent Current (Per Package)	I _Q	5.0	—	1.0	—	0.002	1.0	—	30	μAdc	
		10	—	2.0	—	0.004	2.0	—	60		
		15	—	4.0	—	0.006	4.0	—	120		
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C _L = 50 pF on all outputs) †All outputs switching, 50% Duty Cycle)	I _T	5.0	I _T = (2.5 μA/kHz) f + I _{DD}							μAdc	
		10	I _T = (6.0 μA/kHz) f + I _{DD}								
		15	I _T = (10 μA/kHz) f + I _{DD}								
Three-State Output Leakage Current	I _{TL}	15	—	±0.1	—	±0.0001	±0.1	—	±3.0	μAdc	

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) V/k$$

where: I_T is in μA (per package), C_L in pF, V = (V_{DD} - V_{SS}) in volts, f in kHz is input frequency, and k = 0.006.

MC14503B

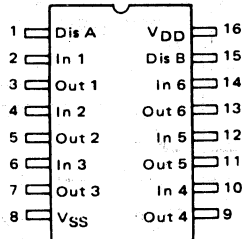
SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V _{DD} V _{CC}	All Types		Unit
			Typ #	Max	
Output Rise Time t _{TLH} = (0.5 ns/pF) C _L + 20 ns t _{TLH} = (0.3 ns/pF) C _L + 8.0 ns t _{TLH} = (0.2 ns/pF) C _L + 8.0 ns	t _{TLH}	5.0 10 15	45 23 18	90 45 35	ns
Output Fall Time t _{THL} = (0.5 ns/pF) C _L + 20 ns t _{THL} = (0.3 ns/pF) C _L + 8.0 ns t _{THL} = (0.2 ns/pF) C _L + 8.0 ns	t _{THL}	5.0 10 15	45 23 18	90 45 35	ns
Turn-Off Delay Time, all Outputs t _{PLH} = (0.3 ns/pF) C _L + 60 ns t _{PLH} = (0.15 ns/pF) C _L + 27 ns t _{PLH} = (0.1 ns/pF) C _L + 20 ns	t _{PLH}	5.0 10 15	75 35 25	150 70 50	ns
Turn-On Delay Time, all Outputs t _{PHL} = (0.3 ns/pF) C _L + 60 ns t _{PHL} = (0.15 ns/pF) C _L + 27 ns t _{PHL} = (0.1 ns/pF) C _L + 20 ns	t _{PHL}	5.0 10 15	75 35 25	150 70 50	ns
3-State Propagation Delay Time Output "1" to High Impedance	t _{PHZ}	5.0	75	150	ns
		10	40	80	
Output "0" to High Impedance	t _{PLZ}	5.0	80	160	ns
		10	40	80	
High Impedance to "1" Level	t _{PZH}	5.0	65	130	ns
		10	25	50	
High Impedance to "0" Level	t _{PZL}	5.0	100	200	ns
		10	35	70	
		15	25	50	

*The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

PIN ASSIGNMENT



MC14503B

FIGURE 1 — SWITCHING TIME TEST CIRCUIT AND WAVEFORMS
(t_{TLH} , t_{THL} , t_{PHL} , and t_{PLH})

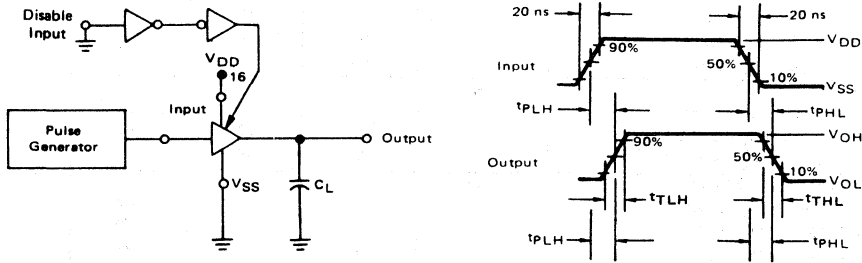
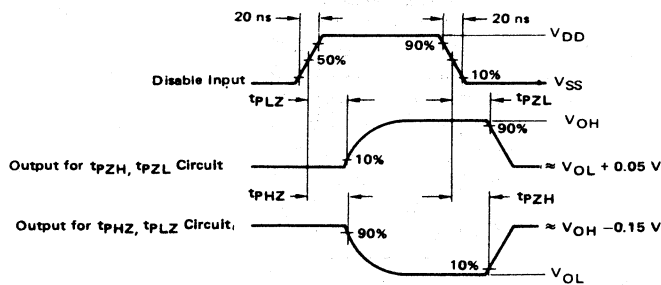
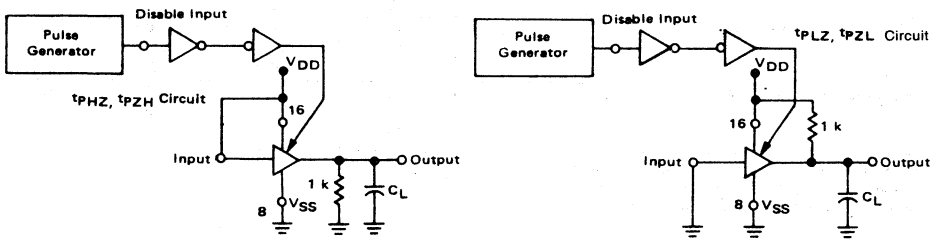


FIGURE 2 — 3 STATE AC TEST CIRCUITS AND WAVEFORMS
(t_{PLZ} , t_{PHZ} , t_{PZH} , t_{PZL})





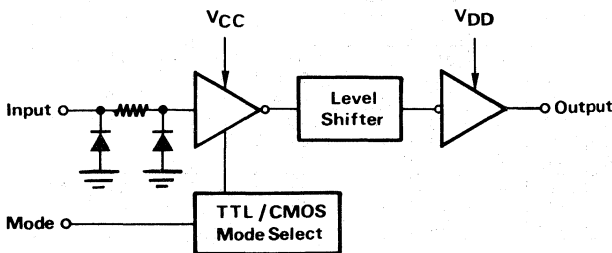
MOTOROLA

**HEX LEVEL SHIFTER FOR
TTL to CMOS or CMOS to CMOS**

The MC14504B is a hex non-inverting level shifter using CMOS technology. The level shifter will shift a TTL signal to CMOS logic levels for any CMOS supply voltage between 5 and 15 volts. A control input also allows interface from CMOS to CMOS at one logic level to another logic level. Either up or down level translating is accomplished by selection of power supply levels V_{DD} and V_{CC} . The V_{CC} level sets the input signal levels while V_{DD} selects the output voltage levels.

- UP Translates from a Low to a High Voltage or DOWN Translates from a High to a Low Voltage
- Input Threshold Can Be Shifted for TTL Compatibility
- No Sequencing Required on Power Supplies or Inputs for Power Up or Power Down
- 3 to 18 Vdc Operation for V_{DD} and V_{CC}
- Diode Protected Inputs to V_{SS}
- Capable of Driving Two Low-Power TTL Loads or One Low-Power Schottky TTL Load Over the Rated Temperature Range

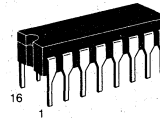
LOGIC DIAGRAM



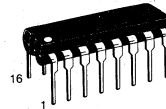
Mode Select	Input Logic Levels	Output Logic Levels
1 (V_{CC})	TTL	CMOS
0 (V_{SS})	CMOS	CMOS

1/6 of package shown.

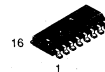
MC14504B



**L SUFFIX
CERAMIC
CASE 620**



**P SUFFIX
PLASTIC
CASE 648**



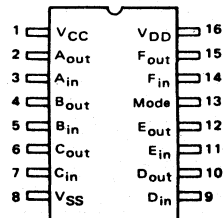
**D SUFFIX
SOIC
CASE 751B**

ORDERING INFORMATION

MC14XXXBCP Plastic
MC14XXXBCL Ceramic
MC14XXXBD SOIC

$T_A = -55^\circ$ to 125°C for all packages.

PIN ASSIGNMENT



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields **referenced to the V_{SS} pin, only**. Extra precautions must be taken to avoid applications of any voltage higher than the maximum rated voltages to this high-impedance circuit. For proper operation, the ranges $V_{SS} \leq V_{in} \leq 18\text{ V}$ and $V_{SS} \leq V_{out} \leq V_{DD}$ are recommended.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

MC14504B

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage	-0.5 to +18.0	V
V _{DD}	DC Supply Voltage	-0.5 to +18.0	V
V _{in}	Input Voltage (DC or Transient)	-0.5 to +18.0	V
V _{out}	Output Voltage (DC or Transient)	-0.5 to V _{DD} +0.5	V
I _{in} , I _{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
P _D	Power Dissipation, per Package**	500	mW
T _{stg}	Storage Temperature	-65 to +150	°C
T _L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.

†Temperature Derating: Plastic "P and D/DW" Packages: -7.0 mW/°C From 65°C To 125°C
Ceramic "L" Packages: -12 mW/°C From 100°C To 125°C

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V _{CC} Vdc	V _{DD} Vdc	-55°C		25°C			125°C		Unit	
				Min	Max	Min	Typ #	Max	Min	Max		
Output Voltage V _{in} = 0 V V _{in} = V _{CC}	V _{OL}	—	5.0	—	0.05	—	0	0.05	—	0.05	Vdc	
			10	—	0.05	—	0	0.05	—	0.05		
			15	—	0.05	—	0	0.05	—	0.05		
	V _{OH}	—	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc	
			10	9.95	—	9.95	10	—	9.95	—		
			15	14.95	—	14.95	15	—	14.95	—		
Input Voltage "0" Level (V _{OL} = 1.0 Vdc) TTL-CMOS (V _{OL} = 1.5 Vdc) TTL-CMOS (V _{OL} = 1.0 Vdc) CMOS-CMOS (V _{OL} = 1.5 Vdc) CMOS-CMOS (V _{OL} = 1.5 Vdc) CMOS-CMOS	V _{IL}	—	5.0	10	—	0.8	—	1.3	0.8	—	0.8	Vdc
			5.0	15	—	0.8	—	1.3	0.8	—	0.8	
			5.0	10	—	1.5	—	2.25	1.5	—	1.4	
			5.0	15	—	1.5	—	2.25	1.5	—	1.5	
			5.0	15	—	3.0	—	4.5	3.0	—	2.9	
			10	15	—	3.0	—	4.5	3.0	—	2.9	
Input Voltage "1" Level (V _{OH} = 9.0 Vdc) TTL-CMOS (V _{OH} = 13.5 Vdc) TTL-CMOS (V _{OH} = 9.0 Vdc) CMOS-CMOS (V _{OH} = 13.5 Vdc) CMOS-CMOS (V _{OH} = 13.5 Vdc) CMOS-CMOS	V _{IH}	—	5.0	10	2.0	—	2.0	1.5	—	2.0	—	Vdc
			5.0	15	2.0	—	2.0	1.5	—	2.0	—	
			5.0	10	3.6	—	3.5	2.75	—	3.5	—	
			5.0	15	3.6	—	3.5	2.75	—	3.5	—	
			5.0	15	7.1	—	7.0	5.5	—	7.0	—	
			10	15	7.1	—	7.0	5.5	—	7.0	—	
Output Drive Current (V _{OH} = 2.5 Vdc) (V _{OH} = 4.6 Vdc) (V _{OH} = 9.5 Vdc) (V _{OH} = 13.5 Vdc) (V _{OL} = 0.4 Vdc) (V _{OL} = 0.5 Vdc) (V _{OL} = 1.5 Vdc)	Source	I _{OH}	—	5.0	-3.0	—	-2.4	-4.2	—	-1.7	—	mAdc
			—	5.0	-0.64	—	-0.51	-0.88	—	-0.36	—	
			—	10	-1.6	—	-1.3	-2.25	—	-0.9	—	
	Sink	I _{OL}	—	5.0	0.64	—	0.51	0.88	—	0.36	—	mAdc
			—	10	1.6	—	1.3	2.25	—	0.9	—	
			—	15	4.2	—	3.4	8.8	—	2.4	—	
Input Current	I _{in}	—	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	μAdc	
Input Capacitance (V _{in} = 0)	C _{in}	—	—	—	—	—	5.0	7.5	—	—	pF	
Quiescent Current (Per Package) CMOS-CMOS Mode	I _{DD} or I _{CC}	—	5.0	—	0.05	—	0.0005	0.05	—	1.5	μAdc	
		—	10	—	0.10	—	0.0010	0.10	—	3.0		
		—	15	—	0.20	—	0.0015	0.20	—	6.0		
Quiescent Current (Per Package) TTL-CMOS Mode	I _{DD}	5.0	5.0	—	0.5	—	0.0005	0.5	—	3.8	μAdc	
		5.0	10	—	1.0	—	0.0010	1.0	—	7.5		
		5.0	15	—	2.0	—	0.0015	2.0	—	15		
Quiescent Current (Per Package) TTL-CMOS Mode	I _{CC}	5.0	5.0	—	5.0	—	2.5	5.0	—	6.0	mAdc	
		5.0	10	—	5.0	—	2.5	5.0	—	6.0		
		5.0	15	—	5.0	—	2.5	5.0	—	6.0		

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

MC14504B

SWITCHING CHARACTERISTICS ($C_L = 50 \text{ pF}$, $T_A = 25^\circ\text{C}$)

Characteristic	Symbol	Shifting Mode	V_{CC} Vdc	V_{DD} Vdc	Limits			Units
					Min	Typ #	Max	
Propagation Delay, High to Low	t_{PHL}	TTL-CMOS $V_{DD} > V_{CC}$	5.0	10	—	140	280	ns
			5.0	15	—	140	280	
		CMOS-CMOS $V_{DD} > V_{CC}$	5.0	10	—	120	240	
			5.0	15	—	120	240	
		CMOS-CMOS $V_{CC} > V_{DD}$	10	15	—	70	140	
			10	5.0	—	185	370	
Propagation Delay, Low to High	t_{PLH}	TTL-CMOS $V_{DD} > V_{CC}$	5.0	10	—	170	340	ns
			5.0	15	—	160	320	
		CMOS-CMOS $V_{DD} > V_{CC}$	5.0	10	—	170	340	
			5.0	15	—	170	340	
		CMOS-CMOS $V_{CC} > V_{DD}$	10	15	—	100	200	
			10	5.0	—	275	550	
Output Rise and Fall Time	t_{TLH} , t_{THL}	ALL	—	5.0	—	100	200	ns
			—	10	—	50	100	
			—	15	—	40	80	

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

FIGURE 1 – INPUT SWITCHPOINT CMOS to CMOS MODE

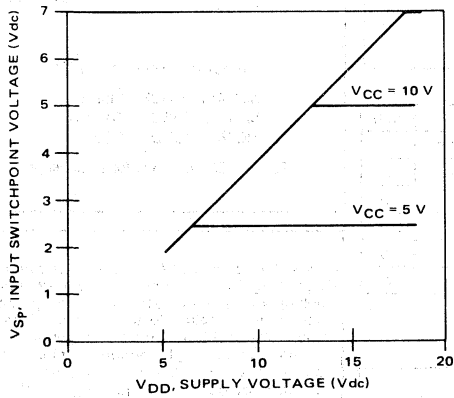


FIGURE 2 – INPUT SWITCHPOINT TTL to CMOS MODE

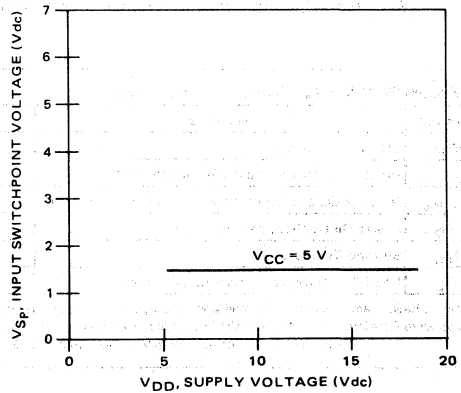


FIGURE 3 – OPERATING BOUNDARY CMOS to CMOS MODE

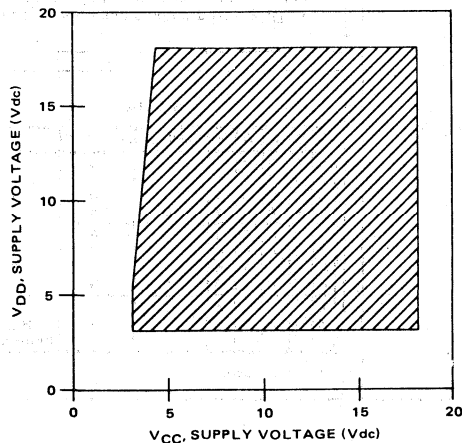
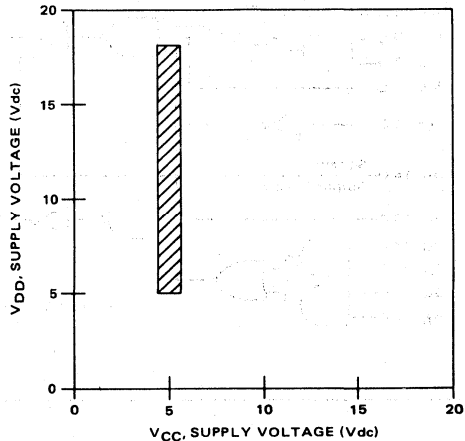


FIGURE 4 – OPERATING BOUNDARY TTL to CMOS MODE





MOTOROLA

MC14506UB

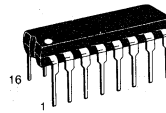
DUAL 2-WIDE, 2-INPUT EXPANDABLE AND-OR-INVERT GATE

The MC14506UB is an expandable AND-OR-INVERT gate with inhibit and 3-state output. The expand option allows cascading with any other gate, which may be carried as far as desired as long as the propagation delay added with each gate is considered. For example, the second AOI gate in this device may be used to expand the first gate, giving an expanded 4-wide, 2-input AOI gate. This device is useful in data control and digital multiplexing applications.

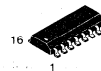
- 3-State Output
- Separate Inhibit Line
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-Power TTL Loads or One Low-Power Schottky TTL Load Over the Rated Temperature Range



L SUFFIX
CERAMIC
CASE 620



P SUFFIX
PLASTIC
CASE 648



D SUFFIX
SOIC
CASE 751B

ORDERING INFORMATION

- MC14XXXUBCP Plastic
- MC14XXXUBCL Ceramic
- MC14XXXUBD SOIC

T_A = -55° to 125°C for all packages.

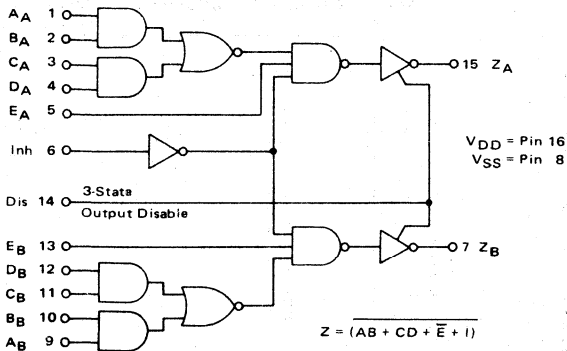
MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V _{DD}	DC Supply Voltage	-0.5 to +18.0	V
V _{in} , V _{out}	Input or Output Voltage (DC or Transient)	-0.5 to V _{DD} + 0.5	V
I _{in} , I _{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
P _D	Power Dissipation, per Package†	500	mW
T _{stg}	Storage Temperature	-65 to +150	°C
T _L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.

†Temperature Derating: Plastic "P and D/DW" Packages: -7.0 mW/°C From 65°C To 125°C
Ceramic "L" Packages: -12 mW/°C From 100°C To 125°C

LOGIC DIAGRAM



This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range V_{SS} ≤ (V_{in} or V_{out}) ≤ V_{DD}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

TRUTH TABLE

A	B	C	D	E	INHIBIT	DISABLE	Z
0	0	0	0	1	0	0	1
0	X	0	X	1	0	0	1
0	X	X	0	1	0	0	1
X	0	0	X	1	0	0	1
X	0	X	0	1	0	0	1
1	1	X	X	X	X	0	0
X	X	1	1	X	X	0	0
X	X	X	X	0	X	0	0
X	X	X	X	X	1	0	0
X	X	X	X	X	X	1	High Impedance

X = Don't Care

MC14506UB

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V _{DD} Vdc	-55°C		25°C			125°C		Unit
			Min	Max	Min	Typ #	Max	Min	Max	
Output Voltage V _{in} = V _{DD} or 0	V _{OL}	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
		10	—	0.05	—	0	0.05	—	0.05	
V _{in} = 0 or V _{DD}	V _{OH}	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc
		10	9.95	—	9.95	10	—	9.95	—	
Input Voltage (V _O = 4.5 or 0.5 Vdc) (V _O = 9.0 or 1.0 Vdc) (V _O = 13.5 or 1.5 Vdc)	V _{IL}	5.0	—	1.0	—	2.25	1.0	—	1.0	Vdc
		10	—	2.0	—	4.50	2.0	—	2.0	
(V _O = 0.5 or 4.5 Vdc) (V _O = 1.0 or 9.0 Vdc) (V _O = 1.5 or 13.5 Vdc)	V _{IH}	5.0	4.0	—	4.0	2.75	—	4.0	—	Vdc
		10	8.0	—	8.0	5.50	—	8.0	—	
Output Drive Current (V _{OH} = 2.5 Vdc) (V _{OH} = 4.6 Vdc) (V _{OH} = 9.5 Vdc) (V _{OH} = 13.5 Vdc)	I _{OH}	5.0	-3.0	—	-2.4	-4.2	—	-1.7	—	mAdc
		5.0	-0.64	—	-0.51	-0.88	—	-0.36	—	
(V _{OL} = 0.4 Vdc) (V _{OL} = 0.5 Vdc) (V _{OL} = 1.5 Vdc)	I _{OL}	5.0	0.64	—	0.51	0.88	—	0.36	—	mAdc
		10	1.6	—	1.3	2.25	—	0.9	—	
		15	4.2	—	3.4	8.8	—	2.4	—	
Input Current	I _{in}	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	μAdc
Input Capacitance (V _{in} = 0)	C _{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)	I _{DD}	5.0	—	1.0	—	0.002	1.0	—	30	μAdc
		10	—	2.0	—	0.004	2.0	—	60	
		15	—	4.0	—	0.006	4.0	—	120	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C _L = 50 pF on all outputs, all buffers switching)	I _T	5.0	I _T = (0.6 μA/kHz) f + I _{DD}							μAdc
		10	I _T = (1.1 μA/kHz) f + I _{DD}							
		15	I _T = (1.7 μA/kHz) f + I _{DD}							
Three-State Leakage Current	I _{TL}	15	—	±0.1	—	±0.00001	±0.1	—	±3.0	μAdc

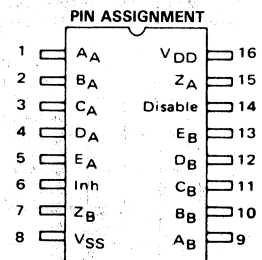
#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) Vfk$$

where: I_T is in μA (per package), C_L in pF, V = (V_{DD} - V_{SS}) in volts, f in kHz is input frequency, and k = 0.002.



MC14506UB

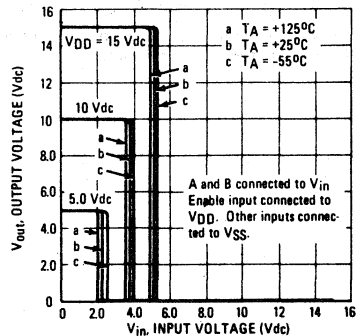
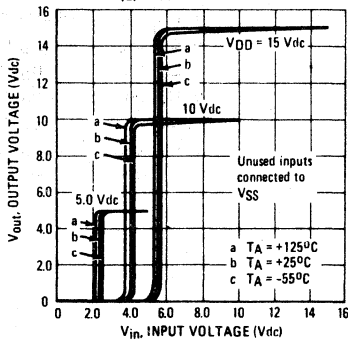
SWITCHING CHARACTERISTICS* ($C_L = 50 \text{ pF}$, $T_A = 25^\circ\text{C}$)

Characteristic	Symbol	V _{DD}	Min	Typ #	Max	Unit
Output Rise and Fall Time $t_{\text{TLH}}, t_{\text{THL}} = (1.5 \text{ ns/pF}) C_L + 25 \text{ ns}$ $t_{\text{TLH}}, t_{\text{THL}} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$ $t_{\text{TLH}}, t_{\text{THL}} = (0.55 \text{ ns/pF}) C_L + 9.5 \text{ ns}$	$t_{\text{TLH}}, t_{\text{THL}}$	5.0	—	100	200	ns
		10	—	50	100	
		15	—	40	80	
Data Propagation Delay Time $t_{\text{PLH}} = (1.7 \text{ ns/pF}) C_L + 210 \text{ ns}$ $t_{\text{PLH}} = (0.66 \text{ ns/pF}) C_L + 77 \text{ ns}$ $t_{\text{PLH}} = (0.5 \text{ ns/pF}) C_L + 50 \text{ ns}$ $t_{\text{PHL}} = (1.7 \text{ ns/pF}) C_L + 185 \text{ ns}$ $t_{\text{PHL}} = (0.66 \text{ ns/pF}) C_L + 62 \text{ ns}$ $t_{\text{PHL}} = (0.5 \text{ ns/pF}) C_L + 40 \text{ ns}$	t_{PLH}	5.0	—	295	580	ns
		10	—	110	225	
		15	—	75	180	
	t_{PHL}	5.0	—	270	480	ns
		10	—	95	175	
		15	—	65	140	
Expand Propagation Delay Time $t_{\text{PLH}} = (1.7 \text{ ns/pF}) C_L + 95 \text{ ns}$ $t_{\text{PLH}} = (0.66 \text{ ns/pF}) C_L + 42 \text{ ns}$ $t_{\text{PLH}} = (0.5 \text{ ns/pF}) C_L + 25 \text{ ns}$ $t_{\text{PHL}} = (1.7 \text{ ns/pF}) C_L + 115 \text{ ns}$ $t_{\text{PHL}} = (0.66 \text{ ns/pF}) C_L + 47 \text{ ns}$ $t_{\text{PHL}} = (0.5 \text{ ns/pF}) C_L + 30 \text{ ns}$	t_{PLH}	5.0	—	180	430	ns
		10	—	75	160	
		15	—	50	125	
	t_{PHL}	5.0	—	200	330	ns
		10	—	80	110	
		15	—	55	90	
Inhibit Propagation Delay Time $t_{\text{PLH}} = (1.7 \text{ ns/pF}) C_L + 135 \text{ ns}$ $t_{\text{PLH}} = (0.66 \text{ ns/pF}) C_L + 67 \text{ ns}$ $t_{\text{PLH}} = (0.5 \text{ ns/pF}) C_L + 40 \text{ ns}$ $t_{\text{PHL}} = (1.7 \text{ ns/pF}) C_L + 145 \text{ ns}$ $t_{\text{PHL}} = (0.66 \text{ ns/pF}) C_L + 62 \text{ ns}$ $t_{\text{PHL}} = (0.5 \text{ ns/pF}) C_L + 35 \text{ ns}$	t_{PLH}	5.0	—	220	500	ns
		10	—	100	225	
		15	—	65	160	
	t_{PHL}	5.0	—	230	400	ns
		10	—	95	175	
		15	—	60	150	
3-State Propagation Delay Time "1" to High Impedance "0" to High Impedance High Impedance to "1" High Impedance to "0"	t_{PHZ}	5.0	—	60	150	ns
		10	—	45	110	
		15	—	35	90	
	t_{PLZ}	5.0	—	90	225	ns
		10	—	55	140	
		15	—	40	100	
	t_{PZH}	5.0	—	110	300	ns
		10	—	50	125	
		15	—	40	100	
	t_{PZL}	5.0	—	170	425	ns
		10	—	70	175	
		15	—	50	125	

*The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

FIGURE 1 – TYPICAL VOLTAGE TRANSFER CHARACTERISTICS
(a) EXPAND INPUTS (b) DATA INPUTS



MC14506UB

FIGURE 2 – TYPICAL OUTPUT SOURCE CHARACTERISTICS TEST CIRCUIT

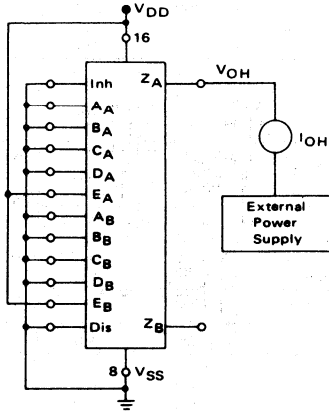


FIGURE 3 – TYPICAL OUTPUT SINK CHARACTERISTICS TEST CIRCUIT

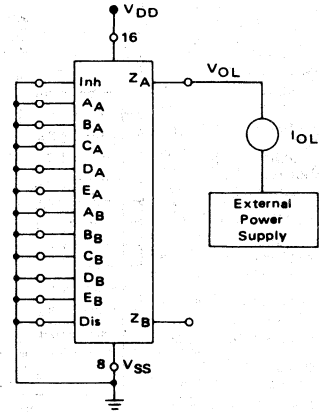


FIGURE 4 – 3-STATE LEAKAGE CURRENT TEST CIRCUIT

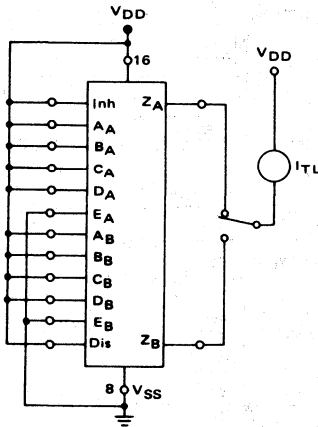
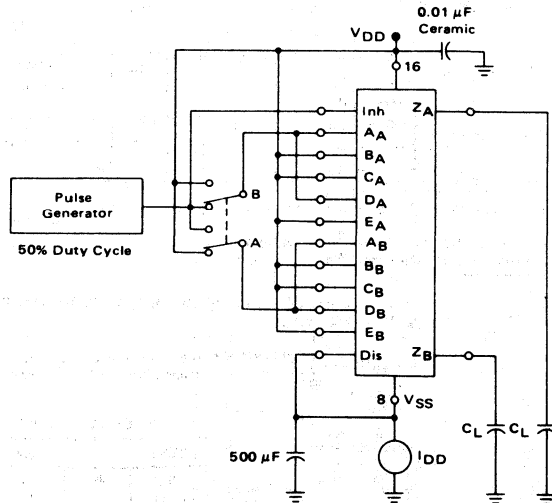


FIGURE 5 – TYPICAL POWER DISSIPATION TEST CIRCUIT



MC14506UB

FIGURE 6 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS (Data Inputs)

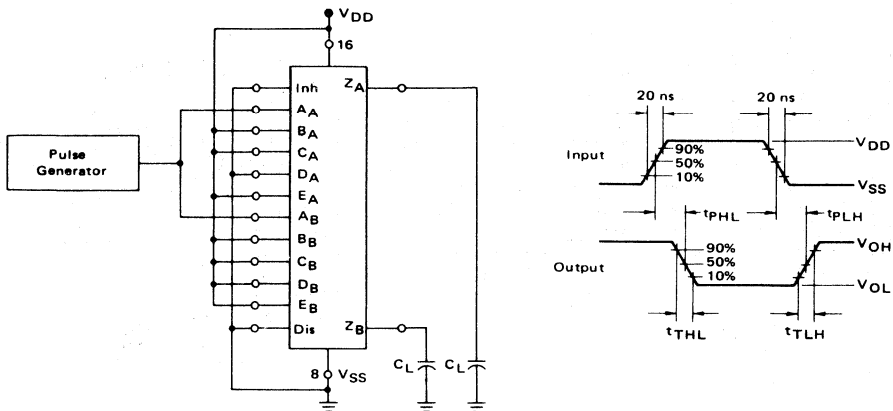
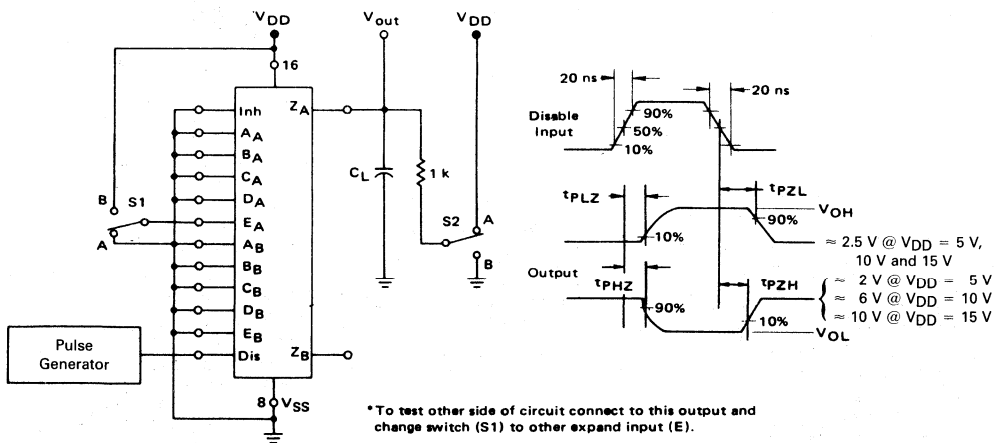


FIGURE 7 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS (For 3-State Output)



SWITCH POSITIONS

TEST	S1	S2
t _{PLZ}	A	A
t _{PHZ}	B	B
t _{PZL}	A	A
t _{PZH}	B	B

6



MOTOROLA

MC14508B

DUAL 4-BIT LATCH

The MC14508B dual 4-bit latch is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. The part consists of two identical, independent 4-bit latches with separate Strobe (ST) and Master Reset (MR) controls. Separate Disable inputs force the outputs to a high impedance state and allow the devices to be used in time sharing bus line applications.

These complementary MOS latches find primary use in buffer storage, holding register, or general digital logic functions where low power dissipation and/or high noise immunity is desired.

- 3-State Output
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load over the Rated Temperature Range.

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V _{DD}	DC Supply Voltage	-0.5 to +18.0	V
V _{in} , V _{out}	Input or Output Voltage (DC or Transient)	-0.5 to V _{DD} + 0.5	V
I _{in} , I _{out}	Input or Output Current (DC or Transient), per Pin	± 10	mA
P _D	Power Dissipation, per Package†	500	mW
T _{stg}	Storage Temperature	-65 to +150	°C
T _L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.

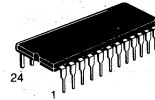
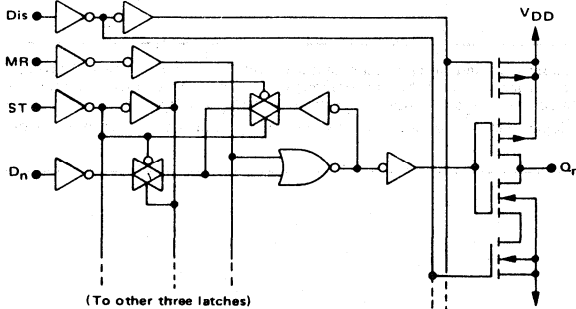
†Temperature Derating: Plastic "P and D/DW" Packages: -7.0 mW/°C From 65°C To 125°C
Ceramic "L" Packages: -12 mW/°C From 100°C To 125°C

TRUTH TABLE

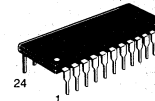
MR	ST	Disable	D3	D2	D1	D0	Q3	Q2	Q1	Q0
0	1	0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	1	0	0	0	1
0	1	0	0	0	1	0	0	0	1	0
0	1	0	0	1	0	0	0	1	0	0
0	1	0	1	0	0	0	1	0	0	0
0	0	0	X	X	X	X	Latched			
1	X	0	X	X	X	X	0	0	0	0
X	X	1	X	X	X	X	High Impedance			

X = Don't Care

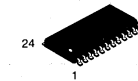
CIRCUIT DIAGRAM



L SUFFIX
CERAMIC
CASE 623



P SUFFIX
PLASTIC
CASE 709



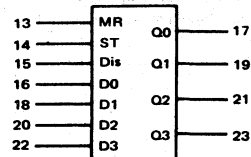
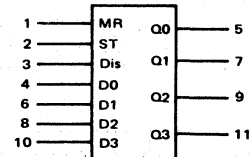
DW SUFFIX
SOIC
CASE 751E

ORDERING INFORMATION

MC14XXXBCP Plastic
MC14XXXBCL Ceramic
MC14XXXBDW SOIC

T_A = -55° to 125°C for all packages.

BLOCK DIAGRAM



V_{DD} = Pin 24
V_{SS} = Pin 12

MC14508B

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V _{DD} Vdc	-55°C		25°C			125°C		Unit	
			Min	Max	Min	Typ #	Max	Min	Max		
Output Voltage V _{in} = V _{DD} or 0	V _{OL}	5.0	—	0.05	—	0	0.05	—	0.05	Vdc	
		10	—	0.05	—	0	0.05	—	0.05		
15		—	0.05	—	0	0.05	—	0.05	0.05		
V _{in} = 0 or V _{DD}	V _{OH}	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc	
		10	9.95	—	9.95	10	—	9.95	—		
		15	14.95	—	14.95	15	—	14.95	—		
Input Voltage (V _O = 4.5 or 0.5 Vdc) (V _O = 9.0 or 1.0 Vdc) (V _O = 13.5 or 1.5 Vdc)	V _{IL}	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc	
		10	—	3.0	—	4.50	3.0	—	3.0		
		15	—	4.0	—	6.75	4.0	—	4.0		
	V _{in} = 0 or V _{DD}	V _{IH}	5.0	3.5	—	3.5	2.75	—	3.5	—	Vdc
			10	7.0	—	7.0	5.50	—	7.0	—	
			15	11	—	11	8.25	—	11	—	
Output Drive Current (V _{OH} = 2.5 Vdc) (V _{OH} = 4.6 Vdc) (V _{OH} = 9.5 Vdc) (V _{OH} = 13.5 Vdc)	Source	I _{OH}	5.0	-3.0	—	-2.4	-4.2	—	-1.7	—	mAdc
			10	-0.64	—	-0.51	-0.88	—	-0.36	—	
			15	-1.6	—	-1.3	-2.25	—	-0.9	—	
	Sink	I _{OL}	5.0	0.64	—	0.51	0.88	—	0.36	—	mAdc
			10	1.6	—	1.3	2.25	—	0.9	—	
			15	4.2	—	3.4	8.8	—	2.4	—	
Input Current	I _{in}	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	μAdc	
Input Capacitance (V _{in} = 0)	C _{in}	—	—	—	—	5.0	7.5	—	—	pF	
Quiescent Current (Per Package)	I _{DD}	5.0	—	5.0	—	0.005	5.0	—	150	μAdc	
		10	—	10	—	0.010	10	—	300		
		15	—	20	—	0.015	20	—	600		
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C _L = 50 pF on all outputs, all buffers switching)	I _T	5.0	I _T = (1.46 μA/kHz) f + I _{DD}						μAdc		
		10	I _T = (2.91 μA/kHz) f + I _{DD}								
		15	I _T = (4.37 μA/kHz) f + I _{DD}								
Three-State Leakage Current	I _{TL}	15	—	±0.1	—	±0.00001	±0.1	—	±3.0	μAdc	

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) V/k$$

where: I_T is in μA (per package), C_L in pF, V = (V_{DD} - V_{SS}) in volts, f in kHz is input frequency, and k = 0.008.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range V_{SS} ≤ (V_{in} or V_{out}) ≤ V_{DD}. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

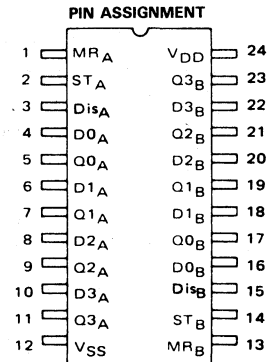
MC14508B

SWITCHING CHARACTERISTICS* ($C_L = 50 \text{ pF}$, $T_A = 25^\circ\text{C}$)

Characteristic	Symbol	V_{DD}	All Types			Unit
			Min	Typ #	Max	
Output Rise and Fall Time t_{TLH} , $t_{THL} = (1.5 \text{ ns/pF}) C_L + 25 \text{ ns}$ t_{TLH} , $t_{THL} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$ t_{TLH} , $t_{THL} = (0.55 \text{ ns/pF}) C_L + 9.5 \text{ ns}$	t_{TLH} , t_{THL}	5.0 10 15	— — —	100 50 40	200 100 80	ns
Propagation Delay Time, Dn or MR to Q t_{PLH} , $t_{PHL} = (1.7 \text{ ns/pF}) C_L + 135 \text{ ns}$ t_{PLH} , $t_{PHL} = (0.66 \text{ ns/pF}) C_L + 57 \text{ ns}$ t_{PLH} , $t_{PHL} = (0.5 \text{ ns/pF}) C_L + 35 \text{ ns}$	t_{PLH} , t_{PHL}	5.0 10 15	— — —	220 90 60	440 180 120	ns
Master Reset Pulse Width	$t_{WH(R)}$	5.0 10 15	200 100 70	100 50 35	— — —	ns
Master Reset Removal Time	t_{rem}	5.0 10 15	30 25 20	-15 0 0	— — —	ns
Strobe Pulse Width	$t_{WH(S)}$	5.0 10 15	140 70 40	70 35 20	— — —	ns
Setup Time Data to Strobe	t_{su}	5.0 10 15	50 20 10	25 10 5.0	— — —	ns
Hold Time Strobe to Data	t_h	5.0 10 15	50 35 35	20 10 10	— — —	ns
3-State Propagation Delay Time Output "1" to High Impedance	t_{PHZ}	5.0 10 15	— — —	55 35 30	170 100 70	ns
Output "0" to High Impedance	t_{PLZ}	5.0 10 15	— — —	75 40 35	170 100 70	
High Impedance to "1" Level	t_{PZH}	5.0 10 15	— — —	80 35 30	170 100 70	
High Impedance to "0" Level	t_{PZL}	5.0 10 15	— — —	105 50 35	210 100 70	

*The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.



MC14508B

FIGURE 1 – AC WAVEFORMS

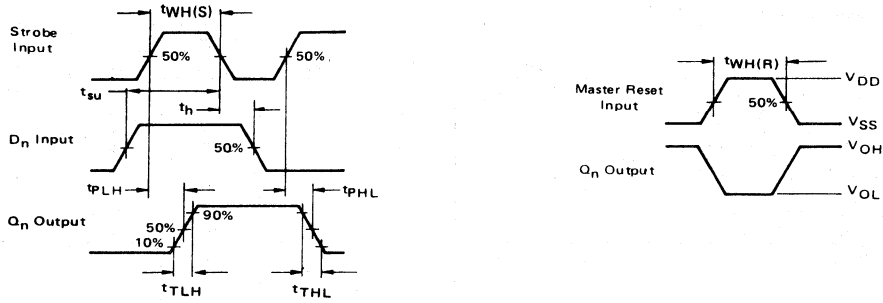
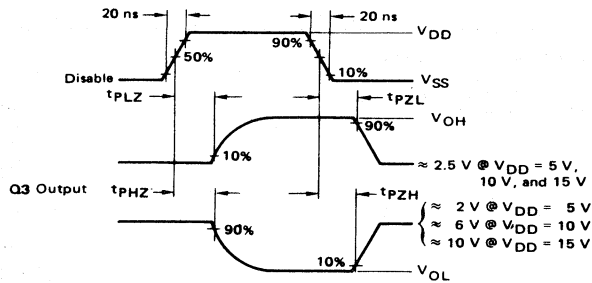
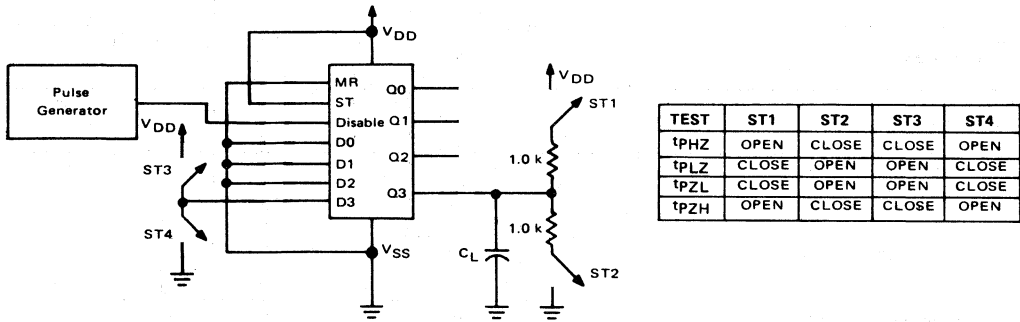


FIGURE 2 – 3-STATE AC TEST CIRCUIT AND WAVEFORMS



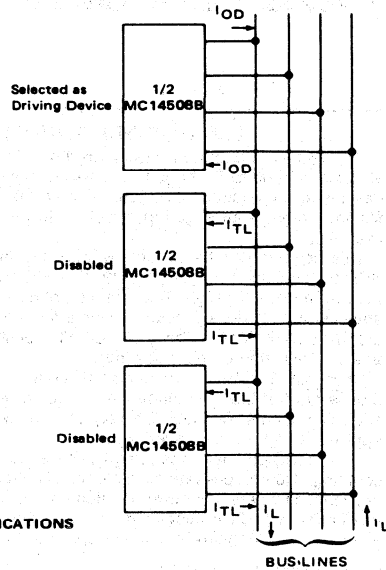
MC14508B

3-STATE MODE OF OPERATION

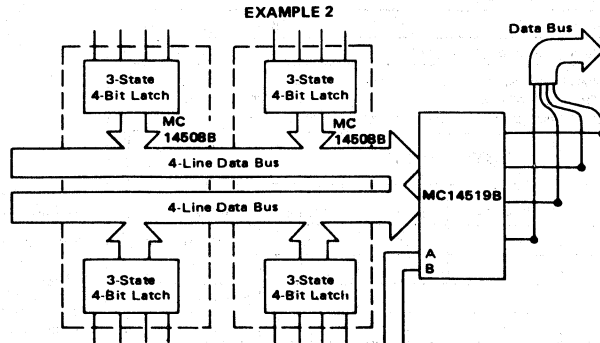
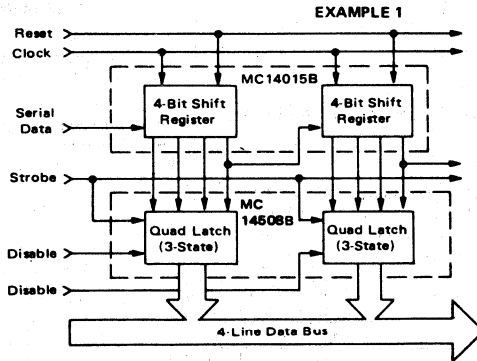
The MC14508B can be used in bussed systems as shown. The output terminals of N 4-bit latches can be directly wired to a bus line, and to one of the 4-bit latches selected. The selected latch controls the logic state of the bus line, and the remaining (N-1) 4-bit latches are disabled into a high impedance "off" state. The number of latches, N, which may be connected to a bus line is determined from the output drive current, I_{OD} , the 3-state or disabled output leakage current, I_{TL} , and the load current, I_L , required to drive the bus line (including fanout to other device inputs) and can be calculated by the following:

$$N = \frac{I_{OD} - I_L}{I_{TL}} + 1$$

N must be calculated for both high and low logic states of the bus line.



TYPICAL 3-STATE APPLICATIONS



MC14510B

BCD UP/DOWN COUNTER

The MC14510B synchronous up/down BCD counter is constructed with MOS P-channel and N-channel enhancement mode devices in a monolithic structure. The counter consists of type D flip-flop stages with a gating structure to provide type T flip-flop capability.

This counter can be preset by applying the desired value in BCD to the Preset inputs (P1, P2, P3, P4) and then bringing the Preset Enable (PE) high. The direction of counting is controlled by applying a high (for up counting) or a low (for down counting) to the UP/DOWN input. The state of the counter changes on the positive transition of the clock input.

Cascading can be accomplished by connecting the Carry Out to the Carry In of the next stage while clocking each counter in parallel. The outputs (Q1, Q2, Q3, Q4) can be reset to a low state by applying a high to the Reset (R) pin.

This CMOS counter finds primary use in up/down and difference counting. Other applications include: (1) Frequency synthesizer applications where low power dissipation and/or high noise immunity is desired, (2) Analog-to-digital and digital-to-analog conversions, and (3) Magnitude and sign generation.

- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Internally Synchronous for High Speed
- Logic Edge-Clocked Design – Count Occurs on Positive Going Edge of Clock
- Asynchronous Preset Enable Operation
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range.



MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V _{DD}	DC Supply Voltage	-0.5 to +18.0	V
V _{in} , V _{out}	Input or Output Voltage (DC or Transient)	-0.5 to V _{DD} + 0.5	V
I _{in} , I _{out}	Input or Output Current (DC or Transient), per Pin	± 10	mA
P _D	Power Dissipation, per Package†	500	mW
T _{stg}	Storage Temperature	-65 to +150	°C
T _L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.

†Temperature Derating: Plastic "P and D/DW" Packages: -7.0 mW/°C From 65°C To 125°C
Ceramic "L" Packages: -12 mW/°C From 100°C To 125°C

TRUTH TABLE

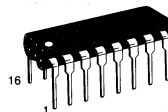
Carry In	Up/Down	Preset Enable	Reset	Clock	Action
1	X	0	0	X	No Count
0	1	0	0		Count Up
0	0	0	0		Count Down
X	X	1	0	X	Preset
X	X	X	1	X	Reset

X = Don't Care

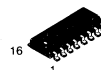
Note: When counting up, the Carry Out signal is normally high, and is low only when Q1 and Q4 are high and Carry In is low. When counting down, Carry Out is low only when Q1 through Q4 and Carry In are low.



L SUFFIX
CERAMIC
CASE 620



P SUFFIX
PLASTIC
CASE 648



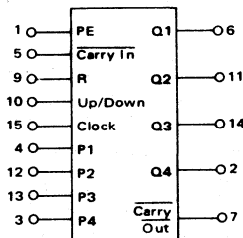
D SUFFIX
SOIC
CASE 751B

ORDERING INFORMATION

MC14XXXBCP Plastic
MC14XXXBCL Ceramic
MC14XXXBD SOIC

T_A = -55° to 125°C for all packages.

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range V_{SS} ≤ (V_{in} or V_{out}) ≤ V_{DD}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

MC14510B

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V _{DD} V _d c	-55°C		25°C			125°C		Unit
			Min	Max	Min	Typ #	Max	Min	Max	
Output Voltage V _{in} = V _{DD} or 0	V _{OL}	5.0	—	0.05	—	0	0.05	—	0.05	V _d c
		10	—	0.05	—	0	0.05	—	0.05	
		15	—	0.05	—	0	0.05	—	0.05	
V _{in} = 0 or V _{DD}	V _{OH}	5.0	4.95	—	4.95	5.0	—	4.95	—	V _d c
		10	9.95	—	9.95	10	—	9.95	—	
		15	14.95	—	14.95	15	—	14.95	—	
Input Voltage (V _O = 4.5 or 0.5 V _d c) (V _O = 9.0 or 1.0 V _d c) (V _O = 13.5 or 1.5 V _d c)	V _{IL}	5.0	—	1.5	—	2.25	1.5	—	1.5	V _d c
		10	—	3.0	—	4.50	3.0	—	3.0	
		15	—	4.0	—	6.75	4.0	—	4.0	
(V _O = 0.5 or 4.5 V _d c) (V _O = 1.0 or 9.0 V _d c) (V _O = 1.5 or 13.5 V _d c)	V _{IH}	5.0	3.5	—	3.5	2.75	—	3.5	—	V _d c
		10	7.0	—	7.0	5.50	—	7.0	—	
		15	11	—	11	8.25	—	11	—	
Output Drive Current (V _{OH} = 2.5 V _d c) (V _{OH} = 4.6 V _d c) (V _{OH} = 9.5 V _d c) (V _{OH} = 13.5 V _d c)	Source I _{OH}	5.0	-3.0	—	-2.4	-4.2	—	-1.7	—	mAdc
		5.0	-0.64	—	-0.51	-0.88	—	-0.36	—	
		10	-1.6	—	-1.3	-2.25	—	-0.9	—	
	Sink I _{OL}	5.0	0.64	—	0.51	0.88	—	0.36	—	mAdc
		10	1.6	—	1.3	2.25	—	0.9	—	
		15	4.2	—	3.4	8.8	—	2.4	—	
Input Current	I _{in}	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	μAdc
Input Capacitance (V _{in} = 0)	C _{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)	I _{DD}	5.0	—	5.0	—	0.005	5.0	—	150	μAdc
		10	—	10	—	0.010	10	—	300	
		15	—	20	—	0.015	20	—	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C _L = 50 pF on all outputs, all buffers switching)	I _T	5.0	I _T = (0.58 μA/kHz) f + I _{DD}						μAdc	
		10	I _T = (1.20 μA/kHz) f + I _{DD}							
		15	I _T = (1.70 μA/kHz) f + I _{DD}							

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

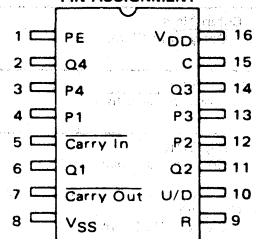
**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) V f k$$

where: I_T is in μA (per package), C_L in pF, V = (V_{DD} - V_{SS}) in volts, f in kHz is input frequency, and k = 0.001.

PIN ASSIGNMENT



MC14510B

SWITCHING CHARACTERISTICS* ($C_L = 50$ pF, $T_A = 25^\circ\text{C}$, See Figure 2)

Characteristic	Symbol	V_{DD}	All Types			Unit
			Min	Typ #	Max	
Output Rise and Fall Time $t_{TLH}, t_{THL} = (1.5 \text{ ns/pF}) C_L + 25 \text{ ns}$ $t_{TLH}, t_{THL} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$ $t_{TLH}, t_{THL} = (0.55 \text{ ns/pF}) C_L + 9.5 \text{ ns}$	t_{TLH}, t_{THL}	5.0 10 15	— — —	100 50 40	200 100 80	ns
Propagation Delay Time Clock to Q $t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 230 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 97 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 75 \text{ ns}$ Clock to Carry Out $t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 230 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 97 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 75 \text{ ns}$ Carry In to Carry Out $t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 230 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 47 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 35 \text{ ns}$ Preset or Reset to Q $t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 230 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 97 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 75 \text{ ns}$ Preset or Reset to Carry Out $t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 465 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 192 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 125 \text{ ns}$	t_{PLH}, t_{PHL}	5.0 10 15	— — —	315 130 100	630 260 200	ns
Reset Pulse Width	$t_w(H)$	5.0 10 15	360 210 160	180 105 80	— — —	ns
Clock Pulse Width	$t_w(H)$	5.0 10 15	350 170 140	200 100 75	— — —	ns
Clock Pulse Frequency	f_{cl}	5.0 10 15	— — —	3.0 6.0 8.0	1.5 3.0 4.0	MHz
Preset or Reset Removal Time The Preset or Reset Signal must be low prior to a positive-going transition of the clock.	t_{rem}	5.0 10 15	650 230 180	325 115 90	— — —	ns
Clock Rise and Fall Time	t_{TLH}, t_{THL}	5.0 10 15	— — —	— — —	15 5 4	μs
Setup Time Carry In to Clock	t_{su}	5.0 10 15	260 120 100	130 60 50	— — —	ns
Hold Time Clock to Carry In	t_h	5.0 10 15	0 10 10	-50 -15 -5	— — —	ns
Setup Time Up/Down to Clock	t_{su}	5.0 10 15	500 200 175	250 100 75	— — —	ns
Hold Time Clock to Up/Down	t_h	5.0 10 15	-70 -30 -20	-140 -80 -50	— — —	ns
Setup Time Pn to PE	t_{su}	5.0 10 15	-50 -30 -25	-100 -65 -55	— — —	ns
Hold Time PE to Pn	t_h	5.0 10 15	480 410 410	240 205 205	— — —	ns
Preset Enable Pulse Width	t_{WH}	5.0 10 15	200 100 80	100 50 40	— — —	ns

*The formulas given are for the typical characteristics only at 25°C .

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

MC14510B

FIGURE 1 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

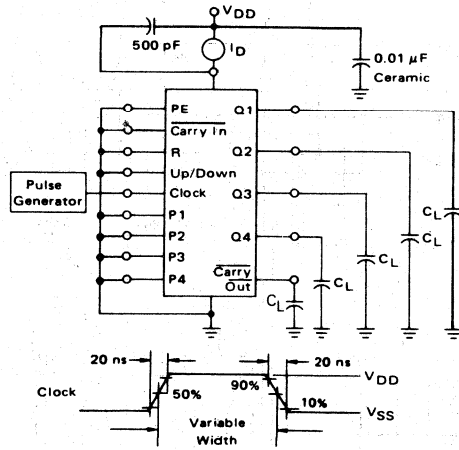
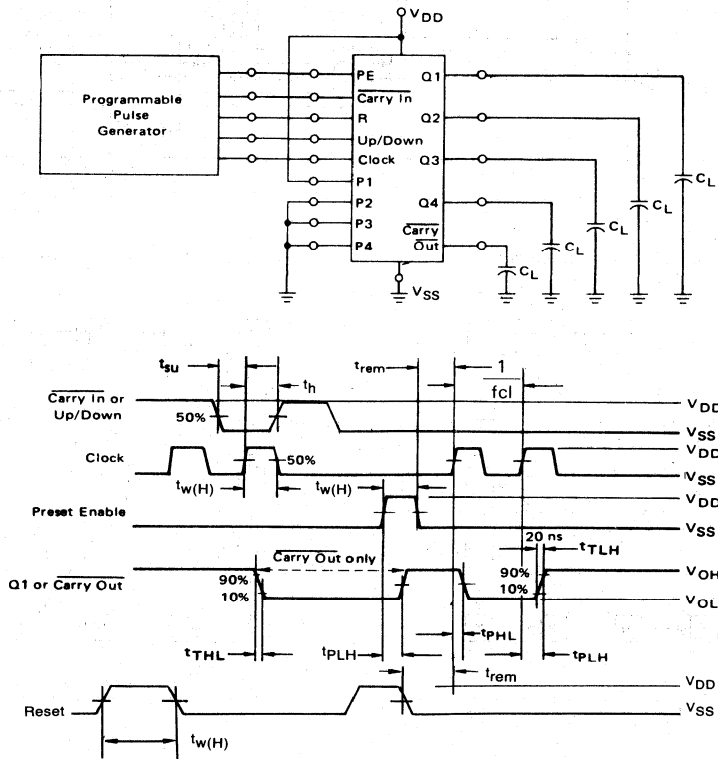
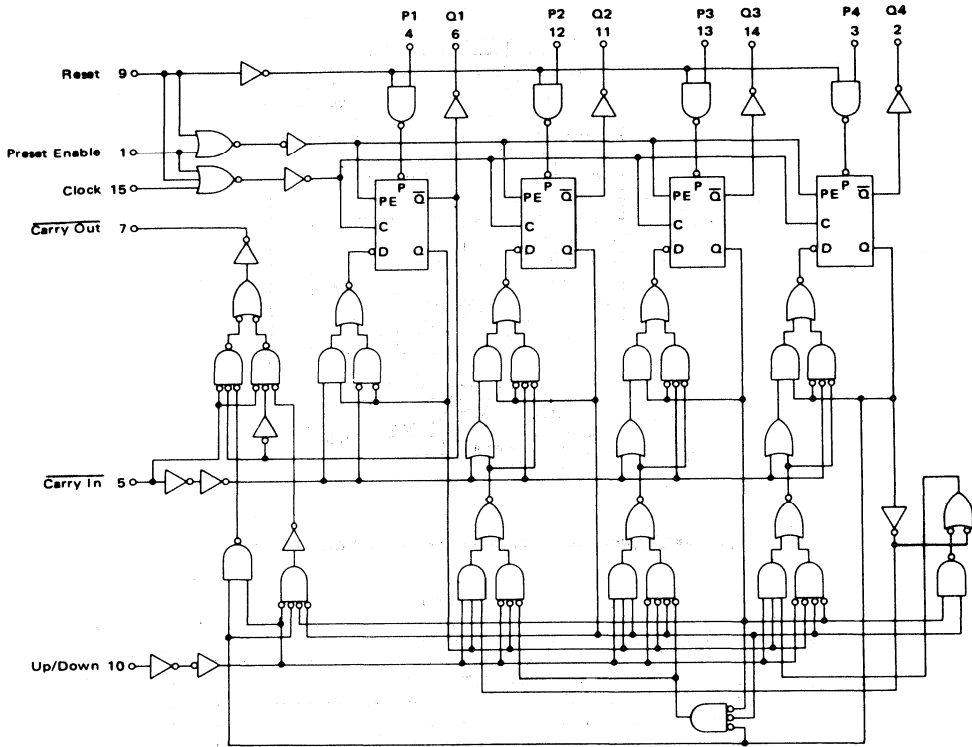


FIGURE 2 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



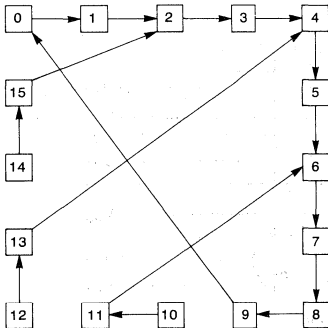
MC14510B

LOGIC DIAGRAM

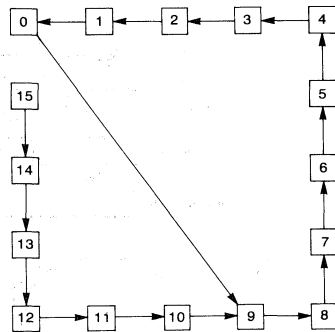


6

STATE DIAGRAM FOR UP COUNTING



STATE DIAGRAM FOR DOWN COUNTING



MC14510B

PIN DESCRIPTIONS

INPUTS

P1, P2, P3, P4, Preset Inputs (Pins 4, 12, 13, 3) — Data on these inputs is loaded into the counter when PE is taken high.

Carry In, (Pin 5) — Active-low input used when cascading stages. Usually connected to Carry Out of the previous stage. While high, clock is inhibited.

Clock, (Pin 15) — BCD data is incremented or decremented, depending on the direction of count, on the positive transition of this signal.

OUTPUTS

Q1, Q2, Q3, Q4, BCD outputs (Pins 6, 11, 14, 2) — BCD data is present on these outputs with Q1 corresponding to the least significant bit.

Carry Out, (Pin 7) — Used when cascading stages, this pin is usually connected to Carry In of the next stage. This synchronous output is active low and may also be used to indicate terminal count.

CONTROLS

PE, Preset Enable (Pin 1) — Asynchronously loads data on the Preset Inputs. This pin is active high and will inhibit the clock when high.

R, Reset, (Pin 9) — Asynchronously resets the Q outputs to a low state. This pin is active high and will inhibit the clock when high.

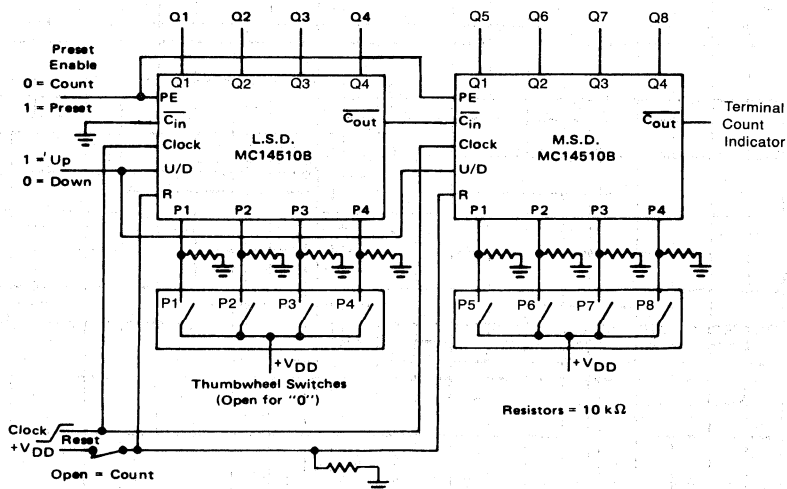
Up/Down, (Pin 10) — Controls the direction of count: high for up count, low for down count.

SUPPLY PINS

VSS, Negative Supply Voltage, (Pin 8) — This pin is usually connected to ground.

VDD, Positive Supply Voltage, (Pin 16) — This pin is connected to a positive supply voltage ranging from 3.0 Vdc to 18.0 Vdc.

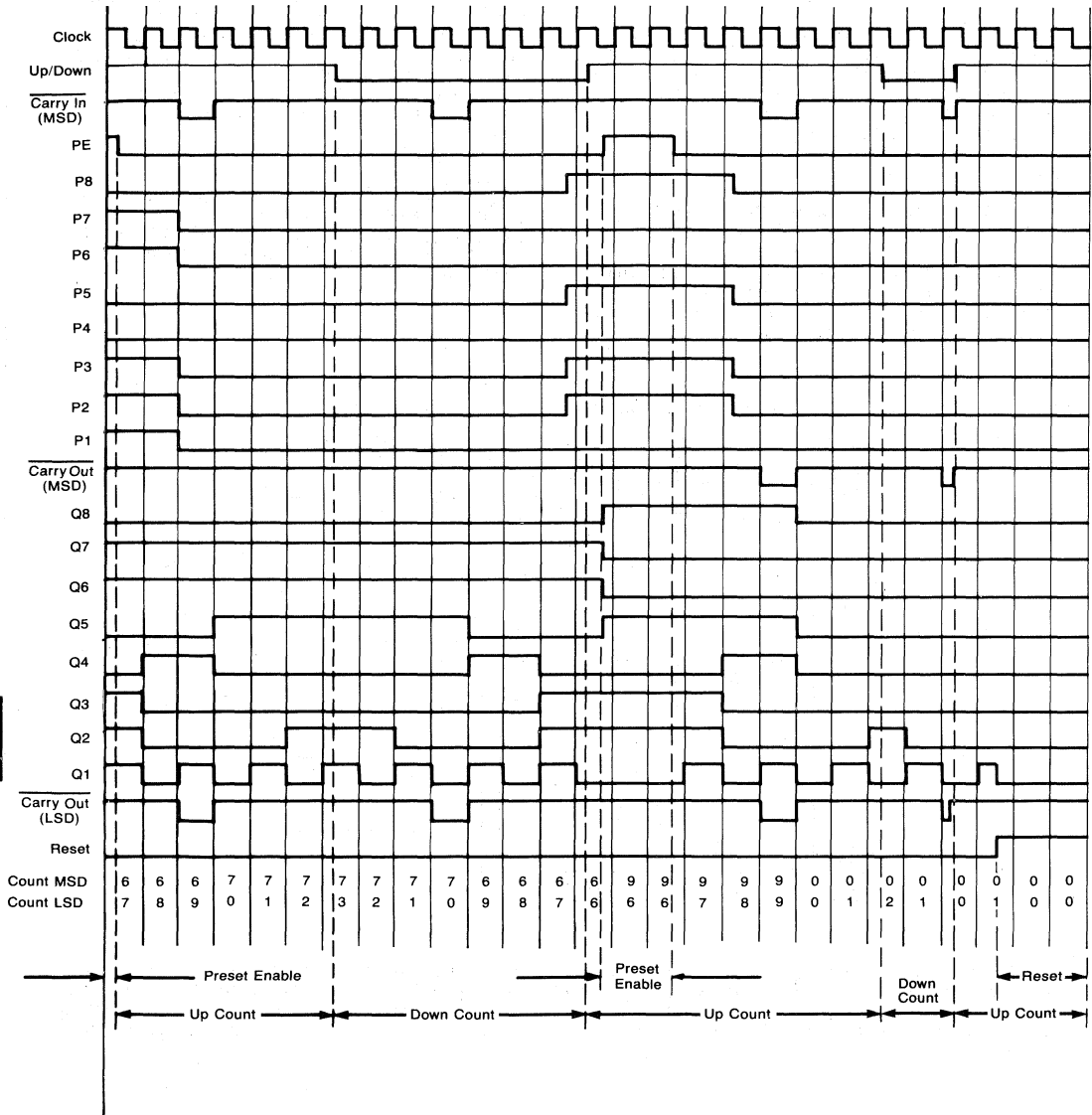
FIGURE 3 — PRESETTABLE CASCADED 8-BIT UP/DOWN COUNTER



Note: The Least Significant Digit (L.S.D.) counts from a preset value once Preset Enable (PE) goes low. The Most Significant Digit (M.S.D.) does not change while $\overline{C_{in}}$ is high. When the count of the L.S.D. reaches 0 (count down mode) or reaches 9 (count up mode), $\overline{C_{out}}$ goes low for one complete clock cycle, thus allowing the next counter to decrement/increment one count. The L.S.D. now counts through another cycle (10 clock pulses) and the above cycle is repeated.

MC14510B

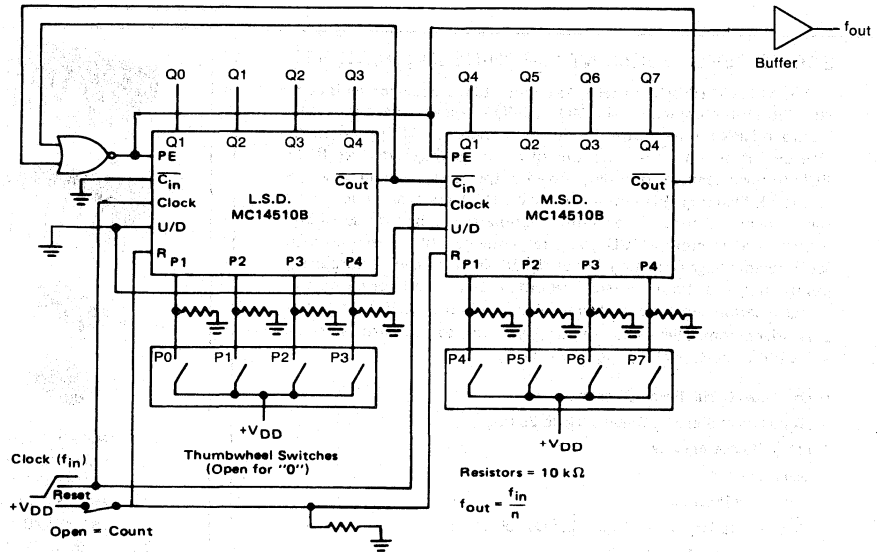
TIMING DIAGRAM FOR THE PRESETTABLE CASCADED 8-BIT UP/DOWN COUNTER



6

MC14510B

FIGURE 4 — PROGRAMMABLE CASCADED FREQUENCY DIVIDER



Note: The programmable frequency divider can be set by applying the desired divide ratio, in BCD, to the preset inputs. For example, the maximum divide ratio of 99 may be obtained by applying a 10011001 to the preset inputs P0 to P7. For this divide operation, both counters should be configured in the count down mode. The divide ratio of zero is an undefined state and should be avoided.



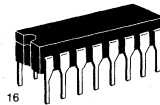
MC14511B

BCD-TO-SEVEN SEGMENT LATCH/DECODER/DRIVER

The MC14511B BCD-to-seven segment latch/decoder/driver is constructed with complementary MOS (CMOS) enhancement mode devices and NPN bipolar output drivers in a single monolithic structure. The circuit provides the functions of a 4-bit storage latch, an 8421 BCD-to-seven segment decoder, and an output drive capability. Lamp test (LT), blanking (BI), and latch enable (LE) inputs are used to test the display, to turn-off or pulse modulate the brightness of the display, and to store a BCD code, respectively. It can be used with seven-segment light emitting diodes (LED), incandescent, fluorescent, gas discharge, or liquid crystal readouts either directly or indirectly.

Applications include instrument (e.g., counter, DVM, etc.) display driver, computer/calculator display driver, cockpit display driver, and various clock, watch, and timer uses.

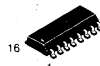
- Low Logic Circuit Power Dissipation
- High-Current Sourcing Outputs (Up to 25 mA)
- Latch Storage of Code
- Blanking Input
- Lamp Test Provision
- Readout Blanking on all Illegal Input Combinations
- Lamp Intensity Modulation Capability
- Time Share (Multiplexing) Facility
- Supply Voltage Range = 3.0 V to 18 V
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range
- Chip Complexity: 216 FETs or 54 Equivalent Gates
- Triple Diode Protection on all Inputs



L SUFFIX
CERAMIC
CASE 620



P SUFFIX
PLASTIC
CASE 648



D SUFFIX
SOIC
CASE 751B



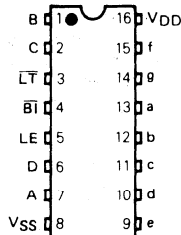
DW SUFFIX
SOIC
CASE 751G

ORDERING INFORMATION

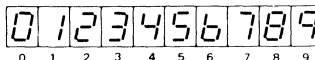
- MC14XXXBCP Plastic
- MC14XXXBCL Ceramic
- MC14XXXBDW SOIC
- MC14XXXBD SOIC

T_A = -55° to 125°C for all packages.

PIN ASSIGNMENT



DISPLAY



TRUTH TABLE

INPUTS				OUTPUTS							
LE	BI	LT	DCBA	a	b	c	d	e	f	g	DISPLAY
X	X	0	X X X X	1	1	1	1	1	1	1	8
X	0	1	X X X X	0	0	0	0	0	0	0	Blank
0	1	1	0 0 0 0	1	1	1	1	1	0	0	0
0	1	1	0 0 0 1	0	1	0	0	0	0	0	1
0	1	1	0 0 1 0	1	1	0	1	0	0	0	2
0	1	1	0 0 1 1	1	1	1	0	0	0	1	3
0	1	1	0 1 0 0	0	1	1	0	0	1	1	4
0	1	1	0 1 0 1	1	0	1	1	0	1	1	5
0	1	1	0 1 1 0	0	0	1	1	1	1	1	6
0	1	1	0 1 1 1	1	1	0	0	0	0	0	7
0	1	1	1 0 0 0	1	1	1	1	1	1	1	8
0	1	1	1 0 0 1	1	1	1	0	0	1	1	9
0	1	1	1 0 1 0	0	0	0	0	0	0	0	Blank
0	1	1	1 0 1 1	0	0	0	0	0	0	0	Blank
0	1	1	1 1 0 0	0	0	0	0	0	0	0	Blank
0	1	1	1 1 0 1	0	0	0	0	0	0	0	Blank
0	1	1	1 1 1 0	0	0	0	0	0	0	0	Blank
0	1	1	1 1 1 1	0	0	0	0	0	0	0	Blank
1	1	1	X X X X	*	*	*	*	*	*	*	*

X = Don't Care

* Depends upon the BCD code previously applied when LE = 0

MAXIMUM RATINGS* (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V _{DD}	-0.5 to +18	V
Input Voltage, All Inputs	V _{in}	-0.5 to V _{DD} + 0.5	V
DC Current Drain per Input Pin	I	10	mA
Operating Temperature Range	T _A	-55 to +125	°C
Power Dissipation per Package†	P _D	500	mW
Storage Temperature Range	T _{stg}	-65 to +150	°C
Maximum Output Drive Current (Source) per Output	I _{OHmax}	25	mA
Maximum Continuous Output Power (Source) per Output ‡	POHmax	50	mW

‡ POHmax = I_{OH} (V_{DD} - V_{OH})

*Maximum Ratings are those values beyond which damage to the device may occur.

†Temperature Derating: Plastic "P and D/DW" Packages: -7.0 mW/°C From 65°C To 125°C
Ceramic "L" Packages: -12 mW/°C From 100°C To 125°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. A destructive high current mode may occur if V_{in} and V_{out} are not constrained to the range V_{SS} ≤ (V_{in} or V_{out}) ≤ V_{DD}.

Due to the sourcing capability of this circuit, damage can occur to the device if V_{DD} is applied, and the outputs are shorted to V_{SS} and are at a logical 1 (See Maximum Ratings).

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

MC14511B

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V _{DD} Vdc	-55°C		25°C			125°C		Unit
			Min	Max	Min	Typ #	Max	Min	Max	
Output Voltage V _{in} = V _{DD} or 0	V _{OL}	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
		10	—	0.05	—	0	0.05	—	0.05	
		15	—	0.05	—	0	0.05	—	0.05	
V _{in} = 0 or V _{DD}	V _{OH}	5.0	4.1	—	4.1	4.57	—	4.1	—	Vdc
		10	9.1	—	9.1	9.58	—	9.1	—	
		15	14.1	—	14.1	14.59	—	14.1	—	
Input Voltage # (V _O = 3.8 or 0.5 Vdc) (V _O = 8.8 or 1.0 Vdc) (V _O = 13.8 or 1.5 Vdc)	"0" Level V _{IL}	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc
		10	—	3.0	—	4.50	3.0	—	3.0	
		15	—	4.0	—	6.75	4.0	—	4.0	
	"1" Level V _{IH}	5.0	3.5	—	3.5	2.75	—	3.5	—	Vdc
		10	7.0	—	7.0	5.50	—	7.0	—	
		15	11	—	11	8.25	—	11	—	
Output Drive Voltage (I _{OH} = 0 mA) (I _{OH} = 5.0 mA) (I _{OH} = 10 mA) (I _{OH} = 15 mA) (I _{OH} = 20 mA) (I _{OH} = 25 mA)	Source V _{OH}	5.0	4.1	—	4.1	4.57	—	4.1	—	Vdc
			—	—	—	4.24	—	—	—	
			3.9	—	3.9	4.12	—	3.5	—	
			—	—	—	3.94	—	—	—	
			3.4	—	3.4	3.70	—	3.0	—	
			—	—	—	3.54	—	—	—	
		10	9.1	—	9.1	9.58	—	9.1	—	Vdc
			—	—	—	9.26	—	—	—	
			9.0	—	9.0	9.17	—	8.6	—	
			—	—	—	9.04	—	—	—	
			8.6	—	8.6	8.90	—	8.2	—	
			—	—	—	8.70	—	—	—	
15	14.1	—	14.1	14.59	—	14.1	—	Vdc		
	—	—	—	14.27	—	—	—			
	14	—	14	14.18	—	13.6	—			
	—	—	—	14.07	—	—	—			
	13.6	—	13.6	13.95	—	13.2	—			
	—	—	—	13.70	—	—	—			
Output Drive Current (V _{OL} = 0.4 V) (V _{OL} = 0.5 V) (V _{OL} = 1.5 V)	Sink I _{OL}	5.0	0.64	—	0.51	0.88	—	0.36	—	mAdc
		10	1.6	—	1.3	2.25	—	0.9	—	
		15	4.2	—	3.4	8.8	—	2.4	—	
Input Current	I _{in}	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	μAdc
Input Capacitance	C _{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package) V _{in} = 0 or V _{DD} . I _{out} = 0 μA	I _{DD}	5.0	—	5.0	—	0.005	5.0	—	150	μAdc
		10	—	10	—	0.010	10	—	300	
		15	—	20	—	0.015	20	—	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C _L = 50 pF on all outputs, all buffers switching)	I _T	5.0	I _T = (1.9 μA/kHz) f + I _{DD}							μAdc
		10	I _T = (3.8 μA/kHz) f + I _{DD}							
		15	I _T = (5.7 μA/kHz) f + I _{DD}							

#Noise immunity specified for worst-case input combination.

Noise Margin for both "1" and "0" level =
 1.0 Vdc min @ V_{DD} = 5.0 Vdc
 2.0 Vdc min @ V_{DD} = 10 Vdc
 2.5 Vdc min @ V_{DD} = 15 Vdc

**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + 3.5 \times 10^{-3} (C_L - 50) V_{DD} f$$

where: I_T is in μA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.

MC14511B

SWITCHING CHARACTERISTICS* ($C_L = 50 \text{ pF}$, $T_A = 25^\circ\text{C}$)

Characteristic	Symbol	VDD Vdc	Min	Typ	Max	Unit
Output Rise Time $t_{TLH} = (0.40 \text{ ns/pF}) C_L + 20 \text{ ns}$ $t_{TLH} = (0.25 \text{ ns/pF}) C_L + 17.5 \text{ ns}$ $t_{TLH} = (0.20 \text{ ns/pF}) C_L + 15 \text{ ns}$	t_{TLH}	5.0 10 15	— — —	40 30 25	80 60 50	ns
Output Fall Time $t_{THL} = (1.5 \text{ ns/pF}) C_L + 50 \text{ ns}$ $t_{THL} = (0.75 \text{ ns/pF}) C_L + 37.5 \text{ ns}$ $t_{THL} = (0.55 \text{ ns/pF}) C_L + 37.5 \text{ ns}$	t_{THL}	5.0 10 15	— — —	125 75 65	250 150 130	ns
Data Propagation Delay Time $t_{PLH} = (0.40 \text{ ns/pF}) C_L + 620 \text{ ns}$ $t_{PLH} = (0.25 \text{ ns/pF}) C_L + 237.5 \text{ ns}$ $t_{PLH} = (0.20 \text{ ns/pF}) C_L + 165 \text{ ns}$ $t_{PHL} = (1.3 \text{ ns/pF}) C_L + 655 \text{ ns}$ $t_{PHL} = (0.60 \text{ ns/pF}) C_L + 260 \text{ ns}$ $t_{PHL} = (0.35 \text{ ns/pF}) C_L + 182.5 \text{ ns}$	t_{PLH} t_{PHL}	5.0 10 15 5.0 10 15	— — — — — — —	640 250 175 720 290 200	1280 500 350 1440 580 400	ns
Blank Propagation Delay Time $t_{PLH} = (0.30 \text{ ns/pF}) C_L + 585 \text{ ns}$ $t_{PLH} = (0.25 \text{ ns/pF}) C_L + 187.5 \text{ ns}$ $t_{PLH} = (0.15 \text{ ns/pF}) C_L + 142.5 \text{ ns}$ $t_{PHL} = (0.85 \text{ ns/pF}) C_L + 442.5 \text{ ns}$ $t_{PHL} = (0.45 \text{ ns/pF}) C_L + 177.5 \text{ ns}$ $t_{PHL} = (0.35 \text{ ns/pF}) C_L + 142.5 \text{ ns}$	t_{PLH} t_{PHL}	5.0 10 15 5.0 10 15	— — — — — — —	600 200 150 485 200 160	750 300 220 970 400 320	ns
Lamp Test Propagation Delay Time $t_{PLH} = (0.45 \text{ ns/pF}) C_L + 290.5 \text{ ns}$ $t_{PLH} = (0.25 \text{ ns/pF}) C_L + 112.5 \text{ ns}$ $t_{PLH} = (0.20 \text{ ns/pF}) C_L + 80 \text{ ns}$ $t_{PHL} = (1.3 \text{ ns/pF}) C_L + 248 \text{ ns}$ $t_{PHL} = (0.45 \text{ ns/pF}) C_L + 102.5 \text{ ns}$ $t_{PHL} = (0.35 \text{ ns/pF}) C_L + 72.5 \text{ ns}$	t_{PLH} t_{PHL}	5.0 10 15 5.0 10 15	— — — — — — —	313 125 90 313 125 90	625 250 180 625 250 180	ns
Setup Time	t_{su}	5.0 10 15	100 40 30	— — —	— — —	ns
Hold Time	t_h	5.0 10 15	60 40 30	— — —	— — —	ns
Latch Enable Pulse Width	t_{WL}	5.0 10 15	520 220 130	260 110 65	— — —	ns

*The formulas given are for the typical characteristics only.

MC14511B

FIGURE 1 – DYNAMIC POWER DISSIPATION SIGNAL WAVEFORMS

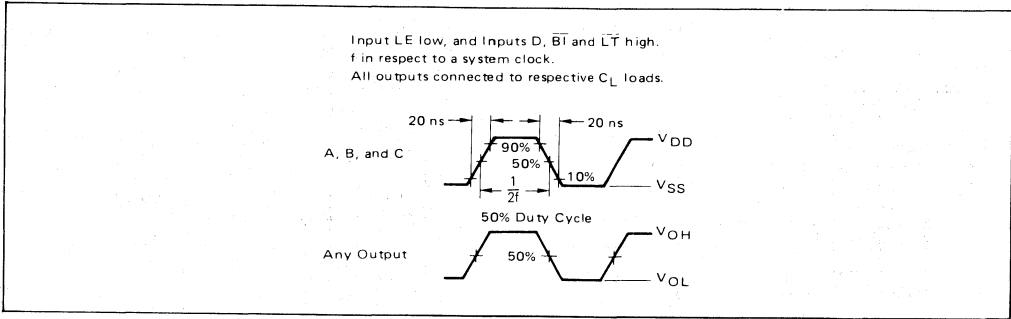
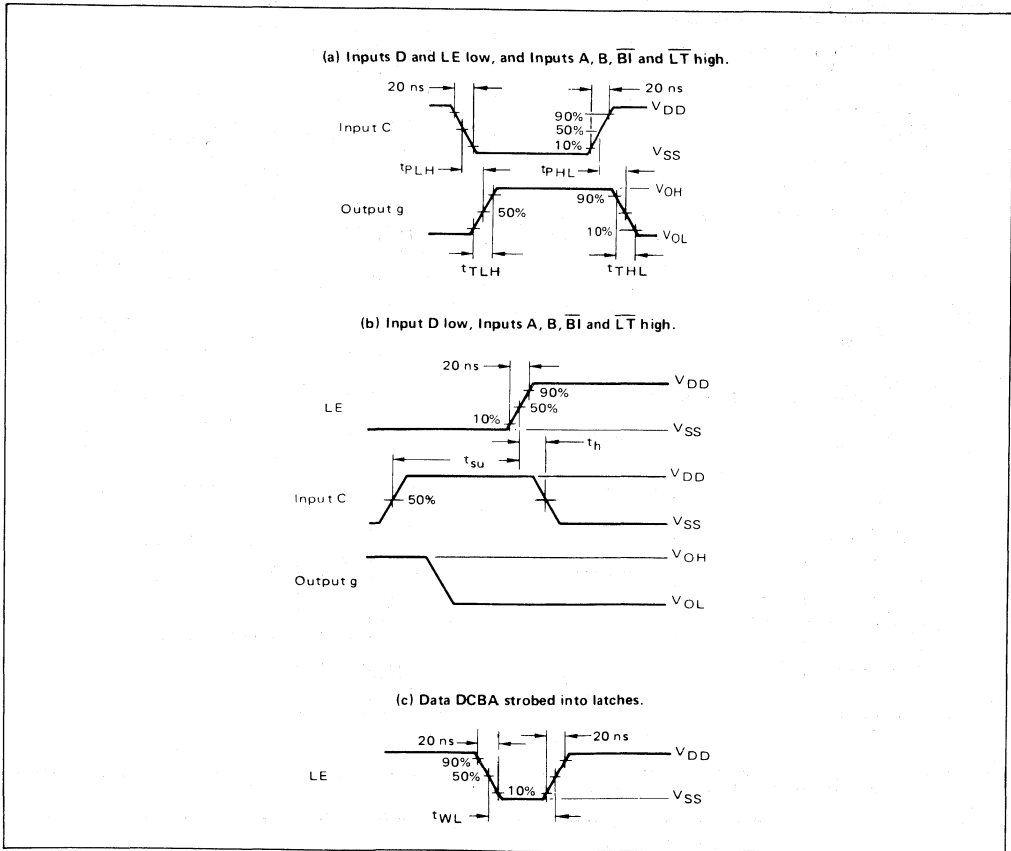
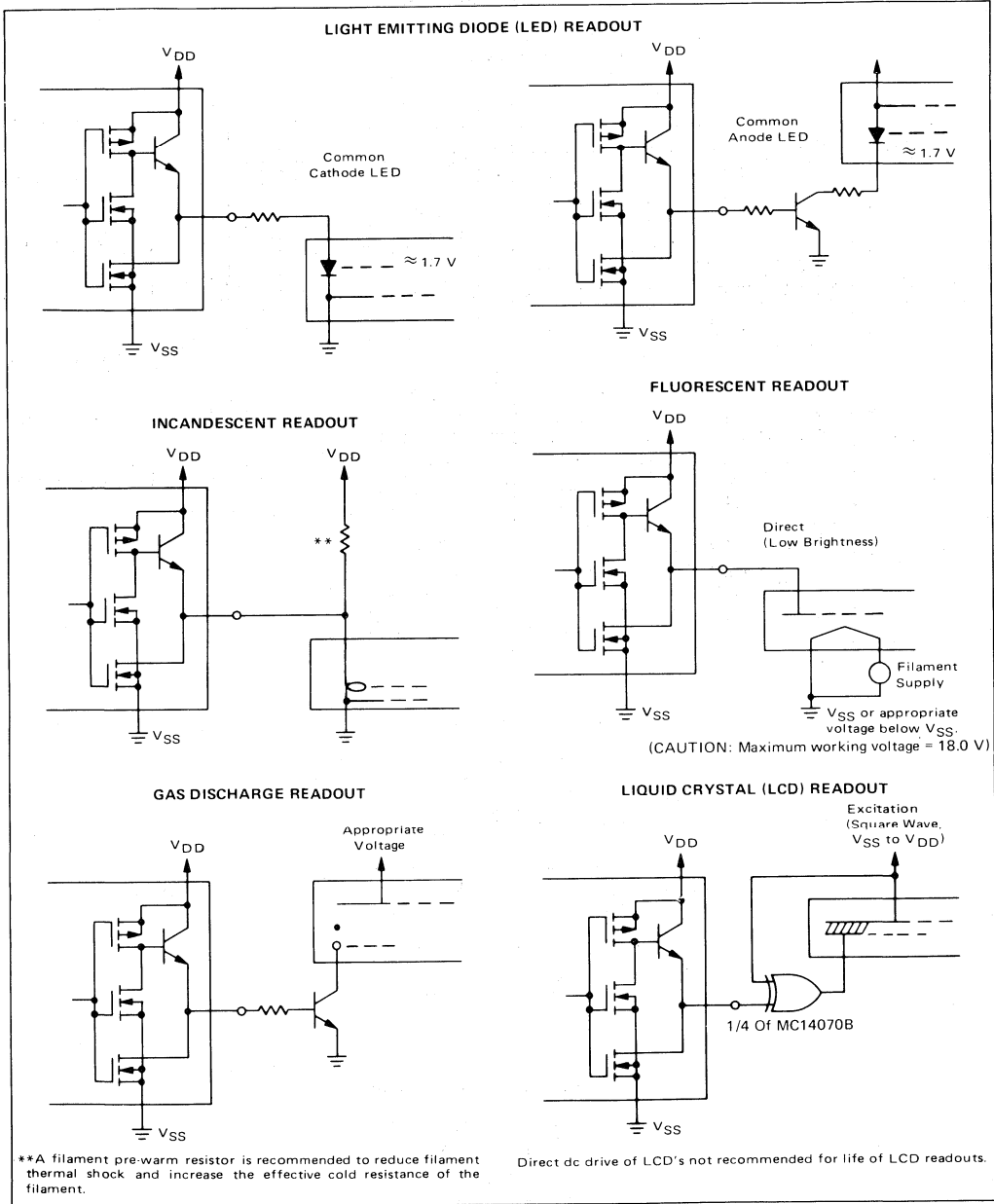


FIGURE 2 – DYNAMIC SIGNAL WAVEFORMS



MC14511B

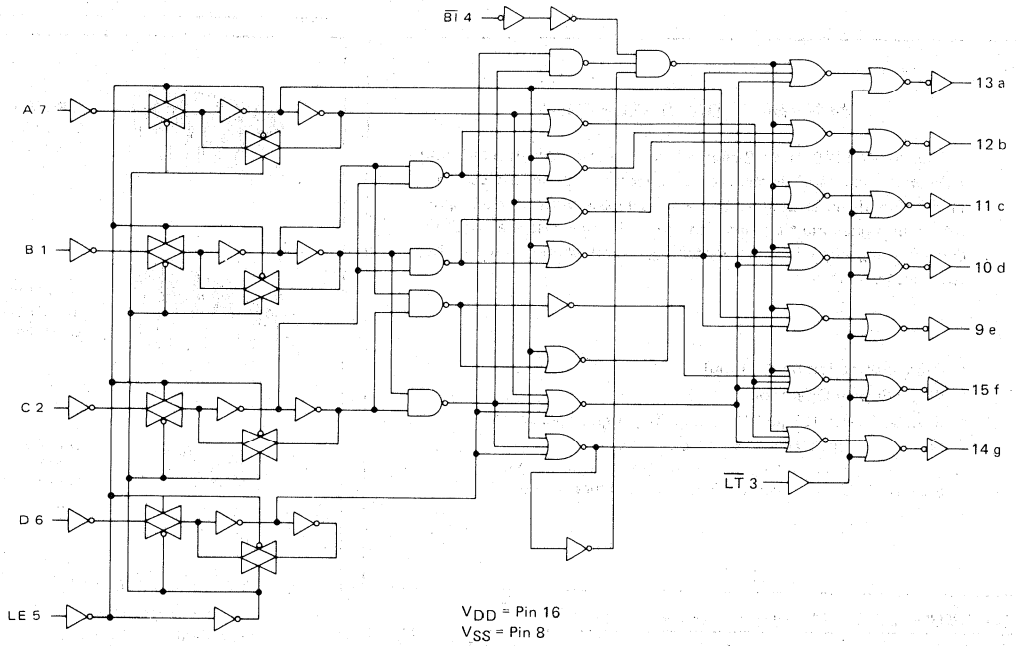
CONNECTIONS TO VARIOUS DISPLAY READOUTS



6

MC14511B

LOGIC DIAGRAM





MOTOROLA

MC14512B

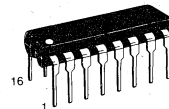
8-CHANNEL DATA SELECTOR

The MC14512B is an 8-channel data selector constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. This data selector finds primary application in signal multiplexing functions. It may also be used for data routing, digital signal switching, signal gating, and number sequence generation.

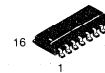
- Diode Protection on All Inputs
- Single Supply Operation
- 3-State Output (Logic "1", Logic "0", High Impedance)
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range



L SUFFIX
CERAMIC
CASE 620



P SUFFIX
PLASTIC
CASE 648



D SUFFIX
SOIC
CASE 751B

ORDERING INFORMATION

MC14512BCP Plastic
MC14512BCL Ceramic
MC14512BD SOIC

T_A = -55° to 125°C for all packages.

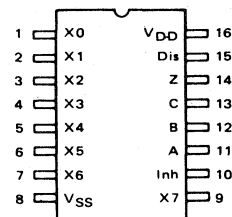
MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V _{DD}	DC Supply Voltage	-0.5 to +18.0	V
V _{in} , V _{out}	Input or Output Voltage (DC or Transient)	-0.5 to V _{DD} + 0.5	V
I _{in} , I _{out}	Input or Output Current (DC or Transient), per Pin	± 10	mA
P _D	Power Dissipation, per Package†	500	mW
T _{stg}	Storage Temperature	-65 to +150	°C
T _L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.

†Temperature Derating: Plastic "P and D/DW" Packages: -7.0 mW/°C From 65°C To 125°C
Ceramic "L" Packages: -12 mW/°C From 100°C To 125°C

PIN ASSIGNMENT



TRUTH TABLE

C	B	A	INHIBIT	DISABLE	Z
0	0	0	0	0	X0
0	0	1	0	0	X1
0	1	0	0	0	X2
0	1	1	0	0	X3
1	0	0	0	0	X4
1	0	1	0	0	X5
1	1	0	0	0	X6
1	1	1	0	0	X7
X	X	X	1	0	0
X	X	X	X	1	High Impedance

X = Don't Care

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range V_{SS} ≤ (V_{in} or V_{out}) ≤ V_{DD}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

MC14512B

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V _{DD} Vdc	-55°C		25°C			125°C		Unit
			Min	Max	Min	Typ #	Max	Min	Max	
Output Voltage V _{in} = V _{DD} or 0 "0" Level	V _{OL}	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
		10	—	0.05	—	0	0.05	—	0.05	
V _{in} = 0 or V _{DD} "1" Level	V _{OH}	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc
		10	9.95	—	9.95	10	—	9.95	—	
Input Voltage (V _O = 4.5 or 0.5 Vdc) (V _O = 9.0 or 1.0 Vdc) (V _O = 13.5 or 1.5 Vdc) "0" Level	V _{IL}	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc
		10	—	3.0	—	4.50	3.0	—	3.0	
(V _O = 0.5 or 4.5 Vdc) (V _O = 1.0 or 9.0 Vdc) (V _O = 1.5 or 13.5 Vdc) "1" Level	V _{IH}	5.0	3.5	—	3.5	2.75	—	3.5	—	Vdc
		10	7.0	—	7.0	5.50	—	7.0	—	
Output Drive Current (V _{OH} = 2.5 Vdc) (V _{OH} = 4.6 Vdc) (V _{OH} = 9.5 Vdc) (V _{OH} = 13.5 Vdc) Source	I _{OH}	5.0	-3.0	—	-2.4	-4.2	—	-1.7	—	mA _{dc}
		5.0	-0.64	—	-0.51	-0.88	—	-0.36	—	
(V _{OL} = 0.4 Vdc) (V _{OL} = 0.5 Vdc) (V _{OL} = 1.5 Vdc) Sink	I _{OL}	10	-1.6	—	-1.3	-2.25	—	-0.9	—	mA _{dc}
		15	-4.2	—	-3.4	-8.8	—	-2.4	—	
Input Current	I _{in}	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	μA _{dc}
Input Capacitance (V _{in} = 0)	C _{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)	I _{DD}	5.0	—	5.0	—	0.005	5.0	—	150	μA _{dc}
		10	—	10	—	0.010	10	—	300	
		15	—	20	—	0.015	20	—	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C _L = 50 pF on all outputs, all buffers switching)	I _T	5.0	I _T = (0.8 μA/kHz) f + I _{DD}							μA _{dc}
		10	I _T = (1.6 μA/kHz) f + I _{DD}							
		15	I _T = (2.4 μA/kHz) f + I _{DD}							
Three-State Leakage Current	I _{TL}	15	—	±0.1	—	±0.00001	±0.1	—	±3.0	μA _{dc}

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) Vfk$$

where: I_T is in μA (per package), C_L in pF, V = (V_{DD} - V_{SS}) in volts, f in kHz is input frequency, and k = 0.001.

MC14512B

SWITCHING CHARACTERISTICS (C_L = 50 pF, T_A = 25°C, See Figure 1)

Characteristic	Symbol	V _{DD}	All Types		Unit
			Typ #	Max	
Output Rise and Fall Time t _{TLH} , t _{THL} = (1.5 ns/pF) C _L + 25 ns t _{TLH} , t _{THL} = (0.75 ns/pF) C _L + 12.5 ns t _{TLH} , t _{THL} = (0.55 ns/pF) C _L + 9.5 ns	t _{TLH} , t _{THL}	5.0 10 15	100 50 40	200 100 80	ns
Propagation Delay Time (Figure 2) Inhibit, Control, or Data to Z	t _{PLH}	5.0 10 15	330 125 85	650 250 170	ns
Propagation Delay Time (Figure 2) Inhibit, Control, or Data to Z	t _{PHL}	5.0 10 15	330 125 85	650 250 170	ns
3-State Output Delay Times (Figure 3) "1" or "0" to High Z, and High Z to "1" or "0"	t _{PHZ} , t _{PLZ} , t _{PZH} , t _{PZL}	5.0 10 15	60 35 30	150 100 75	ns

*The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

FIGURE 1 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

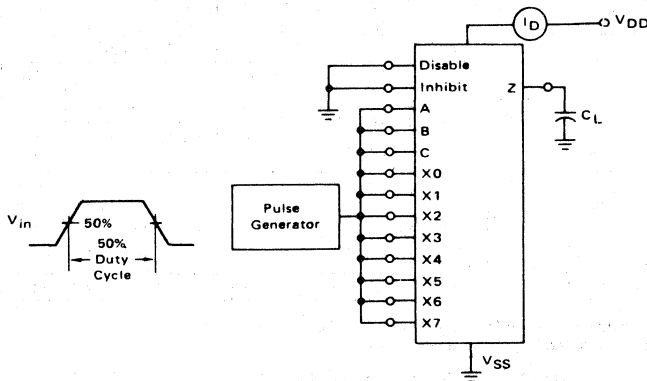
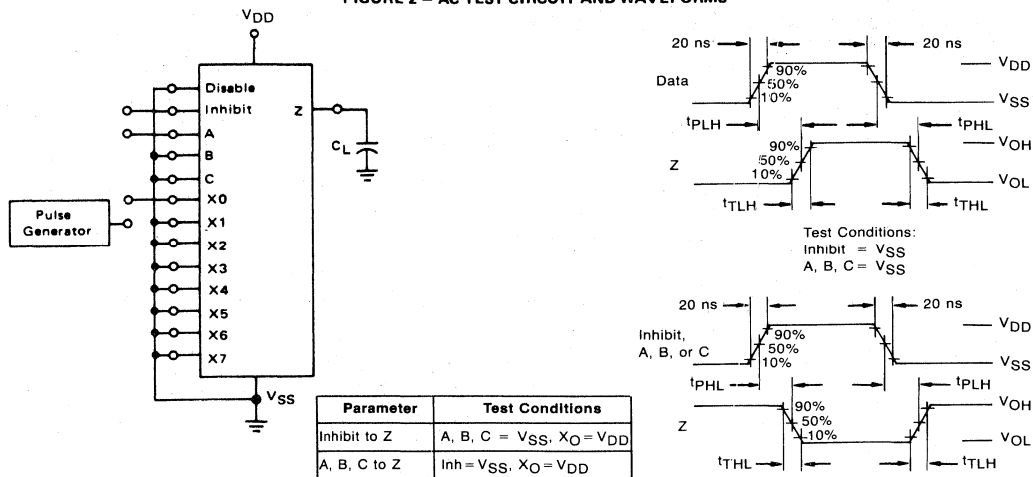
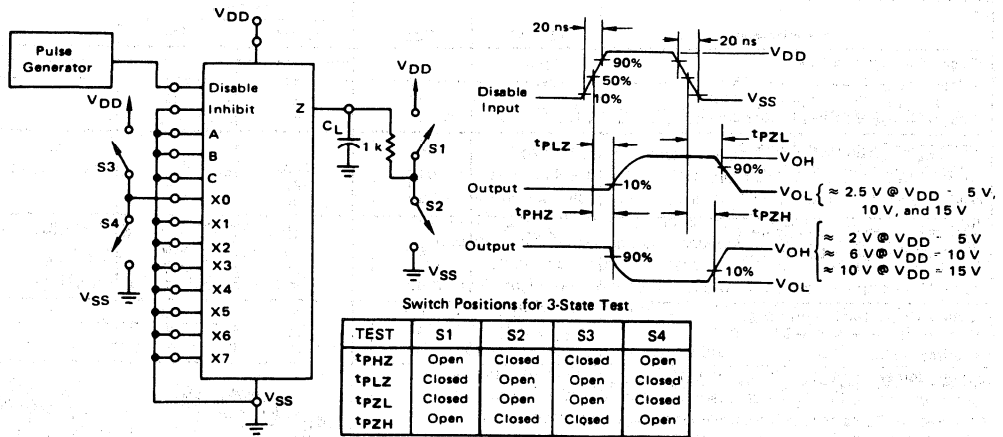


FIGURE 2 – AC TEST CIRCUIT AND WAVEFORMS

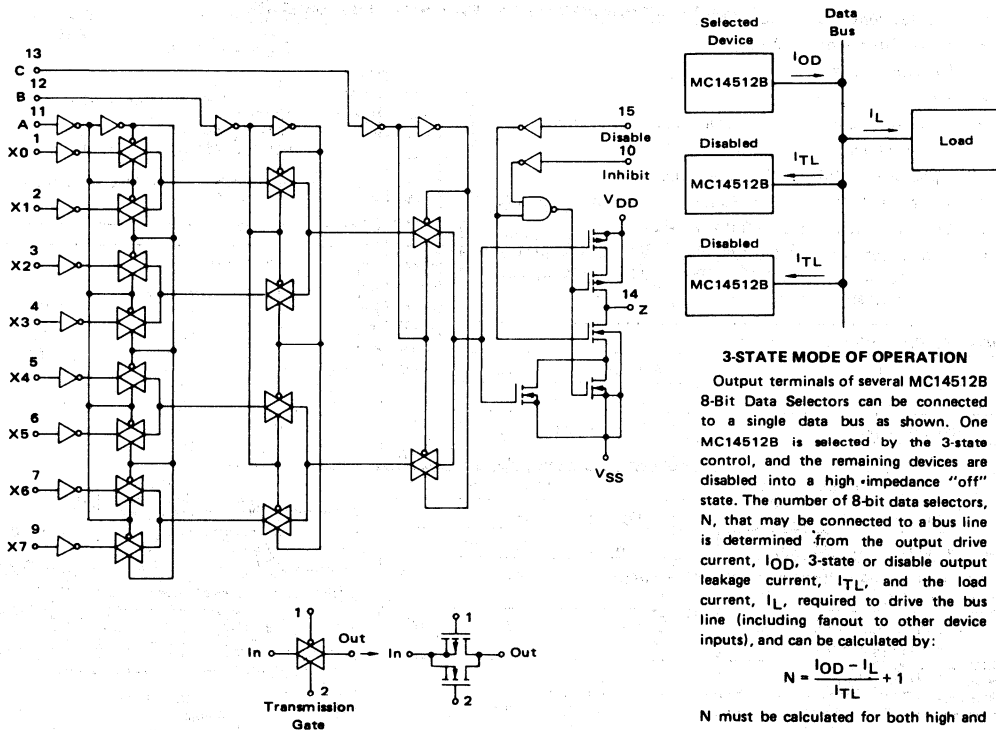


MC14512B

FIGURE 3 - 3-STATE AC TEST CIRCUIT AND WAVEFORM



LOGIC DIAGRAM





MOTOROLA

MC14513B

BCD-TO-SEVEN SEGMENT LATCH/DECODER/DRIVER

The MC14513B BCD-to-seven segment latch/decoder/driver is constructed with complementary MOS (CMOS) enhancement mode devices and NPN bipolar output drivers in a single monolithic structure. The circuit provides the functions of a 4-bit storage latch, an 8421 BCD-to-seven segment decoder, and has output drive capability. Lamp test (LT), blanking (BI), and latch enable (LE) inputs are used to test the display, to turn-off or pulse modulate the brightness of the display, and to store a BCD code, respectively. The Ripple Blanking Input (RBI) and Ripple Blanking Output (RBO) can be used to suppress either leading or trailing zeroes. It can be used with seven-segment light emitting diodes (LED), incandescent, fluorescent, gas discharge, or liquid crystal readouts either directly or indirectly.

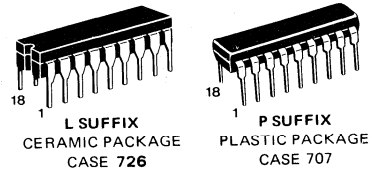
Applications include instrument (e.g., counter, DVM, etc.) display driver, computer/calculator display driver, cockpit display driver, and various clock, watch, and timer uses.

- Low Logic Circuit Power Dissipation
- High-current Sourcing Outputs (Up to 25 mA)
- Latch Storage of Binary Input
- Blanking Input
- Lamp Test Provision
- Readout Blanking on all Illegal Input Combinations
- Lamp Intensity Modulation Capability
- Time Share (Multiplexing) Capability
- Adds Ripple Blanking In, Ripple Blanking Out to MC14511B
- Supply Voltage Range = 3.0 V to 18 V
- Capable of Driving Two Low-Power TTL Loads, One Low-power Schottky TTL Load to Two HTL Loads Over the Rated Temperature Range.

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

BCD-TO-SEVEN SEGMENT LATCH/DECODER/DRIVER WITH RIPPLE BLANKING



ORDERING INFORMATION

MC14XXXBCP (Plastic Package)
MC14XXXBCL (Ceramic Package)

T_A = -55°C to +125°C for all packages

6

MAXIMUM RATINGS* (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V _{DD}	-0.5 to +18	V
Input Voltage, All Inputs	V _{in}	-0.5 to V _{DD} + 0.5	V
DC Current Drain per Input Pin	I	10	mA
Operating Temperature Range	T _A	-55 to +125	°C
Power Dissipation, per Package†	P _D	500	mW
Storage Temperature Range	T _{stg}	-65 to +150	°C
Maximum Continuous Output Drive Current (Source) per Output	I _{OHmax}	25	mA
Maximum Continuous Output Power (Source) per Output‡	P _{OHmax}	50	mW

‡ P_{OHmax} = I_{OH}(V_{DD} - V_{OH})

*Maximum Ratings are those values beyond which damage to the device may occur.

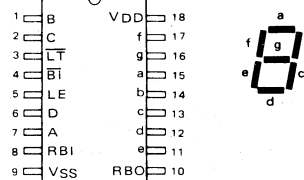
† Temperature Derating: Plastic "P" and "D/DW" Packages: 7.0 mW/°C From 65°C To 125°C
Ceramic "L" Packages: -12 mW/°C From 100°C To 125°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. A destructive high current mode may occur if V_{in} and V_{out} is not constrained to the range V_{SS} ≤ (V_{in} or V_{out}) ≤ V_{DD}.

Due to the sourcing capability of this circuit, damage can occur to the device if V_{DD} is applied, and the outputs are shorted to V_{SS} and are at a logical 1 (see Maximum Ratings).

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

PIN ASSIGNMENT



TRUTH TABLE

INPUTS				OUTPUTS												
RBI	LE	BI	LT	D	C	B	A	RBO	a	b	c	d	e	f	g	DISPLAY
X	X	X	0	X	X	X	X	+	1	1	1	1	1	1	1	8
X	X	0	1	0	0	0	0	+	0	0	0	0	0	0	0	Blank
0	0	1	1	0	0	0	0	0	1	1	1	1	1	0	0	0
X	0	1	1	0	0	0	1	0	0	1	1	0	0	0	0	1
X	0	1	1	0	0	1	1	0	1	1	0	0	0	0	0	2
X	0	1	1	0	1	1	0	0	1	1	1	0	0	0	0	3
X	0	1	1	0	1	0	0	0	0	1	1	0	0	1	1	4
X	0	1	1	0	1	0	1	0	1	0	1	0	1	1	0	5
X	0	1	1	0	1	1	1	0	0	1	0	1	1	1	1	6
X	0	1	1	0	1	1	1	1	1	1	0	0	0	0	0	7
X	0	1	1	1	0	0	0	0	1	1	1	1	0	1	1	8
X	0	1	1	1	0	0	1	0	1	1	1	0	1	1	1	9
X	0	1	1	1	0	1	1	0	0	0	0	0	0	0	0	Blank
X	0	1	1	1	0	1	0	0	0	0	0	0	0	0	0	Blank
X	0	1	1	1	1	0	1	0	0	0	0	0	0	0	0	Blank
X	0	1	1	1	1	1	0	0	0	0	0	0	0	0	0	Blank
X	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0	Blank
X	1	1	1	1	X	X	X	+	*	*	*	*	*	*	*	*

X = Don't Care
+ RBO = RBI if C B A, indicated by other rows of table
* Depends upon the BCD code previously applied when LE = 0

MC14513B

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V _{DD} V _d c	-55°C		25°C			125°C		Unit	
			Min	Max	Min	Typ #	Max	Min	Max		
Output Voltage — Segment Outputs V _{in} = V _{DD} or 0	"0" Level V _{OL}	5.0	—	0.05	—	0	0.05	—	0.05	V _d c	
		10	—	0.05	—	0	0.05	—	0.05		
		15	—	0.05	—	0	0.05	—	0.05		
	"1" Level V _{OH}	5.0	4.1	—	4.1	5.0	—	4.1	—		
		10	9.1	—	9.1	10	—	9.1	—		
		15	14.1	—	14.1	15	—	14.1	—		
Output Voltage — RBO Output V _{in} = V _{DD} or 0	"0" Level V _{OL}	5.0	—	0.05	—	0	0.05	—	0.05	V _d c	
		10	—	0.05	—	0	0.05	—	0.05		
		15	—	0.05	—	0	0.05	—	0.05		
	"1" Level V _{OH}	5.0	4.95	—	4.95	5.0	—	4.95	—		
		10	9.95	—	9.95	10	—	9.95	—		
		15	14.95	—	14.95	15	—	14.95	—		
Input Voltage # "0" Level (V _O = 3.8 or 0.5 V _d c) (V _O = 8.8 or 1.0 V _d c) (V _O = 13.8 or 1.5 V _d c)	V _{IL}	5.0	—	1.5	—	2.25	1.5	—	1.5	V _d c	
		10	—	3.0	—	4.50	3.0	—	3.0		
		15	—	4.0	—	6.75	4.0	—	4.0		
	"1" Level (V _O = 0.5 or 3.8 V _d c) (V _O = 1.0 or 8.8 V _d c) (V _O = 1.5 or 13.8 V _d c)	V _{IH}	5.0	3.5	—	3.5	2.75	—	3.5		—
			10	7.0	—	7.0	5.50	—	7.0		—
			15	11	—	11	8.25	—	11		—
Output Drive Voltage — Segments Source	V _{OH}	5.0	4.1	—	4.1	4.57	—	4.1	—	V _d c	
			(I _{OH} = 0 mA)	—	—	—	4.24	—	—		—
			(I _{OH} = 5.0 mA)	—	—	—	4.12	—	3.5		—
			(I _{OH} = 10 mA)	3.9	—	3.9	—	—	—		—
			(I _{OH} = 15 mA)	—	—	—	3.94	—	—		—
			(I _{OH} = 20 mA)	—	—	—	3.70	—	3.0		—
			(I _{OH} = 25 mA)	3.4	—	3.4	3.70	—	—		—
			(I _{OH} = 0 mA)	—	—	—	3.54	—	—		—
			(I _{OH} = 5.0 mA)	—	—	—	—	—	—		—
		10	9.1	—	9.1	9.58	—	9.1	—	V _d c	
			(I _{OH} = 5.0 mA)	—	—	—	9.26	—	—		—
			(I _{OH} = 10 mA)	—	—	—	9.17	—	8.6		—
			(I _{OH} = 15 mA)	9.0	—	9.0	—	—	—		—
			(I _{OH} = 20 mA)	—	—	—	9.04	—	—		—
			(I _{OH} = 25 mA)	—	—	—	8.90	—	8.2		—
			(I _{OH} = 0 mA)	8.6	—	8.6	8.90	—	—		—
			(I _{OH} = 5.0 mA)	—	—	—	8.75	—	—		—
			(I _{OH} = 10 mA)	—	—	—	—	—	—		—
		15	14.1	—	14.1	14.59	—	14.1	—	V _d c	
			(I _{OH} = 5.0 mA)	—	—	—	14.27	—	—		—
			(I _{OH} = 10 mA)	—	—	—	14.18	—	13.6		—
			(I _{OH} = 15 mA)	14	—	14	—	—	—		—
			(I _{OH} = 20 mA)	—	—	—	14.07	—	—		—
			(I _{OH} = 25 mA)	—	—	—	13.95	—	13.2		—
(I _{OH} = 0 mA)	13.6		—	13.6	13.80	—	—	—			
(I _{OH} = 5.0 mA)	—		—	—	—	—	—	—			
(I _{OH} = 10 mA)	—		—	—	—	—	—	—			

(continued)

MC14513B

ELECTRICAL CHARACTERISTICS — continued (Voltages Referenced to V_{SS})

Characteristic	Symbol	V _{DD} Vdc	-55°C		25°C			125°C		Unit
			Min	Max	Min	Typ #	Max	Min	Max	
Output Drive Current — RBO Output Source (V _{OH} = 2.5 V) (V _{OH} = 9.5 V) (V _{OH} = 13.5 V) (V _{OL} = 0.4 V) (V _{OL} = 0.5 V) (V _{OL} = 1.5 V)	I _{OH}	5.0	-0.40	—	-0.32	-0.64	—	-0.22	—	mAdc
		10	-0.21	—	-0.17	-0.34	—	-0.12	—	
		15	-0.81	—	-0.66	-1.30	—	-0.46	—	
	I _{OL}	5.0	0.18	—	0.15	0.29	—	0.10	—	mAdc
		10	0.47	—	0.38	0.75	—	0.26	—	
		15	1.80	—	1.50	2.90	—	1.0	—	
Output Drive Current — Segments Sink	I _{OL}	5.0	0.64	—	0.51	0.88	—	0.36	—	mAdc
		10	1.6	—	1.3	2.25	—	0.9	—	
		15	4.2	—	3.4	8.8	—	2.4	—	
Input Current	I _{in}	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	μAdc
Input Capacitance	C _{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package) V _{in} = 0 or V _{DD} , I _{out} = 0 μA	I _{DD}	5.0	—	5.0	—	0.005	5.0	—	150	μAdc
		10	—	10	—	0.010	10	—	300	
		15	—	20	—	0.015	20	—	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C _L = 50 pF on all outputs, all buffers switching)	I _T	5.0	I _T = (1.9 μA/kHz) f + I _{DD}							μAdc
		10	I _T = (3.8 μA/kHz) f + I _{DD}							
		15	I _T = (5.7 μA/kHz) f + I _{DD}							

#Noise immunity specified for worst-case input combination.

Noise Margin for both "1" and "0" level =

1.0 Vdc min @ V_{DD} = 5.0 Vdc

2.0 Vdc min @ V_{DD} = 10 Vdc

2.5 Vdc min @ V_{DD} = 15 Vdc

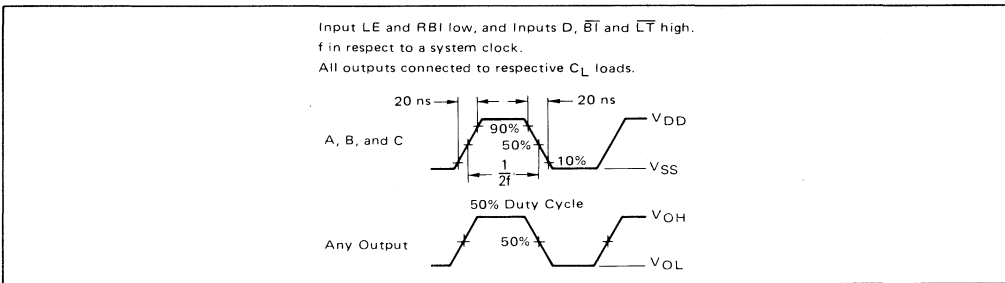
**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + 3.5 \times 10^{-3} (C_L - 50) V_{DD} f$$

where: I_T is in μA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.

FIGURE 1 — DYNAMIC POWER DISSIPATION
SIGNAL WAVEFORMS



MC14513B

SWITCHING CHARACTERISTICS* ($C_L = 50 \text{ pF}$, $T_A = 25^\circ\text{C}$)

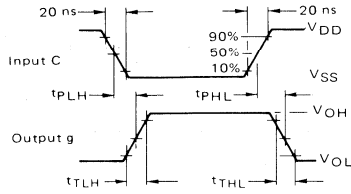
Characteristic	Symbol	VDD Vdc	All Types			Unit
			Min	Typ	Max	
Output Rise Time -- Segment Outputs	t_{TLH}	5.0	--	40	80	ns
		10	--	30	60	
		15	--	25	50	
Output Rise Time -- RBO Output	t_{TLH}	5.0	--	480	960	ns
		10	--	240	480	
		15	--	190	380	
Output Fall Time--Segment Outputs* $t_{THL} = (1.5 \text{ ns/pF}) C_L + 50 \text{ ns}$ $t_{THL} = (0.75 \text{ ns/pF}) C_L + 37.5 \text{ ns}$ $t_{THL} = (0.55 \text{ ns/pF}) C_L + 37.5 \text{ ns}$	t_{THL}	5.0	--	125	250	ns
		10	--	75	150	
		15	--	65	130	
		15	--	65	130	
Output Fall Time -- RBO Outputs $t_{THL} = (3.25 \text{ ns/pF}) C_L + 107.5 \text{ ns}$ $t_{THL} = (1.35 \text{ ns/pF}) C_L + 67.5 \text{ ns}$ $t_{THL} = (0.95 \text{ ns/pF}) C_L + 62.5 \text{ ns}$	t_{THL}	5.0	--	270	540	ns
		10	--	135	270	
		15	--	110	220	
		15	--	110	220	
Propagation Delay Time--A, B, C, D Inputs* $t_{PLH} = (0.40 \text{ ns/pF}) C_L + 620 \text{ ns}$ $t_{PLH} = (0.25 \text{ ns/pF}) C_L + 237.5 \text{ ns}$ $t_{PLH} = (0.20 \text{ ns/pF}) C_L + 165 \text{ ns}$ $t_{PHL} = (1.3 \text{ ns/pF}) C_L + 655 \text{ ns}$ $t_{PHL} = (0.60 \text{ ns/pF}) C_L + 260 \text{ ns}$ $t_{PHL} = (0.35 \text{ ns/pF}) C_L + 182.5 \text{ ns}$	t_{PLH}	5.0	--	640	1280	ns
		10	--	250	500	
		15	--	175	350	
	t_{PHL}	5.0	--	720	1440	ns
		10	--	290	580	
		15	--	200	400	
Propagation Delay Time--RBI and BI Inputs* $t_{PLH} = (1.05 \text{ ns/pF}) C_L + 547.5 \text{ ns}$ $t_{PLH} = (0.45 \text{ ns/pF}) C_L + 177.5 \text{ ns}$ $t_{PLH} = (0.30 \text{ ns/pF}) C_L + 135 \text{ ns}$ $t_{PHL} = (0.85 \text{ ns/pF}) C_L + 442.5 \text{ ns}$ $t_{PHL} = (0.45 \text{ ns/pF}) C_L + 177.5 \text{ ns}$ $t_{PHL} = (0.35 \text{ ns/pF}) C_L + 142.5 \text{ ns}$	t_{PLH}	5.0	--	600	750	ns
		10	--	200	300	
		15	--	150	220	
	t_{PHL}	5.0	--	485	970	ns
		10	--	200	400	
		15	--	160	320	
Propagation Delay Time--LT Input* $t_{PLH} = (0.45 \text{ ns/pF}) C_L + 290.5 \text{ ns}$ $t_{PLH} = (0.25 \text{ ns/pF}) C_L + 112.5 \text{ ns}$ $t_{PLH} = (0.20 \text{ ns/pF}) C_L + 80 \text{ ns}$ $t_{PHL} = (1.3 \text{ ns/pF}) C_L + 248 \text{ ns}$ $t_{PHL} = (0.45 \text{ ns/pF}) C_L + 102.5 \text{ ns}$ $t_{PHL} = (0.35 \text{ ns/pF}) C_L + 72.5 \text{ ns}$	t_{PLH}	5.0	--	313	625	ns
		10	--	125	250	
		15	--	90	180	
	t_{PHL}	5.0	--	313	625	ns
		10	--	125	250	
		15	--	90	180	
Setup Time	t_{su}	5.0	100	--	--	ns
		10	40	--	--	
		15	30	--	--	
Hold Time	t_h	5.0	60	--	--	ns
		10	40	--	--	
		15	30	--	--	
Latch Enable Pulse Width	$t_{WL}(LE)$	5.0	520	260	--	ns
		10	220	110	--	
		15	130	65	--	

*The formulas given are for the typical characteristics only.

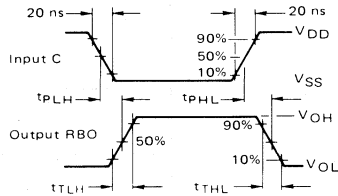
MC14513B

FIGURE 2 – DYNAMIC SIGNAL WAVEFORMS

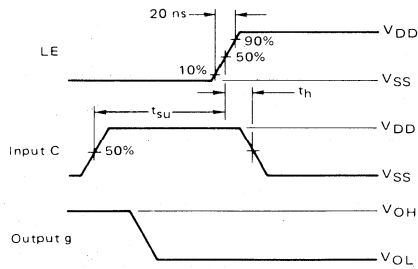
a. Data Propagation Delay: Inputs RBI, D and LE low, and Inputs A, B, $\overline{B\overline{T}}$ and $\overline{C\overline{T}}$ high.



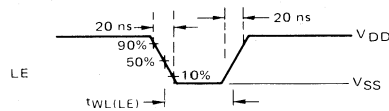
b. Inputs A, B, D and LE low, and Inputs RBI, $\overline{B\overline{T}}$ and $\overline{C\overline{T}}$ high.



c. Setup and Hold Times: Input RBI and D low, Inputs A, B, $\overline{B\overline{T}}$ and $\overline{C\overline{T}}$ high.

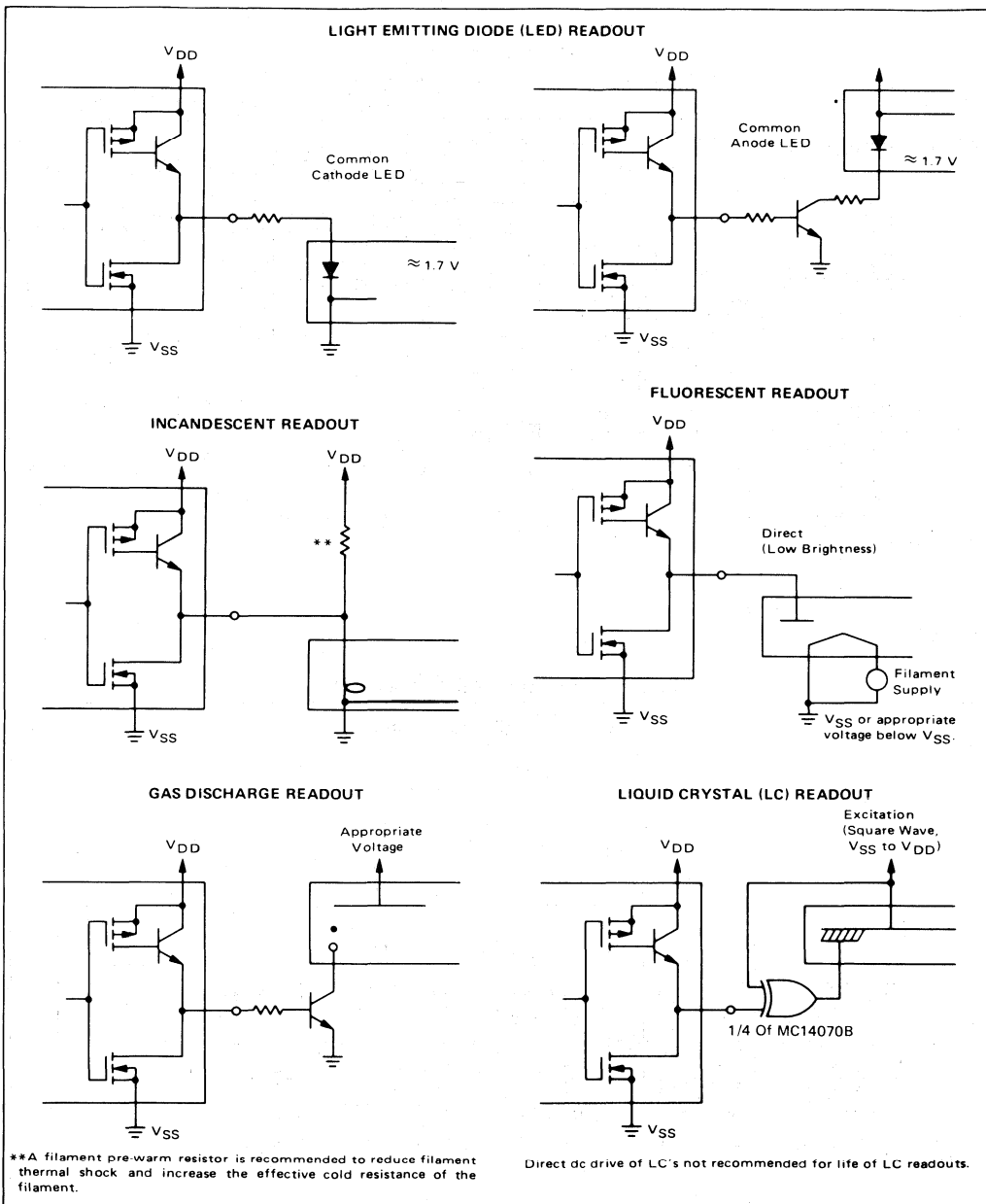


d. Pulse Width: Data DCBA strobed into latches.



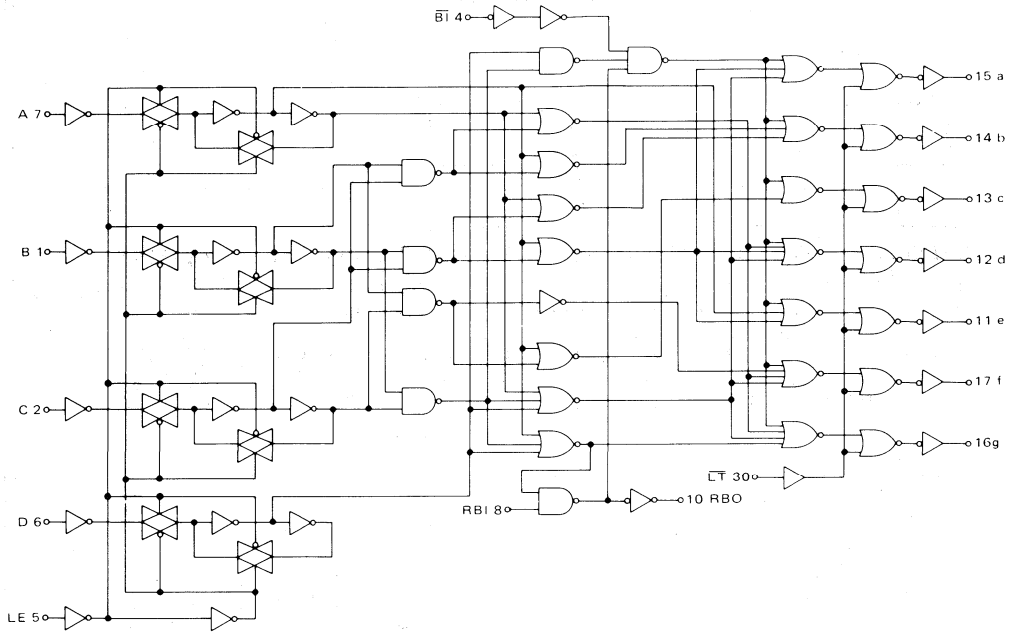
MC14513B

CONNECTIONS TO VARIOUS DISPLAY READOUTS



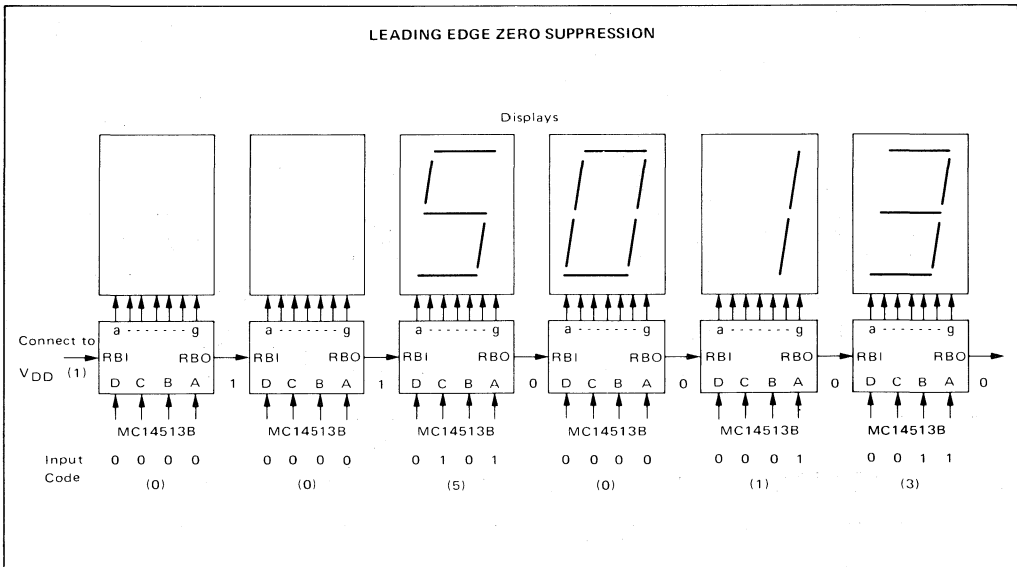
MC14513B

LOGIC DIAGRAM



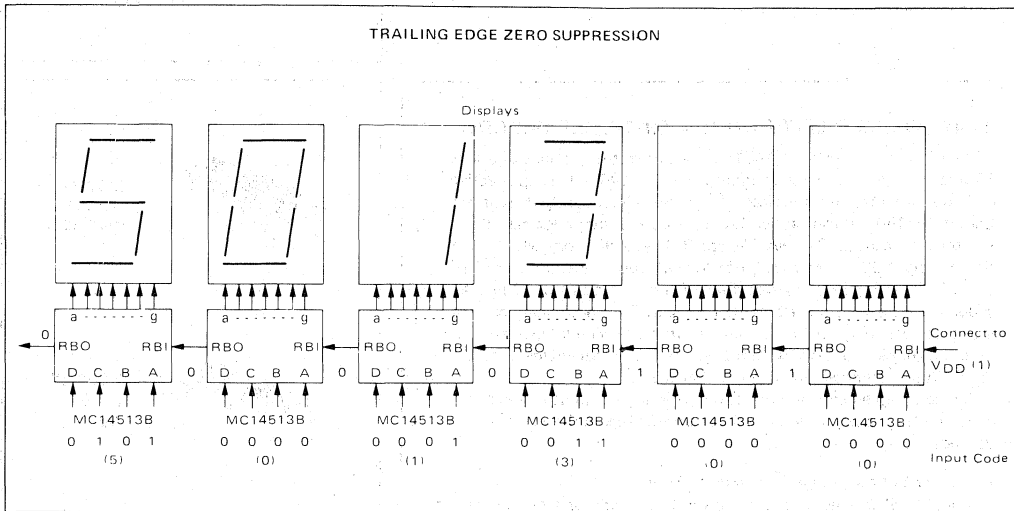
TYPICAL APPLICATIONS FOR RIPPLE BLANKING

LEADING EDGE ZERO SUPPRESSION



MC14513B

TYPICAL APPLICATIONS FOR RIPPLE BLANKING (Cont)





MOTOROLA

**MC14514B
MC14515B**

4-BIT TRANSPARENT LATCH/4-TO-16 LINE DECODER

The MC14514B and MC14515B are two output options of a 4 to 16 line decoder with latched inputs. The MC14514B (output active high option) presents a logical "1" at the selected output, whereas the MC14515B (output active low option) presents a logical "0" at the selected output. The latches are R-S type flip-flops which hold the last input data presented prior to the strobe transition from "1" to "0". These high and low options of a 4-bit latch/4 to 16 line decoder are constructed with N-channel and P-channel enhancement mode devices in a single monolithic structure. The latches are R-S type flip-flops and data is admitted upon a signal incident at the strobe input, decoded, and presented at the output.

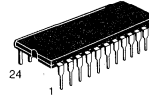
These complementary circuits find primary use in decoding applications where low power dissipation and/or high noise immunity is desired.

- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range

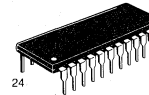
MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V _{DD}	DC Supply Voltage	-0.5 to +18.0	V
V _{in} , V _{out}	Input or Output Voltage (DC or Transient)	-0.5 to V _{DD} + 0.5	V
I _{in} , I _{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
P _D	Power Dissipation, per Package†	500	mW
T _{stg}	Storage Temperature	-65 to +150	°C
T _L	Lead Temperature (8-Second Soldering)	260	°C

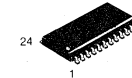
*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P and D/DW" Packages: -7.0 mW/°C From 65°C To 125°C
Ceramic "L" Packages: -12 mW/°C From 100°C To 125°C



**L SUFFIX
CERAMIC
CASE 623**



**P SUFFIX
PLASTIC
CASE 709**



**DW SUFFIX
SOIC
CASE 751E**

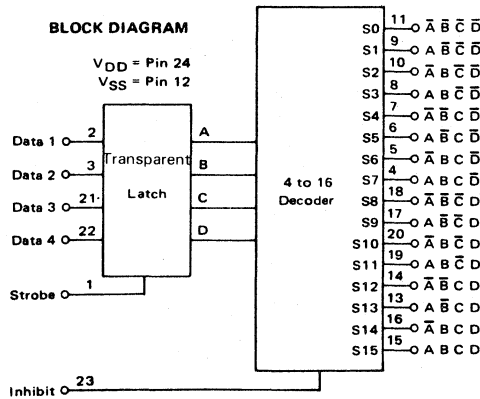
ORDERING INFORMATION

MC14XXXBCP Plastic
MC14XXXBCL Ceramic
MC14XXXBDW SOIC

T_A = -55° to 125°C for all packages.

6

BLOCK DIAGRAM



DECODE TRUTH TABLE (Strobe = 1)*

INHIBIT	DATA INPUTS				SELECTED OUTPUT
	D	C	B	A	MC14514 = Logic "1" MC14515 = Logic "0"
0	0	0	0	0	S0
0	0	0	0	1	S1
0	0	0	1	0	S2
0	0	0	1	1	S3
0	0	1	0	0	S4
0	0	1	0	1	S5
0	0	1	1	0	S6
0	0	1	1	1	S7
0	1	0	0	0	S8
0	1	0	0	1	S9
0	1	0	1	0	S10
0	1	0	1	1	S11
0	1	1	0	0	S12
0	1	1	0	1	S13
0	1	1	1	0	S14
0	1	1	1	1	S15
1	X	X	X	X	All Outputs = 0, MC14514 All Outputs = 1, MC14515

X = Don't Care
*Strobe = 0, Data is latched

MC14514B•MC14515B

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V _{DD} Vdc	-55°C		25°C			125°C		Unit	
			Min	Max	Min	Typ #	Max	Min	Max		
Output Voltage V _{in} = V _{DD} or 0	V _{OL}	5.0	—	0.05	—	0	0.05	—	0.05	Vdc	
		10	—	0.05	—	0	0.05	—	0.05		
15		—	0.05	—	0	0.05	—	0.05			
V _{in} = 0 or V _{DD}	V _{OH}	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc	
		10	9.95	—	9.95	10	—	9.95	—		
		15	14.95	—	14.95	15	—	14.95	—		
Input Voltage (V _O = 4.5 or 0.5 Vdc) (V _O = 9.0 or 1.0 Vdc) (V _O = 13.5 or 1.5 Vdc)	V _{IL}	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc	
		10	—	3.0	—	4.50	3.0	—	3.0		
15		—	4.0	—	6.75	4.0	—	4.0			
(V _O = 0.5 or 4.5 Vdc) (V _O = 1.0 or 9.0 Vdc) (V _O = 1.5 or 13.5 Vdc)	V _{IH}	5.0	3.5	—	3.5	2.75	—	3.5	—	Vdc	
		10	7.0	—	7.0	5.50	—	7.0	—		
		15	11	—	11	8.25	—	11	—		
Output Drive Current (V _{OH} = 2.5 Vdc) (V _{OH} = 4.6 Vdc) (V _{OH} = 9.5 Vdc) (V _{OH} = 13.5 Vdc) (V _{OL} = 0.4 Vdc) (V _{OL} = 0.5 Vdc) (V _{OL} = 1.5 Vdc)	Source	I _{OH}	5.0	-1.2	—	-1.0	-1.7	—	-0.7	—	mAdc
			5.0	-0.25	—	-0.2	-0.36	—	-0.14	—	
			10	-0.62	—	-0.5	-0.9	—	-0.35	—	
		15	-1.8	—	-1.5	-3.5	—	-1.1	—		
	Sink	I _{OL}	5.0	0.64	—	0.51	0.88	—	0.36	—	mAdc
			10	1.6	—	1.3	2.25	—	0.9	—	
15			4.2	—	3.4	8.8	—	2.4	—		
Input Current	I _{in}	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	μAdc	
Input Capacitance (V _{in} = 0)	C _{in}	—	—	—	—	5.0	7.5	—	—	pF	
Quiescent Current (Per Package)	I _{DD}	5.0	—	5.0	—	0.005	5.0	—	150	μAdc	
		10	—	10	—	0.010	10	—	300		
		15	—	20	—	0.015	20	—	600		
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C _L = 50 pF on all outputs, all buffers switching)	I _T	5.0	I _T = (1.35 μA/kHz) f + I _{DD}						μAdc		
		10	I _T = (2.70 μA/kHz) f + I _{DD}								
		15	I _T = (4.05 μA/kHz) f + I _{DD}								

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) V/k$$

where: I_T is in μA (per package), C_L in pF, V = (V_{DD} - V_{SS}) in volts, f in kHz is input frequency, and k = 0.002.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range V_{SS} ≤ (V_{in} or V_{out}) ≤ V_{DD}.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

MC14514B • MC14515B

SWITCHING CHARACTERISTICS* ($C_L = 50 \text{ pF}$, $T_A = 25^\circ\text{C}$)

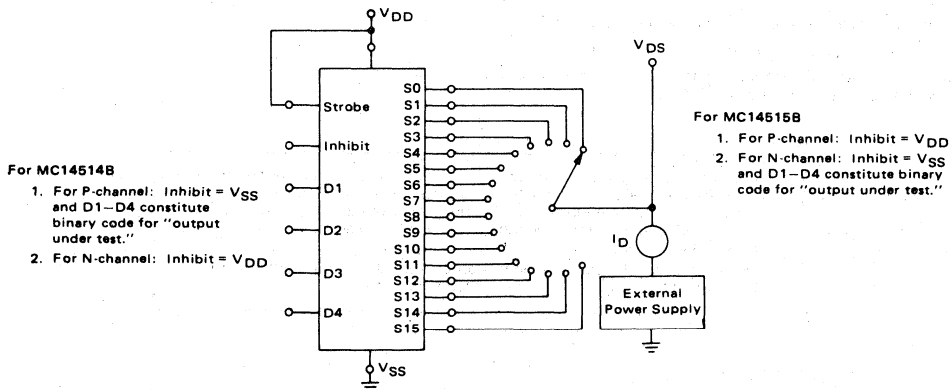
Characteristic	Symbol	V_{DD}	All Types			Unit
			Min	Typ #	Max	
Output Rise Time $t_{TLH} = (3.0 \text{ ns/pF}) C_L + 30 \text{ ns}$ $t_{TLH} = (1.5 \text{ ns/pF}) C_L + 15 \text{ ns}$ $t_{TLH} = (1.1 \text{ ns/pF}) C_L + 10 \text{ ns}$	t_{TLH}	5.0 10 15	— — —	180 90 65	360 180 130	ns
Output Fall Time $t_{THL} = (1.5 \text{ ns/pF}) C_L + 25 \text{ ns}$ $t_{THL} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$ $t_{THL} = (0.55 \text{ ns/pF}) C_L + 9.5 \text{ ns}$	t_{THL}	5.0 10 15	— — —	100 50 40	200 100 80	ns
Propagation Delay Time; Data, Strobe to S $t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 465 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 192 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 125 \text{ ns}$	t_{PLH}, t_{PHL}	5.0 10 15	— — —	550 225 150	1100 450 300	ns
Inhibit Propagation Delay Times $t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 315 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 117 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 75 \text{ ns}$	t_{PLH}, t_{PHL}	5.0 10 15	— — —	400 150 100	800 300 200	ns
Setup Time Data to Strobe	t_{su}	5.0 10 15	250 100 75	125 50 38	— — —	ns
Hold Time Strobe to Data	t_h	5.0 10 15	-20 0 10	-100 -40 -30	— — —	ns
Strobe Pulse Width	t_{WH}	5.0 10 15	350 100 75	175 50 38	— — —	ns

*The formulas given are for the typical characteristics only at 25°C .

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

6

FIGURE 1 — DRAIN CHARACTERISTICS TEST CIRCUIT



MC14514B•MC14515B

FIGURE 2 – DYNAMIC POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

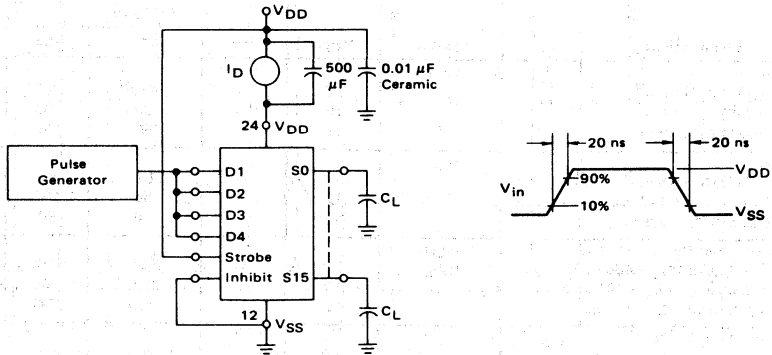
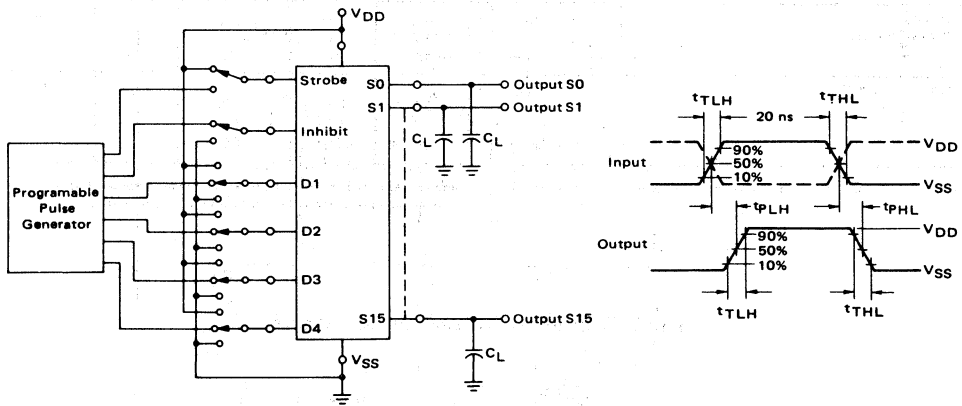
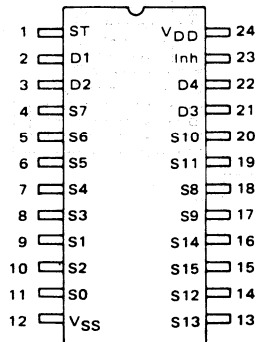


FIGURE 3 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

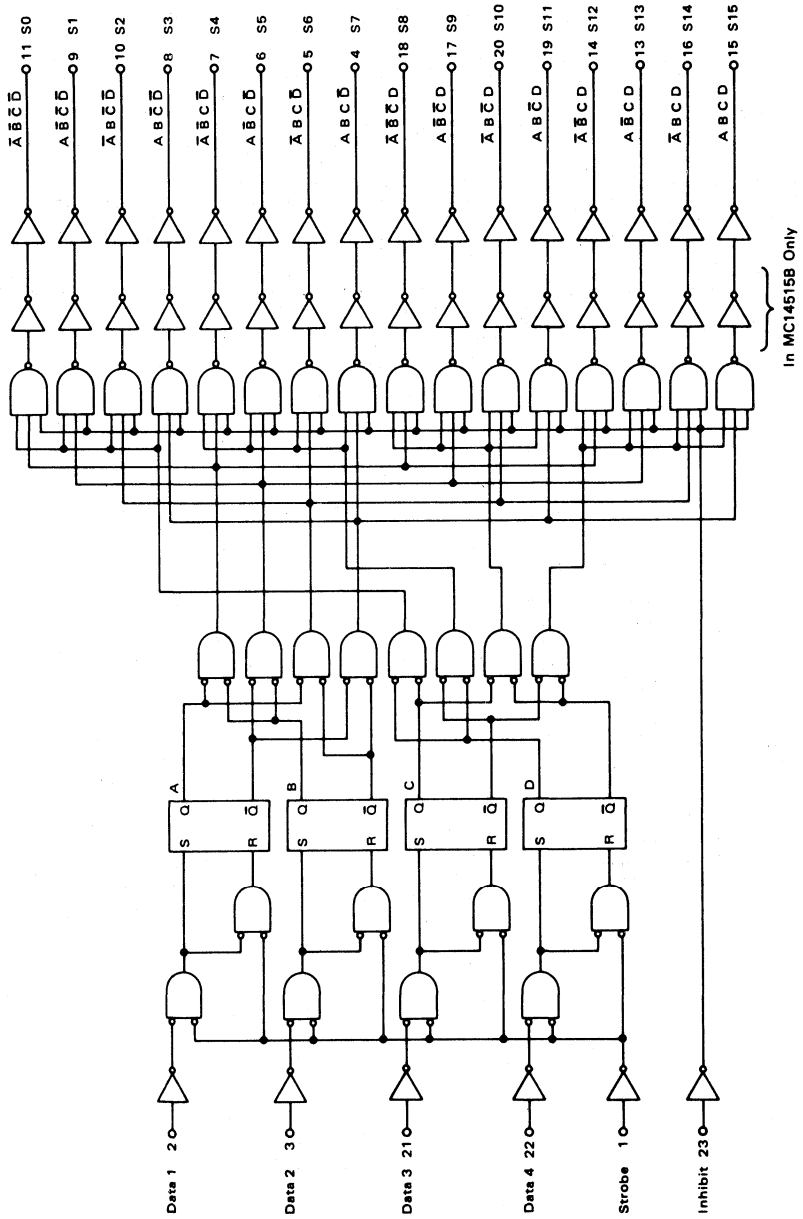


PIN ASSIGNMENT



MC14514B•MC14515B

LOGIC DIAGRAM



MC14514B•MC14515B

COMPLEX DATA ROUTING

Two MC14512 eight-channel data selectors are used here with the MC14514B four-bit latch/decoder to effect a complex data routing system. A total of 16 inputs from data registers are selected and transferred via a 3-state data bus to a data distributor for rearrangement and entry into 16 output registers. In this way sequential data can be re-routed or intermixed according to patterns determined by data select and distribution inputs.

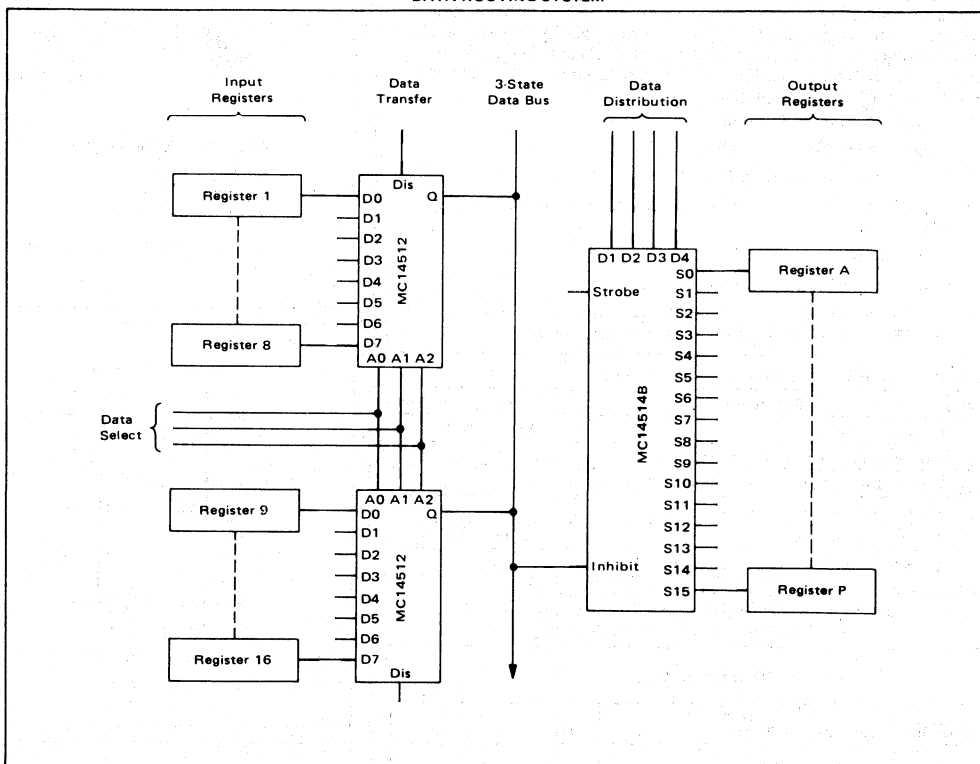
Data is placed into the routing scheme via the eight inputs on both MC14512 data selectors. One register is assigned to each input. The signals on A0, A1, and A2 choose one of eight inputs for transfer out to the 3-state data bus. A fourth signal, labelled Dis, disables one of the MC14512 selectors, assuring transfer of data from only one register.

In addition to a choice of input registers, 1 thru 16, the rate of transfer of the sequential information can also be varied. That is, if the MC14512 were addressed at a rate that is eight times faster

than the shift frequency of the input registers, the most significant bit (MSB) from each register could be selected for transfer to the data bus. Therefore, all of the most significant bits from all of the registers can be transferred to the data bus before the next most significant bit is presented for transfer by the input registers.

Information from the 3-state bus is redistributed by the MC14514B four-bit latch/decoder. Using the four-bit address, D1 thru D4, the information on the inhibit line can be transferred to the addressed output line to the desired output registers, A thru P. This distribution of data bits to the output registers can be made in many complex patterns. For example, all of the most significant bits from the input registers can be routed into output register A, all of the next most significant bits into register B, etc. In this way horizontal, vertical, or other methods of data slicing can be implemented.

DATA ROUTING SYSTEM





MOTOROLA

MC14516B

BINARY UP/DOWN COUNTER

The MC14516B synchronous up/down binary counter is constructed with MOS P-channel and N-channel enhancement mode devices in a monolithic structure.

This counter can be preset by applying the desired value, in binary, to the Preset inputs (P0, P1, P2, P3) and then bringing the Preset Enable (PE) high. The direction of counting is controlled by applying a high (for up counting) or a low (for down counting) to the UP/DOWN input. The state of the counter changes on the positive transition of the clock input.

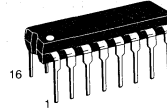
Cascading can be accomplished by connecting the Carry Out to the Carry In of the next stage while clocking each counter in parallel. The outputs (Q0, Q1, Q2, Q3) can be reset to a low state by applying a high to the reset (R) pin.

This CMOS counter finds primary use in up/down and difference counting. Other applications include: (1) Frequency synthesizer applications where low power dissipation and/or high noise immunity is desired, (2) Analog-to-digital and digital-to-analog conversions, and (3) Magnitude and sign generation.

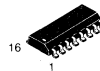
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Internally Synchronous for High Speed
- Logic Edge-Clocked Design – Count Occurs on Positive Going Edge of Clock
- Single Pin Reset
- Asynchronous Preset Enable Operation
- Capable of Driving Two Low-Power TTL Loads or One Low-Power Schottky Load Over the Rated Temperature Range



L SUFFIX
CERAMIC
CASE 620



P SUFFIX
PLASTIC
CASE 648



D SUFFIX
SOIC
CASE 751B

ORDERING INFORMATION

MC14XXXBCP Plastic
MC14XXXBCL Ceramic
MC14XXXBD SOIC

T_A = -55° to 125°C for all packages.

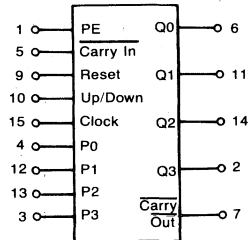
MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V _{DD}	DC Supply Voltage	-0.5 to +18.0	V
V _{in} , V _{out}	Input or Output Voltage (DC or Transient)	-0.5 to V _{DD} + 0.5	V
I _{in} , I _{out}	Input or Output Current (DC or Transient), per Pin	± 10	mA
P _D	Power Dissipation, per Package†	500	mW
T _{stg}	Storage Temperature	-65 to +150	°C
T _L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.

†Temperature Derating: Plastic "P and D/DW" Packages: -7.0 mW/°C From 65°C To 125°C
Ceramic "L" Packages: -12 mW/°C From 100°C To 125°C

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

TRUTH TABLE

Carry In	Up/Down	Preset Enable	Reset	Clock	Action
1	X	0	0	X	No Count
0	1	0	0		Count Up
0	0	0	0		Count Down
X	X	1	0	X	Preset
X	X	X	1	X	Reset

X = Don't Care

Note: When counting up, the Carry Out signal is normally high and is low only when Q0 through Q3 are high and Carry In is low. When counting down, Carry Out is low only when Q0 through Q3 and Carry In are low.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range V_{SS} ≤ (V_{in} or V_{out}) ≤ V_{DD}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

MC14516B

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V _{DD} Vdc	-55°C		25°C			125°C		Unit	
			Min	Max	Min	Typ #	Max	Min	Max		
Output Voltage V _{in} = V _{DD} or 0	V _{OL}	5.0	—	0.05	—	0	0.05	—	0.05	Vdc	
		10	—	0.05	—	0	0.05	—	0.05		
V _{in} = 0 or V _{DD}	V _{OH}	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc	
		10	9.95	—	9.95	10	—	9.95	—		
Input Voltage (V _O = 4.5 or 0.5 Vdc) (V _O = 9.0 or 1.0 Vdc) (V _O = 13.5 or 1.5 Vdc)	V _{IL}	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc	
		10	—	3.0	—	4.50	3.0	—	3.0		
(V _O = 0.5 or 4.5 Vdc) (V _O = 1.0 or 9.0 Vdc) (V _O = 1.5 or 13.5 Vdc)	V _{IH}	5.0	3.5	—	3.5	2.75	—	3.5	—	Vdc	
		10	7.0	—	7.0	5.50	—	7.0	—		
Output Drive Current (V _{OH} = 2.5 Vdc) (V _{OH} = 4.6 Vdc) (V _{OH} = 9.5 Vdc) (V _{OH} = 13.5 Vdc)	Source I _{OH}	5.0	-3.0	—	-2.4	-4.2	—	-1.7	—	mA _{dc}	
		5.0	-0.64	—	-0.51	-0.88	—	-0.36	—		
(V _{OL} = 0.4 Vdc) (V _{OL} = 0.5 Vdc) (V _{OL} = 1.5 Vdc)	Sink I _{OL}	5.0	0.64	—	0.51	0.88	—	0.36	—	mA _{dc}	
		10	1.6	—	1.3	2.25	—	0.9	—		
		15	4.2	—	3.4	8.8	—	2.4	—		
Input Current	I _{in}	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	μA _{dc}	
Input Capacitance (V _{in} = 0)	C _{in}	—	—	—	—	5.0	7.5	—	—	pF	
Quiescent Current (Per Package)	I _{DD}	5.0	—	5.0	—	0.005	5.0	—	150	μA _{dc}	
		10	—	10	—	0.010	10	—	300		
		15	—	20	—	0.015	20	—	600		
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C _L = 50 pF on all outputs, all buffers switching)	I _T	5.0	I _T = (0.58 μA/kHz) f + I _{DD} I _T = (1.20 μA/kHz) f + I _{DD} I _T = (1.70 μA/kHz) f + I _{DD}								μA _{dc}
		10									
		15									

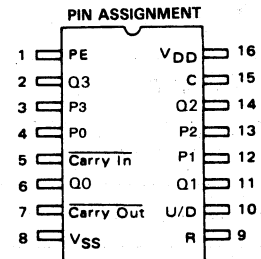
#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) V/k$$

where: I_T is in μA (per package), C_L in pF, V = (V_{DD} - V_{SS}) in volts, f in kHz is input frequency, and k = 0.001.



MC14516B

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

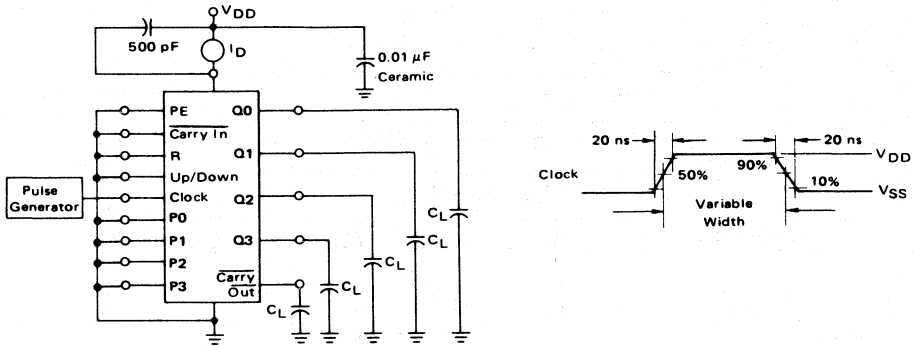
Characteristic	Symbol	V _{DD}	All Types			Unit
			Min	Typ #	Max	
Output Rise and Fall Time t _{TLH} , t _{THL} = (1.5 ns/pF) C _L + 25 ns t _{TLH} , t _{THL} = (0.75 ns/pF) C _L + 12.5 ns t _{TLH} , t _{THL} = (0.55 ns/pF) C _L + 9.5 ns	t _{TLH} , t _{THL}	5.0 10 15	— — —	100 50 40	200 100 80	ns
Propagation Delay Time Clock to Q t _{PLH} , t _{PHL} = (1.7 ns/pF) C _L + 230 ns t _{PLH} , t _{PHL} = (0.66 ns/pF) C _L + 97 ns t _{PLH} , t _{PHL} = (0.5 ns/pF) C _L + 75 ns Clock to Carry Out t _{PLH} , t _{PHL} = (1.7 ns/pF) C _L + 230 ns t _{PLH} , t _{PHL} = (0.66 ns/pF) C _L + 97 ns t _{PLH} , t _{PHL} = (0.5 ns/pF) C _L + 75 ns Carry In to Carry Out t _{PLH} , t _{PHL} = (1.7 ns/pF) C _L + 230 ns t _{PLH} , t _{PHL} = (0.66 ns/pF) C _L + 97 ns t _{PLH} , t _{PHL} = (0.5 ns/pF) C _L + 75 ns Preset or Reset to Q t _{PLH} , t _{PHL} = (1.7 ns/pF) C _L + 230 ns t _{PLH} , t _{PHL} = (0.66 ns/pF) C _L + 97 ns t _{PLH} , t _{PHL} = (0.5 ns/pF) C _L + 75 ns Preset or Reset to Carry Out t _{PLH} , t _{PHL} = (1.7 ns/pF) C _L + 465 ns t _{PLH} , t _{PHL} = (0.66 ns/pF) C _L + 192 ns t _{PLH} , t _{PHL} = (0.5 ns/pF) C _L + 125 ns	t _{PLH} , t _{PHL}	5.0 10 15	— — —	315 130 100	630 260 200	ns
Reset Pulse Width	t _w	5.0 10 15	380 200 160	190 100 80	— — —	ns
Clock Pulse Width	t _{WH}	5.0 10 15	350 170 140	200 100 75	— — —	ns
Clock Pulse Frequency	f _{cl}	5.0 10 15	— — —	3.0 6.0 8.0	1.5 3.0 4.0	MHz
Preset or Reset Removal Time The Preset or Reset signal must be low prior to a positive-going transition of the clock.	t _{rem}	5.0 10 15	650 230 180	325 115 90	— — —	ns
Clock Rise and Fall Time	t _{TLH} , t _{THL}	5.0 10 15	— — —	— — —	15 5 4	μs
Setup Time Carry In to Clock	t _{su}	5.0 10 15	260 120 100	130 60 50	— — —	ns
Hold Time Clock to Carry In	t _h	5.0 10 15	0 20 20	-60 -20 0	— — —	ns
Setup Time Up/Down to Clock	t _{su}	5.0 10 15	500 200 150	250 100 75	— — —	ns
Hold Time Clock to Up/Down	t _h	5.0 10 15	-70 -10 0	-160 -60 -40	— — —	ns
Setup Time Pn to PE	t _{su}	5.0 10 15	-40 -30 -25	-120 -70 -50	— — —	ns
Hold Time PE to Pn	t _h	5.0 10 15	480 420 420	240 210 210	— — —	ns
Preset Enable Pulse Width	t _{WH}	5.0 10 15	200 100 80	100 50 40	— — —	ns

*The formulas given are for the typical characteristics only at 25°C.

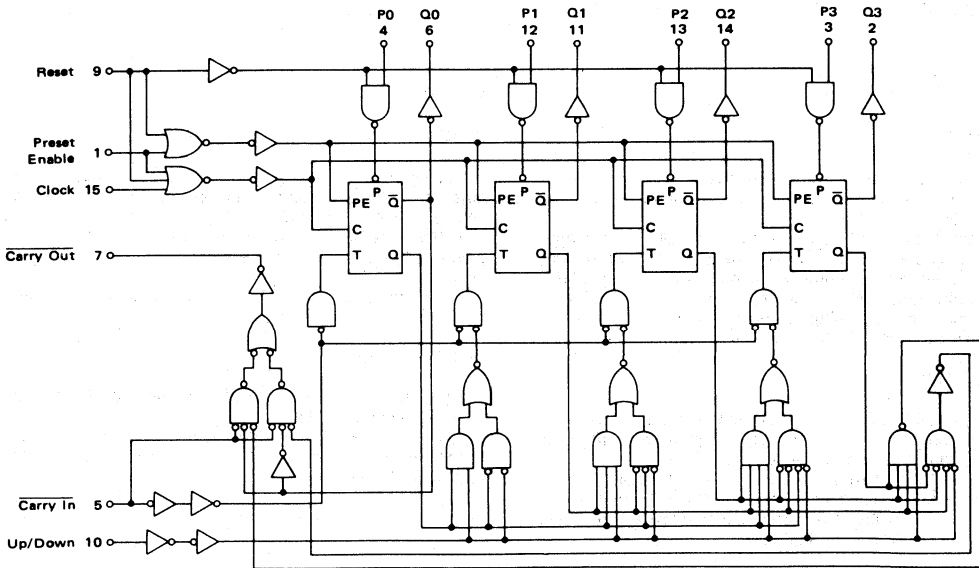
#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

MC14516B

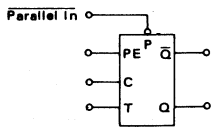
FIGURE 1 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM



LOGIC DIAGRAM



TOGGLE FLIP-FLOP



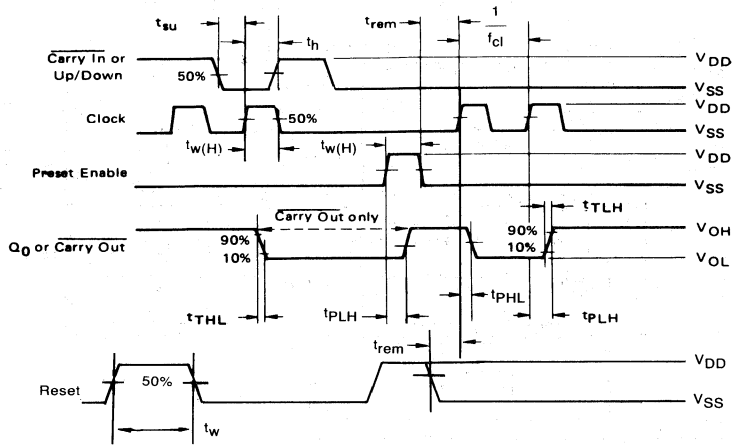
FLIP-FLOP FUNCTIONAL TRUTH TABLE

PRESET ENABLE	CLOCK	T	Q_{n+1}
1	X	X	Parallel In
0		0	Q_n
0		1	\bar{Q}_n
0		X	Q_n

X = Don't Care

MC14516B

FIGURE 2 – SWITCHING TIME WAVEFORMS



PIN DESCRIPTIONS

INPUTS

P0, P1, P2, P3, Preset Inputs (Pins 4, 12, 13, 3) — Data on these inputs is loaded into the counter when PE is taken high.

Carry In, (Pin 5) — This active-low input is used when cascading stages. Carry In is usually connected to Carry Out of the previous stage. While high, Clock is inhibited.

Clock, (Pin 15) — Binary data is incremented or decremented, depending on the direction of count, on the positive transition of this input.

OUTPUTS

Q0, Q1, Q2, Q3, Binary outputs (Pins 6, 11, 14, 2) — Binary data is present on these outputs with Q0 corresponding to the least significant bit.

Carry Out, (Pin 7) — Used when cascading stages, Carry Out is usually connected to Carry In of the next stage. This synchronous output is active low and may also be used to indicate terminal count.

CONTROLS

PE, Preset Enable, (Pin 1) — Asynchronously loads data on the Preset Inputs. This pin is active high and inhibits the clock when high.

R, Reset, (Pin 9) — Asynchronously resets the Q outputs to a low state. This pin is active high and inhibits the clock when high.

Up/Down, (Pin 10) — Controls the direction of count, high for up count, low for down count.

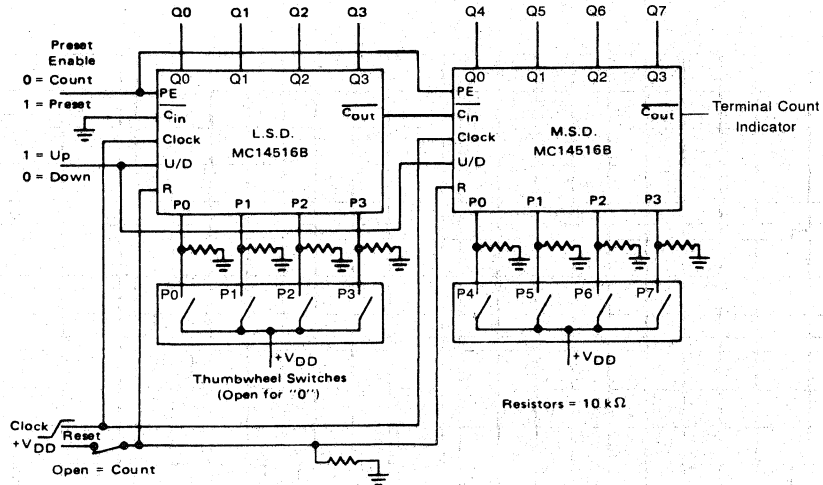
SUPPLY PINS

VSS, Negative Supply Voltage, (Pin 8) — This pin is usually connected to ground.

VDD, Positive Supply Voltage, (Pin 16) — This pin is connected to a positive supply voltage ranging from 3.0 volts to 18.0 volts.

MC14516B

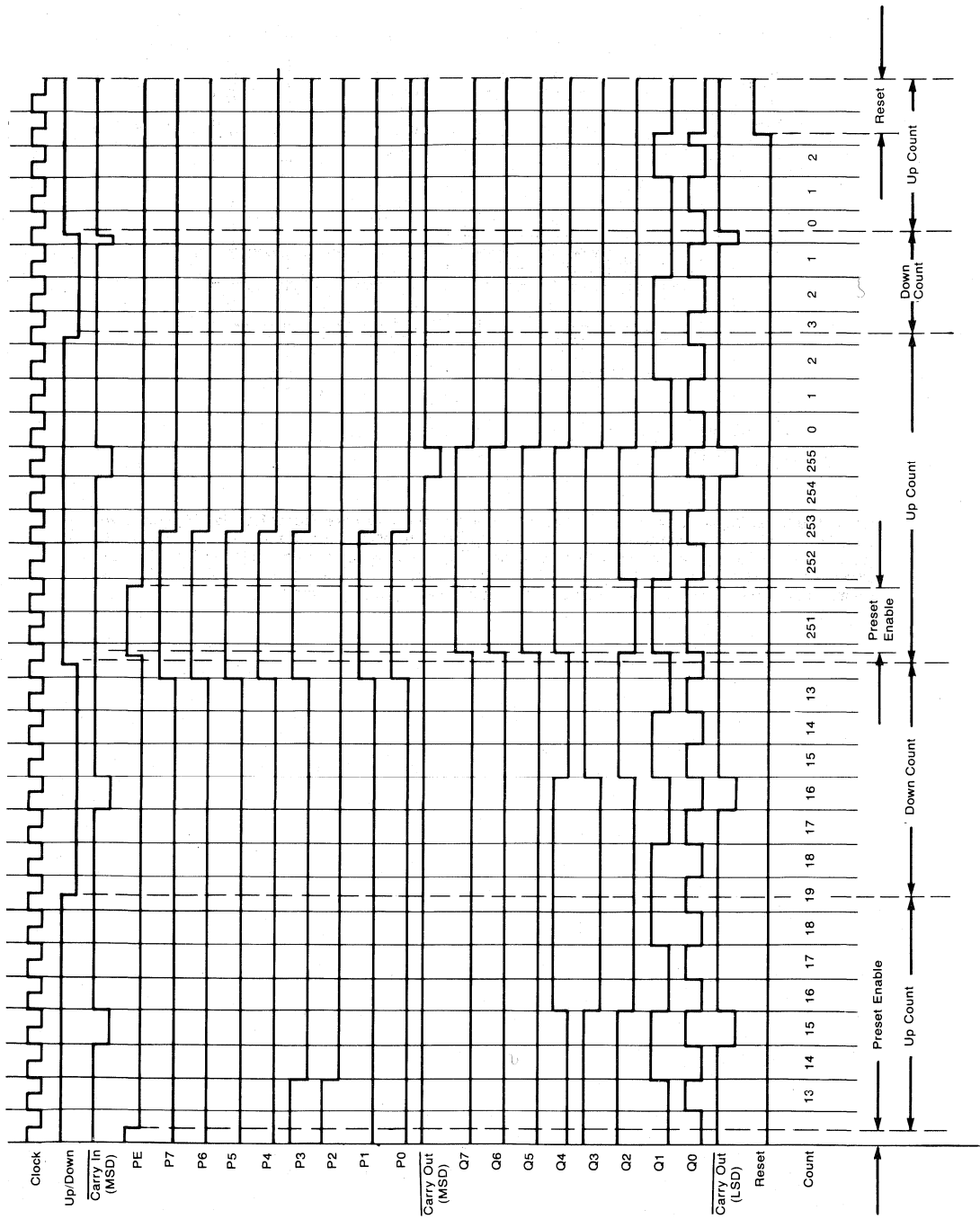
FIGURE 3 — PRESETTABLE CASCADED 8-BIT UP/DOWN COUNTER



Note: The Least Significant Digit (L.S.D.) counts from a preset value once Preset Enable (PE) goes low. The Most Significant Digit (M.S.D.) is disabled while C_{in} is high. When the count of the L.S.D. reaches 0 (count down mode) or reaches 15 (count up mode), C_{out} goes low for one complete clock cycle, thus allowing the next counter to decrement/increment one count. (See Timing Diagram) The L.S.D. now counts through another cycle (15 clock pulses) and the above cycle is repeated.

MC14516B

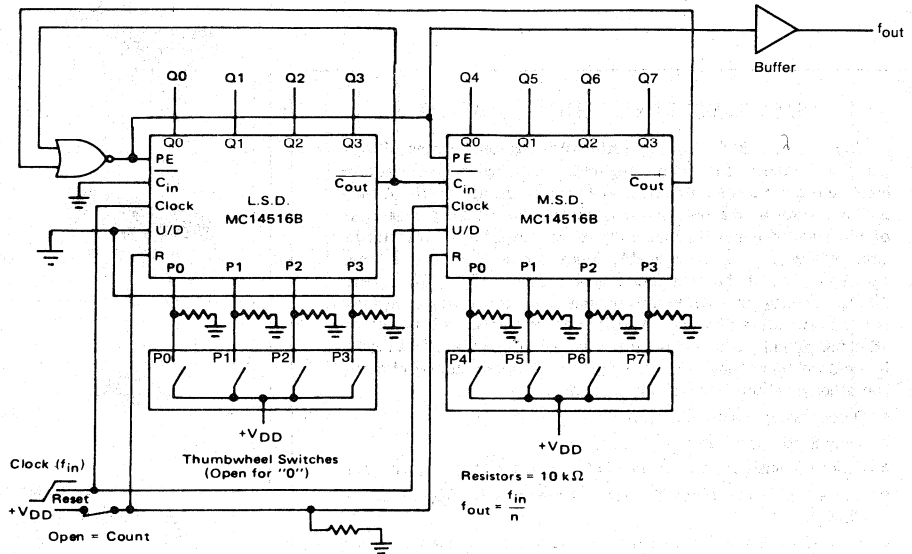
TIMING DIAGRAM FOR THE PRESETTABLE CASCADED 8-BIT UP/DOWN COUNTER



6

MC14516B

FIGURE 4 — PROGRAMMABLE CASCADED FREQUENCY DIVIDER



Note: The programmable frequency divider can be set by applying the desired divide ratio, in binary, to the preset inputs. For example, the maximum divide ratio of 255 may be obtained by applying a 1111 1111 to the preset inputs P0 to P7. For this divide operation, both counters should be configured in the count down mode. The divide ratio of zero is an undefined state and should be avoided.



MOTOROLA

DUAL 64-BIT STATIC SHIFT REGISTER

The MC14517B dual 64-bit static shift register consists of two identical, independent, 64-bit registers. Each register has separate clock and write enable inputs, as well as outputs at bits 16, 32, 48, and 64. Data at the data input is entered by clocking, regardless of the state of the write enable input. An output is disabled (open circuited) when the write enable input is high. During this time, data appearing at the data input as well as the 16-bit, 32-bit, and 48-bit taps may be entered into the device by application of a clock pulse. This feature permits the register to be loaded with 64 bits in 16 clock periods, and also permits bus logic to be used. This device is useful in time delay circuits, temporary memory storage circuits, and other serial shift register applications.

- Diode Protection on All Inputs
- Fully Static Operation
- Output Transitions Occur on the Rising Edge of the Clock Pulse
- Exceedingly Slow Input Transition Rates May Be Applied to the Clock Input
- 3-State Output at 64th-Bit Allows Use in Bus Logic Applications
- Shift Registers of any Length may be Fully Loaded with 16 Clock Pulses
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	-0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	-0.5 to $V_{DD} + 0.5$	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	± 10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

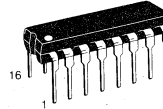
*Maximum Ratings are those values beyond which damage to the device may occur.

†Temperature Derating: Plastic "P" and D/DW" Packages: -7.0 mW/°C From 65°C To 125°C
Ceramic "L" Packages: -12 mW/°C From 100°C To 125°C

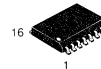
MC14517B



L SUFFIX
CERAMIC
CASE 620



P SUFFIX
PLASTIC
CASE 648



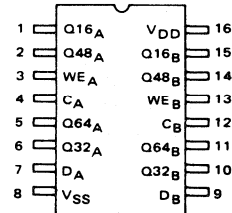
DW SUFFIX
SOIC
CASE 751G

ORDERING INFORMATION

MC14XXXBCP Plastic
MC14XXXBCL Ceramic
MC14XXXBDW SOIC

$T_A = -55^\circ$ to 125°C for all packages.

PIN ASSIGNMENT



FUNCTIONAL TRUTH TABLE

CLOCK	WRITE ENABLE	DATA	16-BIT TAP	32-BIT TAP	48-BIT TAP	64-BIT TAP
0	0	X	Content of 16-Bit Displayed	Content of 32-Bit Displayed	Content of 48-Bit Displayed	Content of 64-Bit Displayed
0	1	X	High Impedance	High Impedance	High Impedance	High Impedance
1	0	X	Content of 16-Bit Displayed	Content of 32-Bit Displayed	Content of 48-Bit Displayed	Content of 64-Bit Displayed
1	1	X	High Impedance	High Impedance	High Impedance	High Impedance
	0	Data entered into 1st Bit	Content of 16-Bit Displayed	Content of 32-Bit Displayed	Content of 48-Bit Displayed	Content of 64-Bit Displayed
	1	Data entered into 1st Bit	Data at tap entered into 17-Bit	Data at tap entered into 33-Bit	Data at tap entered into 49-Bit	High Impedance
	0	X	Content of 16-Bit Displayed	Content of 32-Bit Displayed	Content of 48-Bit Displayed	Content of 64-Bit Displayed
	1	X	High Impedance	High Impedance	High Impedance	High Impedance

X = Don't Care

MC14517B

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V _{DD} Vdc	-55°C		25°C			125°C		Unit
			Min	Max	Min	Typ #	Max	Min	Max	
Output Voltage V _{in} = V _{DD} or 0 V _{in} = 0 or V _{DD}	"0" Level V _{OL}	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
		10	—	0.05	—	0	0.05	—	0.05	
		15	—	0.05	—	0	0.05	—	0.05	
	"1" Level V _{OH}	5.0	4.95	—	4.95	5.0	—	4.95	—	
		10	9.95	—	9.95	10	—	9.95	—	
		15	14.95	—	14.95	15	—	14.95	—	
Input Voltage (V _O = 4.5 or 0.5 Vdc) (V _O = 9.0 or 1.0 Vdc) (V _O = 13.5 or 1.5 Vdc) (V _O = 0.5 or 4.5 Vdc) (V _O = 1.0 or 9.0 Vdc) (V _O = 1.5 or 13.5 Vdc)	"0" Level V _{IL}	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc
		10	—	3.0	—	4.50	3.0	—	3.0	
		15	—	4.0	—	6.75	4.0	—	4.0	
	"1" Level V _{IH}	5.0	3.5	—	3.5	2.75	—	3.5	—	
		10	7.0	—	7.0	5.50	—	7.0	—	
		15	11	—	11	8.25	—	11	—	
Output Drive Current (V _{OH} = 2.5 Vdc) (V _{OH} = 4.6 Vdc) (V _{OH} = 9.5 Vdc) (V _{OH} = 13.5 Vdc) (V _{OL} = 0.4 Vdc) (V _{OL} = 0.5 Vdc) (V _{OL} = 1.5 Vdc)	Source I _{OH}	5.0	-3.0	—	-2.4	-4.2	—	-1.7	—	mAdc
		10	-0.64	—	-0.51	-0.88	—	-0.36	—	
		15	-1.6	—	-1.3	-2.25	—	-0.9	—	
	Sink I _{OL}	5.0	0.64	—	0.51	0.88	—	0.36	—	
		10	1.6	—	1.3	2.25	—	0.9	—	
		15	4.2	—	3.4	8.8	—	2.4	—	
Input Current	I _{in}	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	μAdc
Input Capacitance (V _{in} = 0)	C _{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)	I _{DD}	5.0	—	5.0	—	0.005	5.0	—	150	μAdc
		10	—	10	—	0.010	10	—	300	
		15	—	20	—	0.015	20	—	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C _L = 50 pF on all outputs, all buffers switching)	I _T	5.0	I _T = (4.2 μA/kHz) f + I _{DD}							μAdc
		10	I _T = (8.8 μA/kHz) f + I _{DD}							
		15	I _T = (13.7 μA/kHz) f + I _{DD}							
Three-State Leakage Current	I _{TL}	15	—	±0.1	—	±0.00001	±0.1	—	±3.0	μAdc

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) Vfk$$

where: I_T is in μA (per package), C_L in pF, V = (V_{DD} - V_{SS}) in volts, f in kHz is input frequency, and k = 0.004.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range V_{SS} ≤ (V_{in} or V_{out}) ≤ V_{DD}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

MC14517B

SWITCHING CHARACTERISTICS* ($C_L = 50 \text{ pF}$, $T_A = 25^\circ\text{C}$)

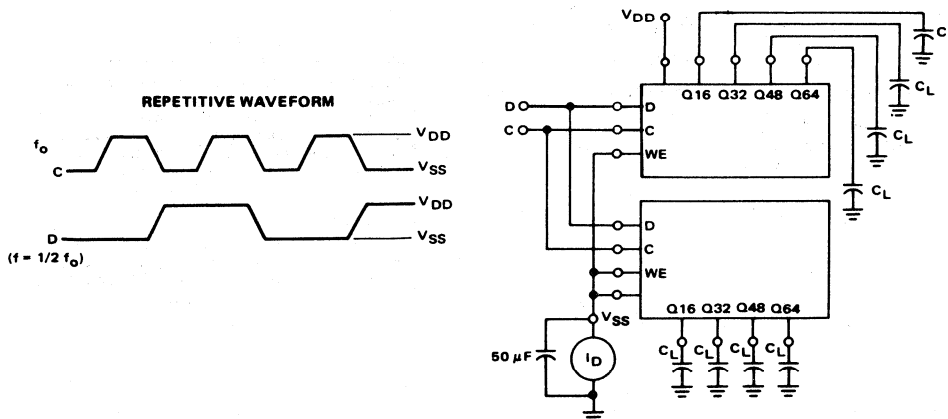
Characteristic	Symbol	VDD	Min	Typ #	Max	Unit
Output Rise and Fall Time $t_{TLH}, t_{THL} = (1.5 \text{ ns/pF}) C_L + 25 \text{ ns}$ $t_{TLH}, t_{THL} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$ $t_{TLH}, t_{THL} = (0.55 \text{ ns/pF}) C_L + 9.5 \text{ ns}$	t_{TLH}, t_{THL}	5.0 10 15	— — —	100 50 40	200 100 80	ns
Propagation Delay Time $t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 390 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 177 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 115 \text{ ns}$	t_{PLH}, t_{PHL}	5.0 10 15	— — —	475 210 140	770 300 215	ns
Clock Pulse Width	t_{WH}	5.0 10 15	330 125 100	170 75 60	— — —	ns
Clock Pulse Frequency	f_{cl}	5.0 10 15	— — —	3.0 6.7 8.3	1.5 4.0 5.3	MHz
Clock Pulse Rise and Fall Time	t_{TLH}, t_{THL}	5.0 10 15	**See Note			—
Data to Clock Setup Time	t_{su}	5.0 10 15	0 10 15	-40 -15 0	— — —	ns
Data to Clock Hold Time	t_h	5.0 10 15	150 75 35	75 25 10	— — —	ns
Write Enable to Clock Setup Time	t_{su}	5.0 10 15	400 200 110	170 65 50	— — —	ns
Write Enable to Clock Release Time	t_{rel}	5.0 10 15	380 180 100	160 55 40	— — —	ns

* The formulas given are for the typical characteristics only at 25°C .

Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

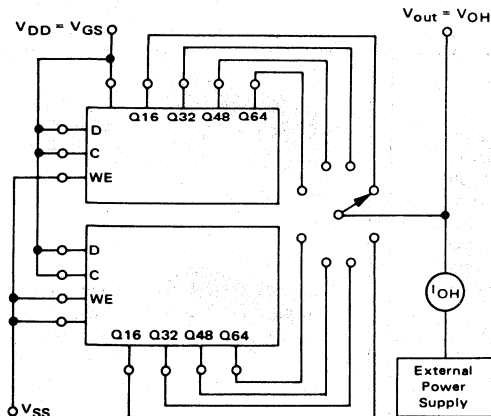
** When shift register sections are cascaded, the maximum rise and fall time of the clock input should be equal to or less than the rise and fall time of the data outputs, driving data inputs, plus the propagation delay of the output driving stage.

FIGURE 1 — POWER DISSIPATION TEST CIRCUIT AND WAVEFORM



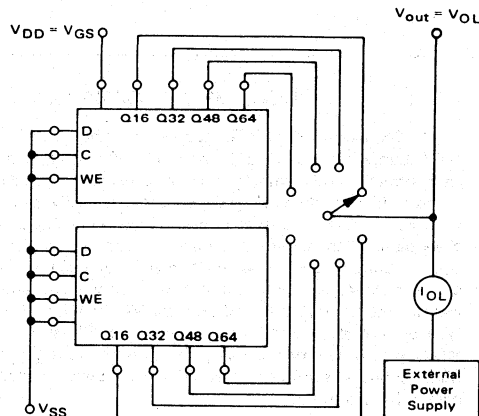
MC14517B

FIGURE 2 – TYPICAL OUTPUT SOURCE CURRENT CHARACTERISTICS TEST CIRCUIT



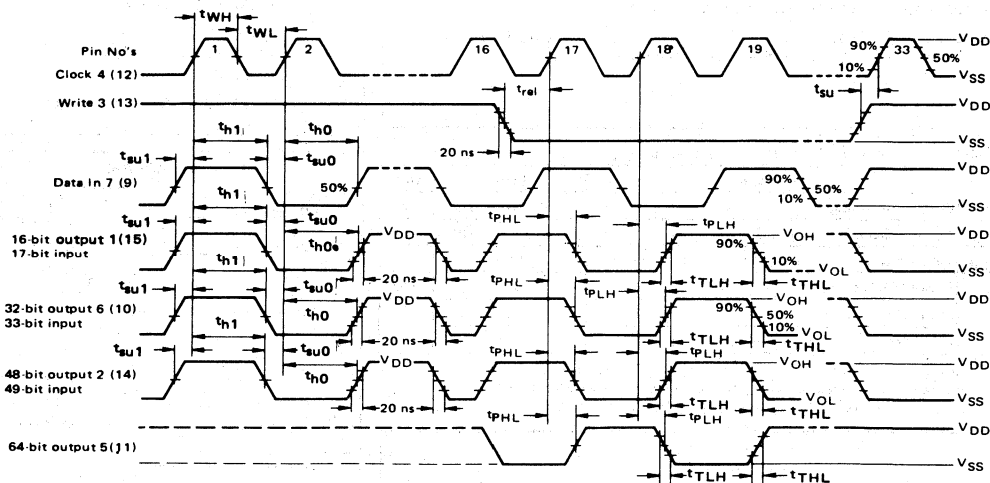
(Output being tested should be in the high-logic state).

FIGURE 3 – TYPICAL OUTPUT SINK CURRENT CHARACTERISTICS TEST CIRCUIT

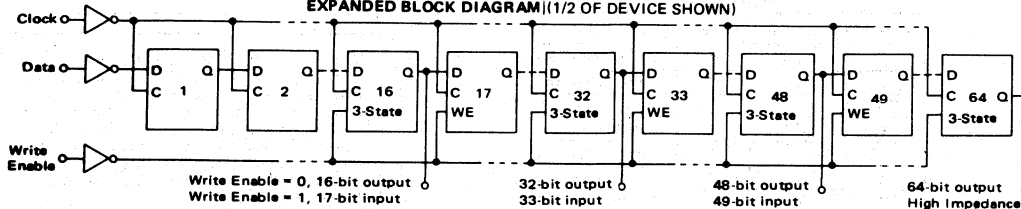


(Output being tested should be in the low-logic state).

FIGURE 4 – AC TEST WAVEFORMS



EXPANDED BLOCK DIAGRAM (1/2 OF DEVICE SHOWN)





MOTOROLA

**MC14518B
MC14520B**

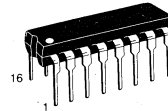
DUAL UP COUNTERS

The MC14518B dual BCD counter and the MC14520B dual binary counter are constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. Each consists of two identical, independent, internally synchronous 4-stage counters. The counter stages are type D flip-flops, with interchangeable Clock and Enable lines for incrementing on either the positive-going or negative-going transition as required when cascading multiple stages. The counter stages can be cleared by applying a high level on the Reset line. In addition, the MC14518B will count out of all undefined states within two clock periods. These complementary MOS up counters find primary use in multi-stage synchronous or ripple counting applications requiring low power dissipation and/or high noise immunity.

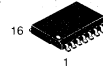
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Internally Synchronous for High Internal and External Speeds
- Logic Edge-Clocked Design – Incremented on Positive Transition of Clock or Negative Transition on Enable
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range



L SUFFIX
CERAMIC
CASE 620



P SUFFIX
PLASTIC
CASE 648



DW SUFFIX
SOIC
CASE 751G

ORDERING INFORMATION

MC14XXXBCP Plastic
MC14XXXBCL Ceramic
MC14XXXBDW SOIC

T_A = -55° to 125°C for all packages.

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V _{DD}	DC Supply Voltage	-0.5 to +18.0	V
V _{in} , V _{out}	Input or Output Voltage (DC or Transient)	-0.5 to V _{DD} + 0.5	V
I _{in} , I _{out}	Input or Output Current (DC or Transient), per Pin	± 10	mA
P _D	Power Dissipation, per Package†	500	mW
T _{stg}	Storage Temperature	-65 to +150	°C
T _L	Lead Temperature (8-Second Soldering)	260	°C

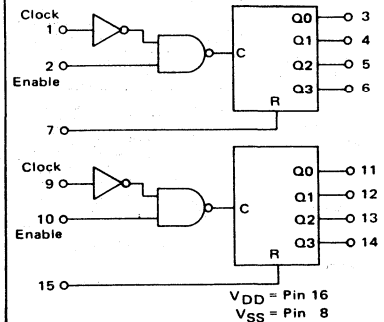
*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P and D/DW" Packages: -7.0 mW/°C From 65°C To 125°C
Ceramic "L" Packages: -12 mW/°C From 100°C To 125°C

TRUTH TABLE

CLOCK	ENABLE	RESET	ACTION
	1	0	Increment Counter
0	1	0	Increment Counter
	X	0	No Change
X		0	No Change
	0	0	No Change
1		0	No Change
X	X	1	Q0 thru Q3 = 0

X = Don't Care

BLOCK DIAGRAM



This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range V_{SS} ≤ (V_{in} or V_{out}) ≤ V_{DD}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

MC14518B•MC14520B

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V _{DD} Vdc	-55°C		25°C			125°C		Unit	
			Min	Max	Min	Typ #	Max	Min	Max		
Output Voltage V _{in} = V _{DD} or 0	V _{OL}	5.0	—	0.05	—	0	0.05	—	0.05	Vdc	
		10	—	0.05	—	0	0.05	—	0.05		
15		—	0.05	—	0	0.05	—	0.05			
V _{in} = 0 or V _{DD}	V _{OH}	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc	
		10	9.95	—	9.95	10	—	9.95	—		
		15	14.95	—	14.95	15	—	14.95	—		
Input Voltage (V _O = 4.5 or 0.5 Vdc) (V _O = 9.0 or 1.0 Vdc) (V _O = 13.5 or 1.5 Vdc)	V _{IL}	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc	
		10	—	3.0	—	4.50	3.0	—	3.0		
15		—	4.0	—	6.75	4.0	—	4.0			
(V _O = 0.5 or 4.5 Vdc) (V _O = 1.0 or 9.0 Vdc) (V _O = 1.5 or 13.5 Vdc)	V _{IH}	5.0	3.5	—	3.5	2.75	—	3.5	—	Vdc	
		10	7.0	—	7.0	5.50	—	7.0	—		
		15	11	—	11	8.25	—	11	—		
Output Drive Current (V _{OH} = 2.5 Vdc) (V _{OH} = 4.6 Vdc) (V _{OH} = 9.5 Vdc) (V _{OH} = 13.5 Vdc)	Source	I _{OH}	5.0	-3.0	—	-2.4	-4.2	—	-1.7	—	mA _{dc}
			5.0	-0.64	—	-0.51	-0.88	—	-0.36	—	
			10	-1.6	—	-1.3	-2.25	—	-0.9	—	
			15	-4.2	—	-3.4	-8.8	—	-2.4	—	
	Sink	I _{OL}	5.0	0.64	—	0.51	0.88	—	0.36	—	mA _{dc}
			10	1.6	—	1.3	2.25	—	0.9	—	
15	4.2	—	3.4	8.8	—	2.4	—				
Input Current	I _{in}	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	μA _{dc}	
Input Capacitance (V _{in} = 0)	C _{in}	—	—	—	—	5.0	7.5	—	—	pF	
Quiescent Current (Per Package)	I _{DD}	5.0	—	5.0	—	0.005	5.0	—	150	μA _{dc}	
		10	—	10	—	0.010	10	—	300		
		15	—	20	—	0.015	20	—	600		
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C _L = 50 pF on all outputs, all buffers switching)	I _T	5.0	I _T = (0.6 μA/kHz) f + I _{DD}						μA _{dc}		
		10	I _T = (1.2 μA/kHz) f + I _{DD}								
		15	I _T = (1.7 μA/kHz) f + I _{DD}								

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

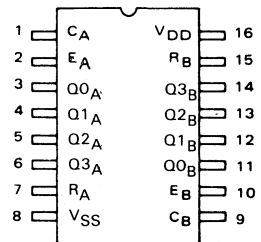
**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) V/k$$

where: I_T is in μA (per package), C_L in pF, V = (V_{DD} - V_{SS}) in volts, f in kHz is input frequency, and k = 0.002.

PIN ASSIGNMENT



MC14518B•MC14520B

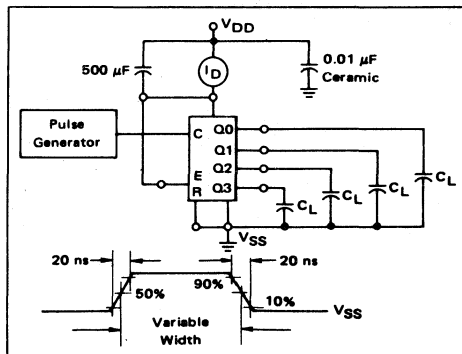
SWITCHING CHARACTERISTICS* ($C_L = 50 \text{ pF}$, $T_A = 25^\circ\text{C}$)

Characteristic	Symbol	V_{DD}	All Types			Unit
			Min	Typ #	Max	
Output Rise and Fall Time $t_{TLH}, t_{THL} = (1.5 \text{ ns/pF}) C_L + 25 \text{ ns}$ $t_{TLH}, t_{THL} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$ $t_{TLH}, t_{THL} = (0.55 \text{ ns/pF}) C_L + 9.5 \text{ ns}$	t_{TLH}, t_{THL}	5.0	—	100	200	ns
		10	—	50	100	
		15	—	40	80	
Propagation Delay Time Clock to Q/Enable to Q $t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 215 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 97 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 75 \text{ ns}$ Reset to Q $t_{PHL} = (1.7 \text{ ns/pF}) C_L + 265 \text{ ns}$ $t_{PHL} = (0.66 \text{ ns/pF}) C_L + 117 \text{ ns}$ $t_{PHL} = (0.66 \text{ ns/pF}) C_L + 95 \text{ ns}$	t_{PLH}, t_{PHL}	5.0	—	280	560	ns
		10	—	115	230	
		15	—	80	160	
	t_{PHL}	5.0	—	330	650	ns
		10	—	130	230	
		15	—	90	170	
Clock Pulse Width	$t_{w(H)}, t_{w(L)}$	5.0	200	100	—	ns
		10	100	50	—	
		15	70	35	—	
Clock Pulse Frequency	f_{cl}	5.0	—	2.5	1.5	MHz
		10	—	6.0	3.0	
		15	—	8.0	4.0	
Clock or Enable Rise and Fall Time	t_{THL}, t_{TLH}	5.0	—	—	15	μs
		10	—	—	5	
		15	—	—	4	
Enable Pulse Width	$t_{WH(E)}$	5.0	440	220	—	ns
		10	200	100	—	
		15	140	70	—	
Reset Pulse Width	$t_{WH(R)}$	5.0	280	125	—	ns
		10	120	55	—	
		15	90	40	—	
Reset Removal Time	t_{rem}	5.0	-5	-45	—	ns
		10	15	-15	—	
		15	20	-5	—	

*The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**FIGURE 1 – POWER DISSIPATION TEST
CIRCUIT AND WAVEFORM**



MC14518B•MC14520B

FIGURE 2 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

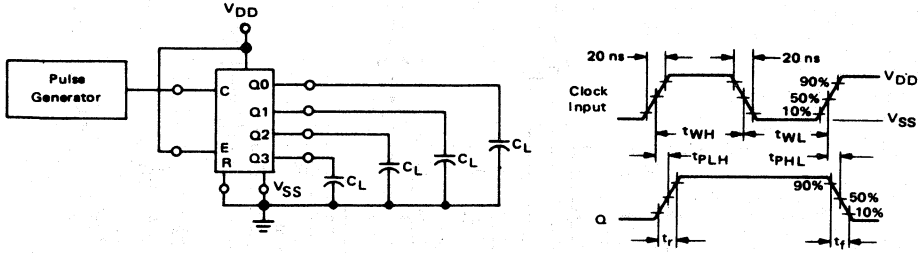
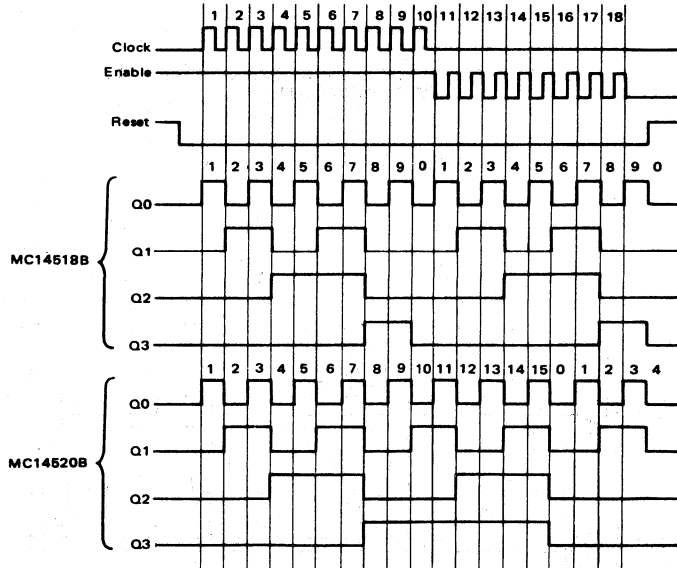


FIGURE 3 – TIMING DIAGRAM



MC14518B•MC14520B

FIGURE 4 – DECADE COUNTER (MC14518B) LOGIC DIAGRAM
(1/2 OF DEVICE SHOWN)

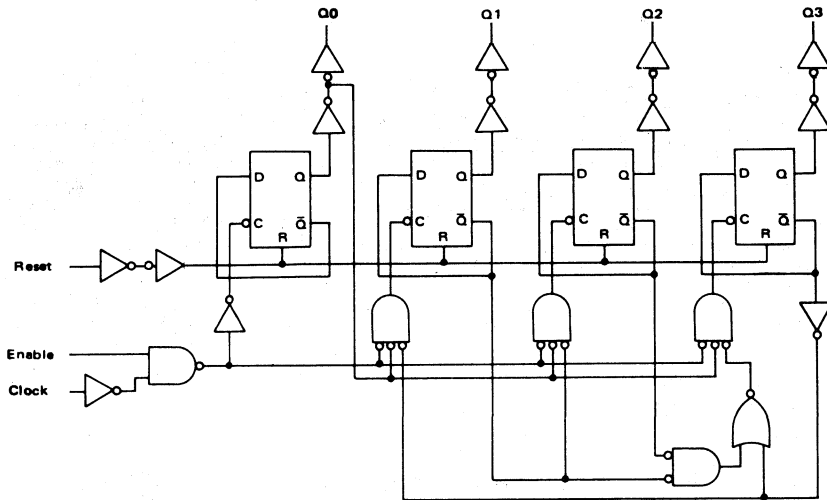
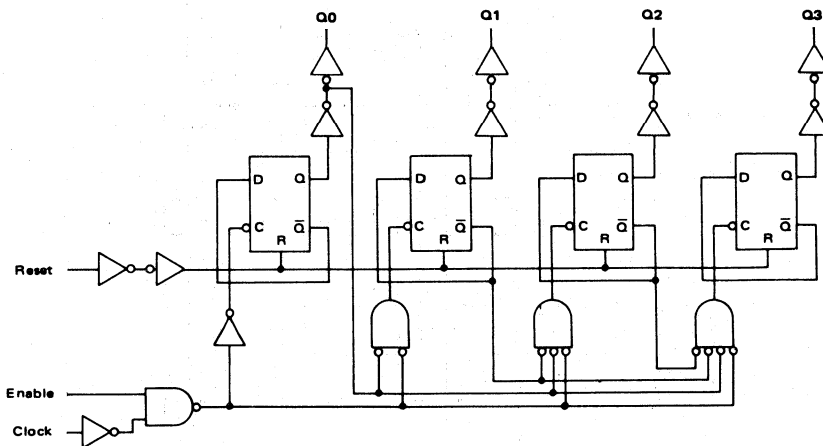


FIGURE 5 – BINARY COUNTER (MC14520B) LOGIC DIAGRAM
(1/2 OF DEVICE SHOWN)





MOTOROLA

MC14519B

**4-BIT AND/OR SELECTOR
or
QUAD 2-CHANNEL DATA SELECTOR
or
QUAD EXCLUSIVE "NOR" GATE**

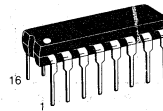
The MC14519B is constructed with MOS P-channel and N-channel enhancement mode devices in a monolithic structure. These complementary MOS logic gates find primary use where low power dissipation and/or high noise immunity is desired.

This device provides three functions in one package; a 4-Bit AND/OR Selector, a Quad 2-Channel Data Selector, or a Quad Exclusive NOR Gate.

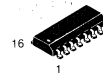
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range
- Plug-In Replacement for CD4019 in Most Applications



**L SUFFIX
CERAMIC
CASE 620**



**P SUFFIX
PLASTIC
CASE 648**



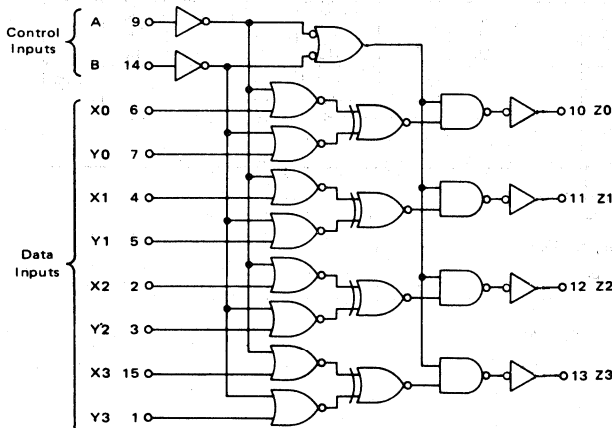
**D SUFFIX
SOIC
CASE 751B**

ORDERING INFORMATION

MC14XXXBCP Plastic
MC14XXXBCL Ceramic
MC14XXXBD SOIC

T_A = -55° to 125°C for all packages.

LOGIC DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

TRUTH TABLE

CONTROL INPUTS		OUTPUT
A	B	Z _n
0	0	0
0	1	Y _n
1	0	X _n
1	1	X _n ⊕ Y _n

Note:

X_n ⊕ Y_n means X_n (Exclusive-NOR) Y_n

MC14519B

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

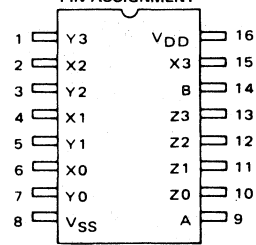
Symbol	Parameter	Value	Unit
V _{DD}	DC Supply Voltage	-0.5 to +18.0	V
V _{in} , V _{out}	Input or Output Voltage (DC or Transient)	-0.5 to V _{DD} + 0.5	V
I _{in} , I _{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
P _D	Power Dissipation, per Package†	500	mW
T _{stg}	Storage Temperature	-65 to +150	°C
T _L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.

†Temperature Derating: Plastic "P and D/DW" Packages: -7.0 mW/°C From 65°C To 125°C

Ceramic "L" Packages: -12 mW/°C From 100°C To 125°C

PIN ASSIGNMENT



ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V _{DD} Vdc	-55°C		25°C			125°C		Unit	
			Min	Max	Min	Typ #	Max	Min	Max		
Output Voltage V _{in} = V _{DD} or 0 "0" Level	V _{OL}	5.0	—	0.05	—	0	0.05	—	0.05	Vdc	
		10	—	0.05	—	0	0.05	—	0.05		
		15	—	0.05	—	0	0.05	—	0.05		
V _{in} = 0 or V _{DD} "1" Level	V _{OH}	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc	
		10	9.95	—	9.95	10	—	9.95	—		
		15	14.95	—	14.95	15	—	14.95	—		
Input Voltage (V _O = 4.5 or 0.5 Vdc) (V _O = 9.0 or 1.0 Vdc) (V _O = 13.5 or 1.5 Vdc) "0" Level	V _{IL}	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc	
		10	—	3.0	—	4.50	3.0	—	3.0		
		15	—	4.0	—	6.75	4.0	—	4.0		
	"1" Level	V _{IH}	5.0	3.5	—	3.5	2.75	—	3.5	—	Vdc
			10	7.0	—	7.0	5.50	—	7.0	—	
			15	11	—	11	8.25	—	11	—	
Output Drive Current (V _{OH} = 2.5 Vdc) (V _{OH} = 4.6 Vdc) (V _{OH} = 9.5 Vdc) (V _{OH} = 13.5 Vdc) Source	I _{OH}	5.0	-3.0	—	-2.4	-4.2	—	-1.7	—	mAdc	
		10	-1.6	—	-1.3	-2.25	—	-0.9	—		
		15	-4.2	—	-3.4	-8.8	—	-2.4	—		
	Sink	I _{OL}	5.0	0.64	—	0.51	0.88	—	0.36	—	mAdc
			10	1.6	—	1.3	2.25	—	0.9	—	
			15	4.2	—	3.4	8.8	—	2.4	—	
Input Current	I _{in}	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	μAdc	
Input Capacitance (V _{in} = 0)	C _{in}	—	—	—	—	5.0	7.5	—	—	pF	
Quiescent Current (Per Package)	I _{DD}	5.0	—	5.0	—	0.005	5.0	—	150	μAdc	
		10	—	10	—	0.010	10	—	300		
		15	—	20	—	0.015	20	—	600		
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C _L = 50 pF on all outputs, all buffers switching)	I _T	5.0	I _T = (1.2 μA/kHz) f + I _{DD}						μAdc		
		10	I _T = (2.4 μA/kHz) f + I _{DD}								
		15	I _T = (3.6 μA/kHz) f + I _{DD}								

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) \text{ V/k}$$

where: I_T is in μA (per package), C_L in pF, V = (V_{DD} - V_{SS}) in volts, f in kHz is input frequency, and k = 0.004.

MC14519B

SWITCHING CHARACTERISTICS* ($C_L = 50 \text{ pF}$, $T_A = 25^\circ\text{C}$)

Characteristic	Symbol	V _{DD}	Min	Typ #	Max	Unit
Output Rise and Fall Time $t_{TLH}, t_{THL} = (1.5 \text{ ns/pF}) C_L + 25 \text{ ns}$ $t_{TLH}, t_{THL} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$ $t_{TLH}, t_{THL} = (0.55 \text{ ns/pF}) C_L + 9.5 \text{ ns}$	t_{TLH}, t_{THL}	5.0 10 15	— — —	100 50 40	200 100 80	ns
Propagation Delay Time $t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 165 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 82$ $t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 65 \text{ ns}$	t_{PLH}, t_{PHL}	5.0 10 15	— — —	250 115 90	500 225 165	ns

*The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

FIGURE 1 – DYNAMIC POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

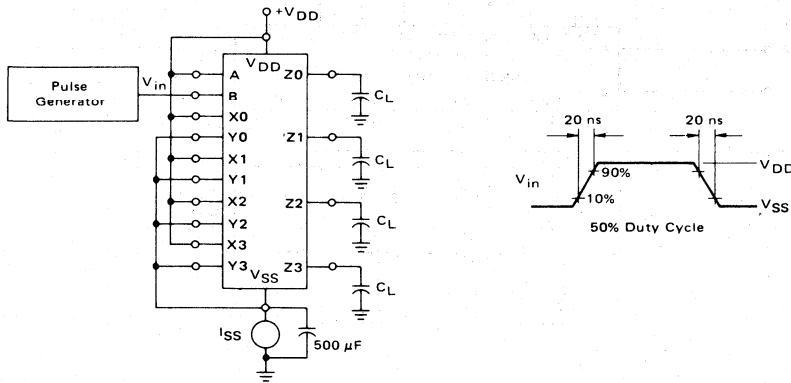
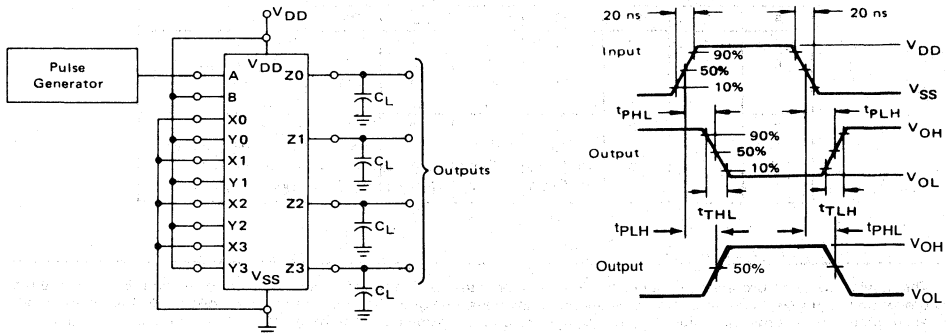


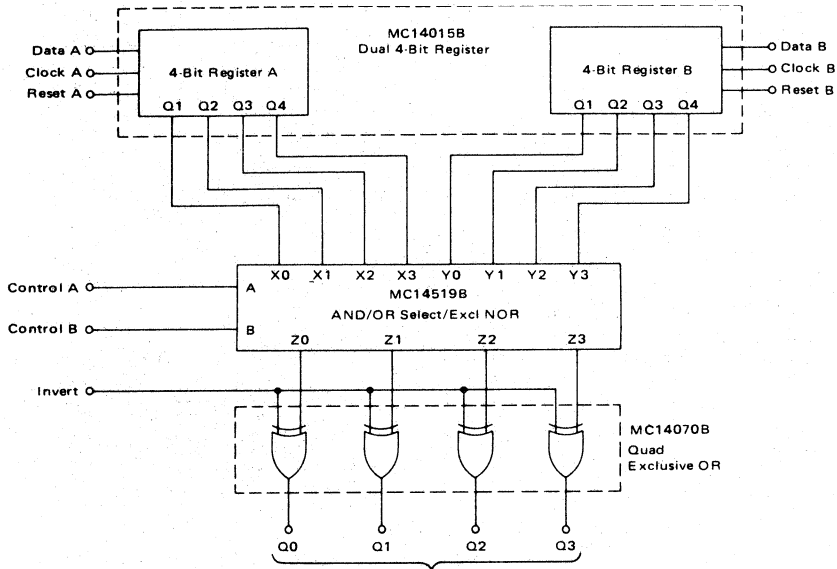
FIGURE 2 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



MC14519B

TYPICAL CIRCUIT APPLICATIONS

DATA REGISTER SELECTION COMPARISON



CONVERSION TABLE

OPERATION CODE			OUTPUT				FUNCTION
A	B	INV	Q0	Q1	Q2	Q3	
0	0	0	0	0	0	0	Inhibit, all zeros
0	0	1	1	1	1	1	Inhibit, all ones
1	0	0	X0	X1	X2	X3	Control A
1	0	1	$\bar{X}0$	$\bar{X}1$	$\bar{X}2$	$\bar{X}3$	Control A and Invert
0	1	0	Y0	Y1	Y2	Y3	Control B
0	1	1	$\bar{Y}0$	$\bar{Y}1$	$\bar{Y}2$	$\bar{Y}3$	Control B and Invert
1	1	0	$X0 \oplus Y0$	$X1 \oplus Y1$	$X2 \oplus Y2$	$X3 \oplus Y3$	Exclusive NOR
1	1	1	$X0 \oplus \bar{Y}0$	$X1 \oplus \bar{Y}1$	$X2 \oplus \bar{Y}2$	$X3 \oplus \bar{Y}3$	Exclusive OR

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.



MOTOROLA

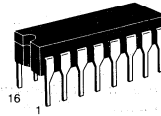
MC14520B
See Page 6-292

MC14521B

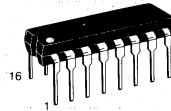
24-STAGE FREQUENCY DIVIDER

The MC14521B consists of a chain of 24 flip-flops with an input circuit that allows three modes of operation. The input will function as a crystal oscillator, an RC oscillator, or as an input buffer for an external oscillator. Each flip-flop divides the frequency of the previous flip-flop by two, consequently this part will count up to $2^{24} = 16,777,216$. The count advances on the negative going edge of the clock. The outputs of the last seven-stages are available for added flexibility.

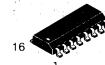
- All Stages are Resettable
- Reset Disables the RC Oscillator for Low Standby Power Drain
- RC and Crystal Oscillator Outputs Are Capable of Driving External Loads
- Test Mode to Reduce Test Time
- V_{DD}' and V_{SS}' Pins Brought Out on Crystal Oscillator Inverter to Allow the Connection of External Resistors for Low-Power Operation
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load over the Rated Temperature Range.



L SUFFIX
CERAMIC
CASE 620



P SUFFIX
PLASTIC
CASE 648



D SUFFIX
SOIC
CASE 751B

ORDERING INFORMATION

MC14XXXBCP Plastic
MC14XXXBCL Ceramic
MC14XXXBD SOIC

$T_A = -55^\circ$ to 125°C for all packages.

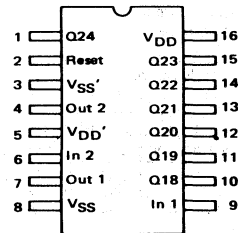
MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	-0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	-0.5 to $V_{DD} + 0.5$	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	± 10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	-65 to +150	$^\circ\text{C}$
T_L	Lead Temperature (8-Second Soldering)	260	$^\circ\text{C}$

*Maximum Ratings are those values beyond which damage to the device may occur.

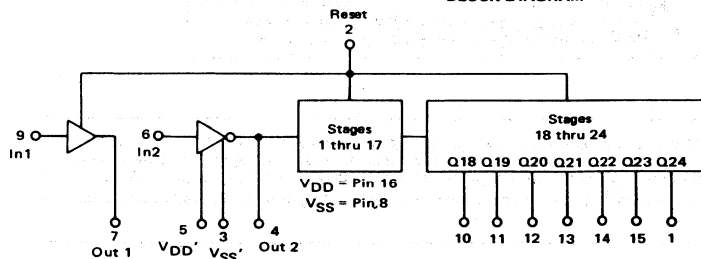
†Temperature Derating: Plastic "P and D/DW" Packages: -7.0 mW/ $^\circ\text{C}$ From 65°C To 125°C
Ceramic "L" Packages: -12 mW/ $^\circ\text{C}$ From 100°C To 125°C

PIN ASSIGNMENT



6

BLOCK DIAGRAM



OUTPUT	COUNT CAPACITY
Q18	$2^{18} = 262,144$
Q19	$2^{19} = 524,288$
Q20	$2^{20} = 1,048,576$
Q21	$2^{21} = 2,097,152$
Q22	$2^{22} = 4,194,304$
Q23	$2^{23} = 8,388,608$
Q24	$2^{24} = 16,777,216$

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

MC14521B

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	VDD Vdc	-55°C		25°C			125°C		Unit	
			Min	Max	Min	Typ #	Max	Min	Max		
Output Voltage V _{in} = VDD or 0 "0" Level	V _{OL}	5.0	—	0.05	—	0	0.05	—	0.05	Vdc	
		10	—	0.05	—	0	0.05	—	0.05		
15		—	0.05	—	0	0.05	—	0.05			
V _{in} = 0 or VDD "1" Level	V _{OH}	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc	
		10	9.95	—	9.95	10	—	9.95	—		
		15	14.95	—	14.95	15	—	14.95	—		
Input Voltage (V _O = 4.5 or 0.5 Vdc) (V _O = 9.0 or 1.0 Vdc) (V _O = 13.5 or 1.5 Vdc) "0" Level	V _{IL}	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc	
		10	—	3.0	—	4.50	3.0	—	3.0		
15		—	4.0	—	6.75	4.0	—	4.0			
(V _O = 0.5 or 4.5 Vdc) (V _O = 1.0 or 9.0 Vdc) (V _O = 1.5 or 13.5 Vdc) "1" Level	V _{IH}	5.0	3.5	—	3.5	2.75	—	3.5	—	Vdc	
		10	7.0	—	7.0	5.50	—	7.0	—		
		15	11	—	11	8.25	—	11	—		
Output Drive Current (V _{OH} = 2.5 Vdc) (V _{OH} = 4.6 Vdc) (V _{OH} = 9.5 Vdc) (V _{OH} = 13.5 Vdc) Source Pins 4 & 7	I _{OH}	5.0	-1.2	—	-1.0	-1.7	—	-0.7	—	mAdc	
		5.0	-0.25	—	0.2	-0.36	—	-0.14	—		
		10	-0.62	—	-0.5	-0.9	—	-0.35	—		
		15	-1.8	—	-1.5	-3.5	—	-1.1	—		
	(V _{OH} = 2.5 Vdc) (V _{OH} = 4.6 Vdc) (V _{OH} = 9.5 Vdc) (V _{OH} = 13.5 Vdc) Source Pins 1, 10, 11, 12, 13, 14 and 15	I _{OH}	5.0	3.0	—	-2.4	-4.2	—	-1.7	—	mAdc
			5.0	-0.64	—	-0.51	-0.88	—	-0.36	—	
			10	-1.6	—	-1.3	-2.25	—	-0.9	—	
			15	-4.2	—	-3.4	-8.8	—	-2.4	—	
	(V _{OL} = 0.4 Vdc) (V _{OL} = 0.5 Vdc) (V _{OL} = 1.5 Vdc) Sink	I _{OL}	5.0	0.64	—	0.51	0.88	—	0.36	—	mAdc
			10	1.6	—	1.3	2.25	—	0.9	—	
			15	4.2	—	3.4	8.8	—	2.4	—	
	Input Current	I _{in}	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	μAdc
Input Capacitance (V _{in} = 0)	C _{in}	—	—	—	—	5.0	7.5	—	—	pF	
Quiescent Current (Per Package)	I _{DD}	5.0	—	5.0	—	0.005	5.0	—	150	μAdc	
		10	—	10	—	0.010	10	—	300		
		15	—	20	—	0.015	20	—	600		
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C _L = 50 pF on all outputs, all buffers switching)	I _T	5.0	I _T = (0.42 μA/kHz) f + I _{DD}							μAdc	
		10	I _T = (0.85 μA/kHz) f + I _{DD}								
		15	I _T = (1.40 μA/kHz) f + I _{DD}								

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) Vfk$$

where: I_T is in μA (per package), C_L in pF, V = (V_{DD} - V_{SS}) in volts, f in kHz is input frequency, and k = 0.003.

MC14521B

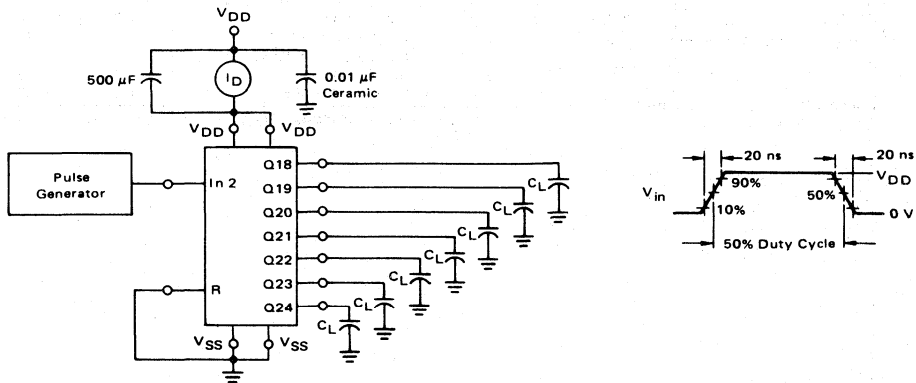
SWITCHING CHARACTERISTICS* ($C_L = 50 \text{ pF}$, $T_A = 25^\circ\text{C}$)

Characteristic	Symbol	VDD Vdc	Min	Typ #	Max	Unit
Output Rise and Fall Time (Counter Outputs) $t_{TLH}, t_{THL} = (1.5 \text{ ns/pF}) C_L + 25 \text{ ns}$ $t_{TLH}, t_{THL} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$ $t_{TLH}, t_{THL} = (0.55 \text{ ns/pF}) C_L + 12.5 \text{ ns}$	t_{TLH}, t_{THL}	5.0 10 15	— — —	100 50 40	200 100 80	ns
Propagation Delay Time Clock to Q18 $t_{PHL}, t_{PLH} = (1.7 \text{ ns/pF}) C_L + 4415 \text{ ns}$ $t_{PHL}, t_{PLH} = (0.66 \text{ ns/pF}) C_L + 1667 \text{ ns}$ $t_{PHL}, t_{PLH} = (0.5 \text{ ns/pF}) C_L + 1275 \text{ ns}$ Clock to Q24 $t_{PHL}, t_{PLH} = (1.7 \text{ ns/pF}) C_L + 5915 \text{ ns}$ $t_{PHL}, t_{PLH} = (0.66 \text{ ns/pF}) C_L + 2167 \text{ ns}$ $t_{PHL}, t_{PLH} = (0.5 \text{ ns/pF}) C_L + 1675 \text{ ns}$	t_{PHL}, t_{PLH}	5.0 10 15	— — —	4.5 1.7 1.3	9.0 3.5 2.7	μs
Propagation Delay Time Reset to Q_n $t_{PHL} = (1.7 \text{ ns/pF}) C_L + 1215 \text{ ns}$ $t_{PHL} = (0.66 \text{ ns/pF}) C_L + 467 \text{ ns}$ $t_{PHL} = (0.5 \text{ ns/pF}) C_L + 350 \text{ ns}$	t_{PHL}	5.0 10 15	— — —	1300 500 375	2600 1000 750	ns
Clock Pulse Width	$t_{WH(c)}$	5.0 10 15	385 150 120	140 55 40	— — —	ns
Clock Pulse Frequency	f_{cl}	5.0 10 15	— — —	3.5 9.0 12	2.0 5.0 6.5	MHz
Clock Rise and Fall Time	t_{TLH}, t_{THL}	5.0 10 15	— — —	— — —	15 5.0 4.0	μs
Reset Pulse Width	$t_{WH(R)}$	5.0 10 15	1400 600 450	700 300 225	— — —	ns
Reset Removal Time	t_{rem}	5.0 10 15	30 0 -40	-200 -160 -110	— — —	ns

*The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

FIGURE 1 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM



MC14521B

FIGURE 2 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

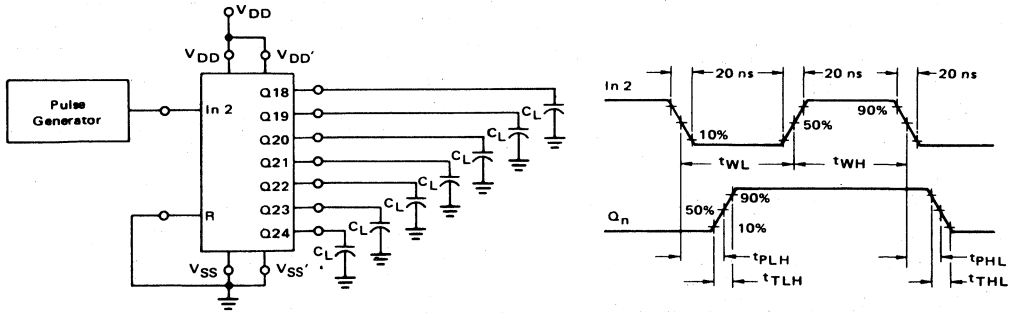
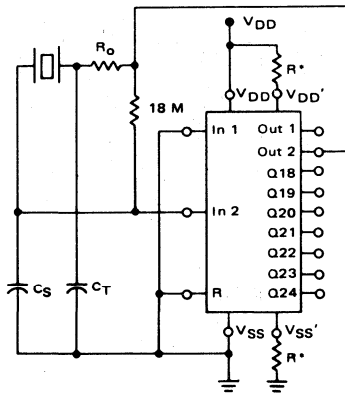


FIGURE 3 – CRYSTAL OSCILLATOR CIRCUIT



* Optional for low power operation.
 $10 \text{ k}\Omega < R < 70 \text{ k}\Omega$

FIGURE 4 – TYPICAL DATA FOR CRYSTAL OSCILLATOR CIRCUIT

CHARACTERISTIC	500 kHz CIRCUIT	50 kHz CIRCUIT	UNIT
Crystal Characteristics			
Resonant Frequency	500	50	k Hz
Equivalent Resistance, R_S	1.0	6.2	k Ω
External Resistor/Capacitor Values			
R_o	47	750	k Ω
C_T	82	82	pF
C_S	20	20	pF
Frequency Stability			
Frequency Change as a Function of V_{DD} ($T_A = 25^\circ\text{C}$)			
V_{DD} Change from 5.0 V to 10 V	+6.0	+2.0	ppm
V_{DD} Change from 10 V to 15 V	+2.0	+2.0	ppm
Frequency Change as a Function of Temperature ($V_{DD} = 10 \text{ V}$)			
T_A Change from -55°C to $+25^\circ\text{C}$			
MC14521 only	-4.0	-2.0	ppm
Complete Oscillator*	+100	+120	ppm
T_A Change from $+25^\circ\text{C}$ to $+125^\circ\text{C}$			
MC14521 only	-2.0	-2.0	ppm
Complete Oscillator*	-160	-560	ppm

* Complete oscillator includes crystal, capacitors, and resistors.

MC14521B

FIGURE 5 – RC OSCILLATOR STABILITY

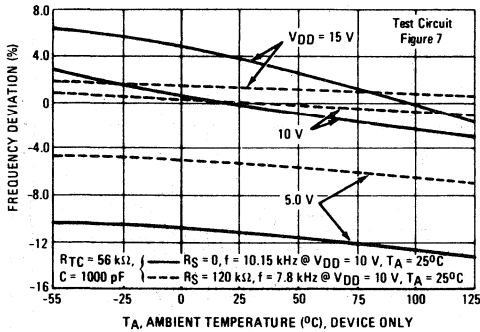


FIGURE 6 – RC OSCILLATOR FREQUENCY AS A FUNCTION OF R_{TC} AND C

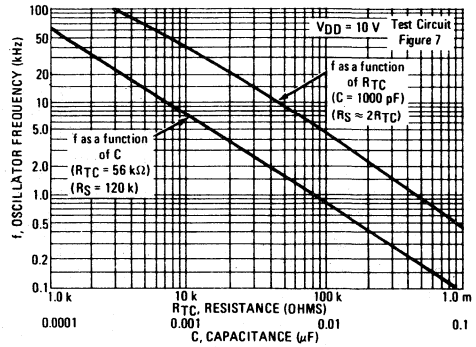


FIGURE 7 – RC OSCILLATOR CIRCUIT

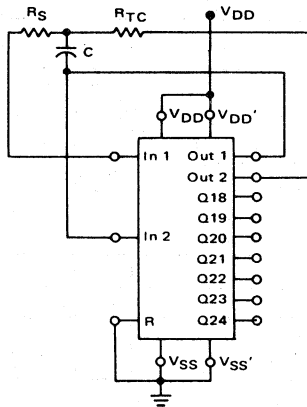
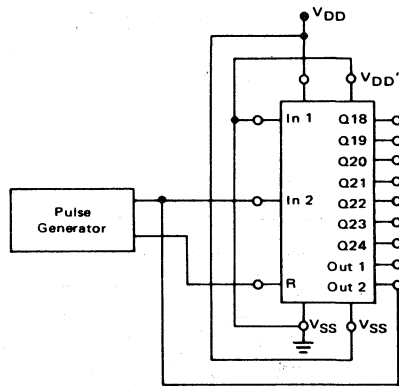


FIGURE 8 – FUNCTIONAL TEST CIRCUIT

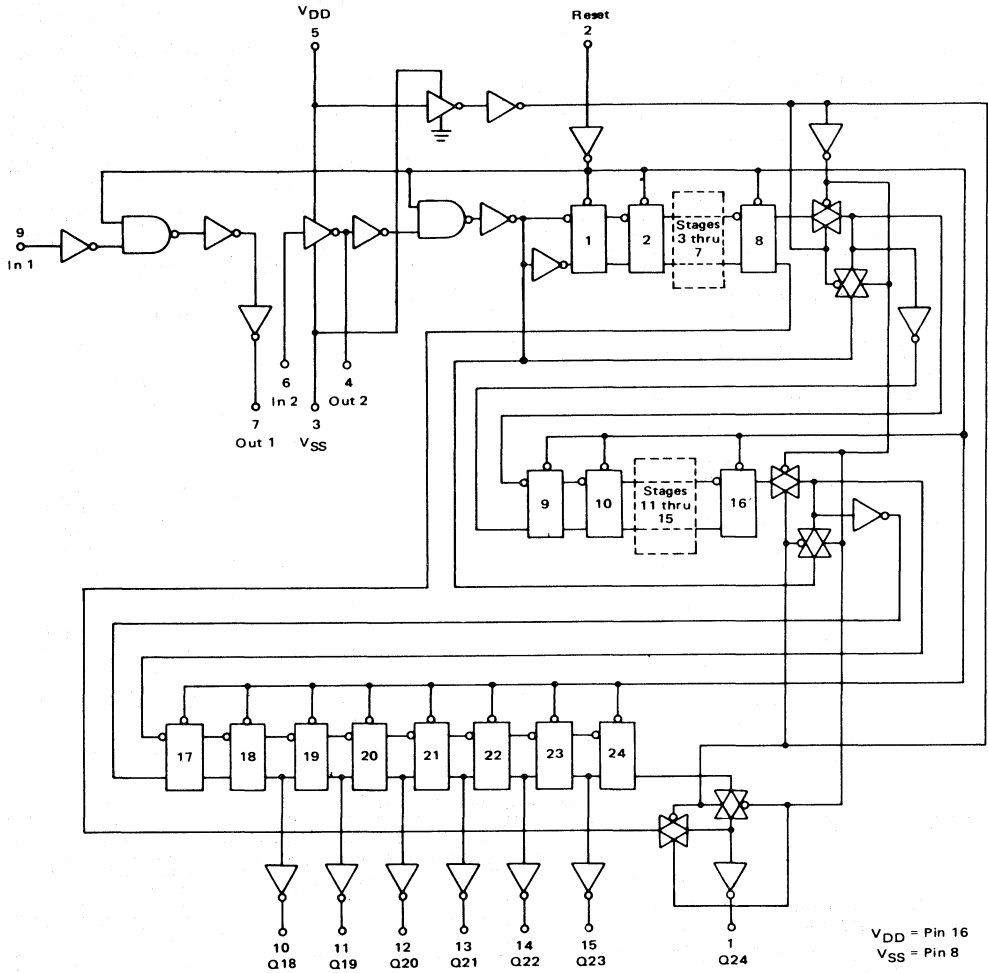


FUNCTIONAL TEST SEQUENCE

	INPUTS			OUTPUTS		COMMENTS		
	Reset	In 2	Out 2	VSS'	VDD'			
<p>A test function (see Figure 8) has been included for the reduction of test time required to exercise all 24 counter stages. This test function divides the counter into three 8-stage sections in parallel. All flip-flops are now at a logic "1". The counter is now returned to the normal 24-stages in series configuration. One more pulse is entered into Input 2 (In 2) which will cause the counter to ripple from an all "1" state to an all "0" state.</p>	1	0	0	VDD	Gnd	0	Counter is in three 8-stage sections in parallel mode. Counter is reset. In 2 and Out 2 are connected together.	
	0	1	1	1	VDD	Gnd	1	First "0" to "1" transition on In 2, Out 2 node.
		0	0	0				255 "0" to "1" transitions are clocked into this In 2, Out 2 node.
		1	1	1				
		0	0	0				
		1	1	1				
	0	0	0	Gnd	VDD	1	The 255th "0" to "1" transition.	
	0	0	0	Gnd	VDD	1	1	Counter converted back to 24-stages in series mode.
	1	1	0	Gnd	VDD	1	1	Out 2 converts back to an output.
	1	1	0	Gnd	VDD	1	1	Counter ripples from an all "1" state to an all "0" stage.
0	0	1	Gnd	VDD	0	0		

MC14521B

LOGIC DIAGRAM



6



MOTOROLA

PRESETTABLE 4-BIT DOWN COUNTERS

The MC14522B BCD counter and the MC14526B binary counter are constructed with MOS P-channel and N-channel enhancement mode devices in a monolithic structure.

These devices are presettable, cascadable, synchronous down counters with a decoded "0" state output for divide-by-N applications. In single stage applications the "0" output is applied to the Preset Enable input. The Cascade Feedback input allows cascade divide-by-N operation with no additional gates required. The Inhibit input allows disabling of the pulse counting function. Inhibit may also be used as a negative edge clock.

These complementary MOS counters can be used in frequency synthesizers, phase-locked loops, and other frequency division applications requiring low power dissipation and/or high noise immunity.

- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Logic Edge-Clocked Design — Incremented on Positive Transition of Clock or Negative Transition of Inhibit
- Asynchronous Preset Enable
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V _{DD}	DC Supply Voltage	-0.5 to +18.0	V
V _{in} , V _{out}	Input or Output Voltage (DC or Transient)	-0.5 to V _{DD} + 0.5	V
I _{in} , I _{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
P _D	Power Dissipation, per Package†	500	mW
T _{stg}	Storage Temperature	-65 to +150	°C
T _L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
 †Temperature Derating: Plastic "P and D/DW" Packages: -7.0 mW/°C From 65°C To 125°C
 Ceramic "L" Packages: -12 mW/°C From 100°C To 125°C

FUNCTION TABLE

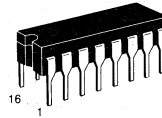
Inputs					Output	Resulting Function
Clock	Reset	Inhibit	Preset Enable	Cascade Feedback	"0"	
X	H	X	L	L	L	Asynchronous reset*
X	H	X	H	L	H	Asynchronous reset
X	H	X	X	H	H	Asynchronous reset
X	L	X	H	X	L	Asynchronous preset
	L		L	X	L	Decrement inhibited
	L		L	X	L	Decrement inhibited
	L		L	L	L	No change** (inactive edge)
	L		L	L	L	No change** (inactive edge)
	L		L	L	L	Decrement**
	L		L	L	L	Decrement**

X = Don't Care

Notes:

- * Output "0" is low when reset goes high only if PE and CF are low.
- ** Output "0" is high when reset is low, only if CF is high and count is 0000.

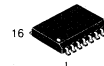
MC14522B
MC14526B



L SUFFIX
CERAMIC
CASE 620



P SUFFIX
PLASTIC
CASE 648



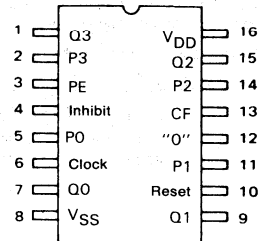
DW SUFFIX
SOIC
CASE 751G

ORDERING INFORMATION

MC14XXXBCP Plastic
 MC14XXXBCL Ceramic
 MC14XXXBDW SOIC

T_A = -55° to 125°C for all packages.

PIN ASSIGNMENT



This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range V_{SS} ≤ (V_{in} or V_{out}) ≤ V_{DD}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

6

MC14522B•MC14526B

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V _{DD} Vdc	-55°C		25°C			125°C		Unit
			Min	Max	Min	Typ #	Max	Min	Max	
Output Voltage V _{in} = V _{DD} or 0	"0" Level V _{OL}	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
		10	—	0.05	—	0	0.05	—	0.05	
V _{in} = 0 or V _{DD}	"1" Level V _{OH}	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc
		10	9.95	—	9.95	10	—	9.95	—	
Input Voltage (V _O = 4.5 or 0.5 Vdc) (V _O = 9.0 or 1.0 Vdc) (V _O = 13.5 or 1.5 Vdc)	"0" Level V _{IL}	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc
		10	—	3.0	—	4.50	3.0	—	3.0	
(V _O = 0.5 or 4.5 Vdc) (V _O = 1.0 or 9.0 Vdc) (V _O = 1.5 or 13.5 Vdc)	"1" Level V _{IH}	5.0	3.5	—	3.5	2.75	—	3.5	—	Vdc
		10	7.0	—	7.0	5.50	—	7.0	—	
Output Drive Current (V _{OH} = 2.5 Vdc) (V _{OH} = 4.6 Vdc) (V _{OH} = 9.5 Vdc) (V _{OH} = 13.5 Vdc)	Source I _{OH}	5.0	-3.0	—	-2.4	-4.2	—	-1.7	—	mAdc
		5.0	-0.64	—	-0.51	-0.88	—	-0.36	—	
(V _{OL} = 0.4 Vdc) (V _{OL} = 0.5 Vdc) (V _{OL} = 1.5 Vdc)	Sink I _{OL}	5.0	0.64	—	0.51	0.88	—	0.36	—	mAdc
		10	1.6	—	1.3	2.25	—	0.9	—	
		15	4.2	—	3.4	8.8	—	2.4	—	
Input Current	I _{in}	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	μAdc
Input Capacitance (V _{in} = 0)	C _{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)	I _{DD}	5.0	—	5.0	—	0.005	5.0	—	150	μAdc
		10	—	10	—	0.010	10	—	300	
		15	—	20	—	0.015	20	—	600	
Total Supply Current**†† (Dynamic plus Quiescent, Per Package) (C _L = 50 pF on all outputs, all buffers switching)	I _T	5.0	I _T = (1.7 μA/kHz) f + I _{DD} I _T = (3.4 μA/kHz) f + I _{DD} I _T = (5.1 μA/kHz) f + I _{DD}							μAdc
		10								
		15								

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) Vfk$$

where: I_T is in μA (per package), C_L in pF, V = (V_{DD} - V_{SS}) in volts, f in kHz is input frequency, and k = 0.001.

MC14522B•MC14526B

SWITCHING CHARACTERISTICS* ($C_L = 50$ pF, $T_A = 25^\circ\text{C}$)

Characteristic	Symbol	V _{DD}	Min	Typ #	Max	Unit
Output Rise and Fall Time $t_{TLH}, t_{THL} = (1.5 \text{ ns/pF}) C_L + 25 \text{ ns}$ $t_{TLH}, t_{THL} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$ $t_{TLH}, t_{THL} = (0.55 \text{ ns/pF}) C_L + 9.5 \text{ ns}$	$t_{TLH},$ t_{THL} (Figures 4, 5)	5.0 10 15	— — —	100 50 40	200 100 80	ns
Propagation Delay Time (Inhibit Used as Negative-Edge Clock) Clock or Inhibit to Q $t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 465 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 197 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 135 \text{ ns}$ Clock or Inhibit to "0" $t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 155 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 87 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 65 \text{ ns}$	$t_{PLH},$ t_{PHL} (Figures 4, 5, 6)	5.0 10 15 5.0 10 15	— — — — — —	550 225 160 240 130 100	1100 450 320 480 260 200	ns
Propagation Delay Time Pn to Q	$t_{PLH},$ t_{PHL} (Figures 4, 7)	5.0 10 15	— — —	260 120 100	520 240 200	ns
Propagation Delay Time Reset to Q	t_{PHL} (Figure 8)	5.0 10 15	— — —	250 110 80	500 220 160	ns
Propagation Delay Time Preset Enable to "0"	$t_{PHL},$ t_{PLH} (Figures 4, 9)	5.0 10 15	— — —	220 100 80	440 200 160	ns
Clock or Inhibit Pulse Width	t_w (Figures 5, 6)	5.0 10 15	250 100 80	125 50 40	— — —	ns
Clock Pulse Frequency (with PE = low)	f_{max} (Figures 4, 5, 6)	5.0 10 15	— — —	2.0 5.0 6.6	1.5 3.0 4.0	MHz
Clock or Inhibit Rise and Fall Time	$t_r,$ t_f (Figures 5, 6)	5.0 10 15	— — —	— — —	15 5 4	μs
Setup Time Pn to Preset Enable	t_{su} (Figure 10)	5.0 10 15	90 50 40	40 15 10	— — —	ns
Hold Time Preset Enable to Pn	t_h (Figure 10)	5.0 10 15	30 30 30	-15 -5 0	— — —	ns
Preset Enable Pulse Width	t_w (Figure 10)	5.0 10 15	250 100 80	125 50 40	— — —	ns
Reset Pulse Width	t_w (Figure 8)	5.0 10 15	350 250 200	175 125 100	— — —	ns
Reset Removal Time	t_{rem} (Figure 8)	5.0 10 15	10 20 30	-110 -30 -20	— — —	ns

*The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

MC14522B•MC14526B

FIGURE 1 – TYPICAL OUTPUT SOURCE CHARACTERISTICS TEST CIRCUIT

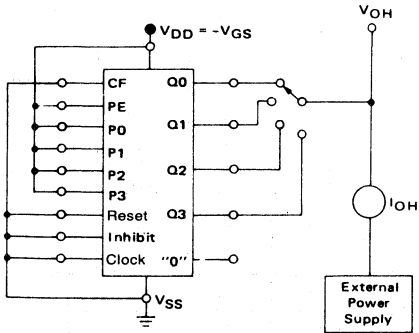


FIGURE 2 – TYPICAL OUTPUT SINK CHARACTERISTICS TEST CIRCUIT

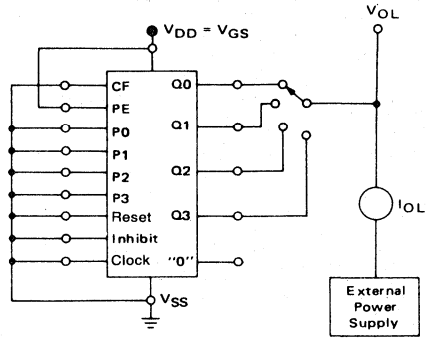


FIGURE 3 – POWER DISSIPATION

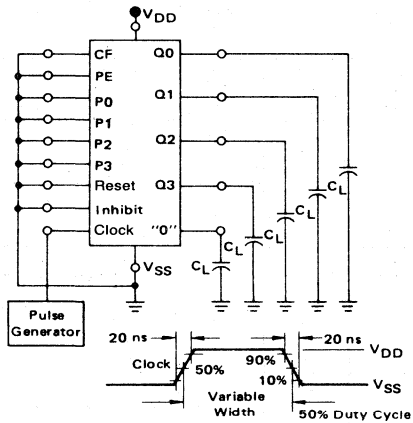
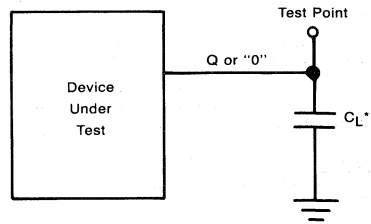


FIGURE 4 – TEST CIRCUIT



*Includes all probe and jig capacitance.

MC14522B•MC14526B

SWITCHING WAVEFORMS

FIGURE 5

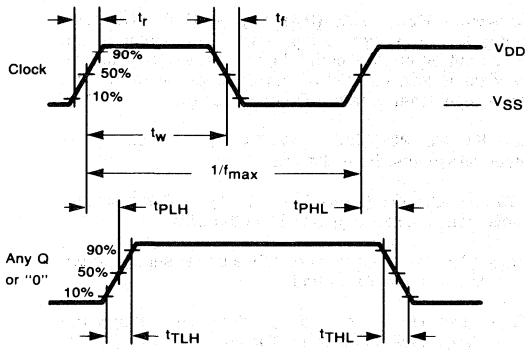


FIGURE 6

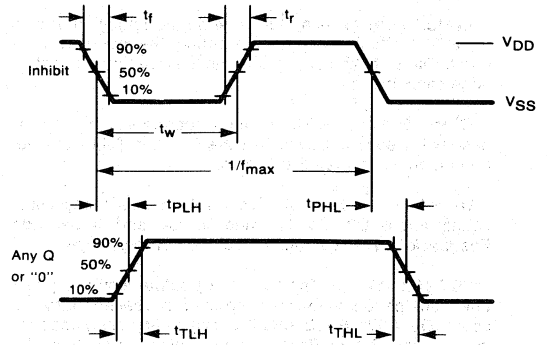


FIGURE 7

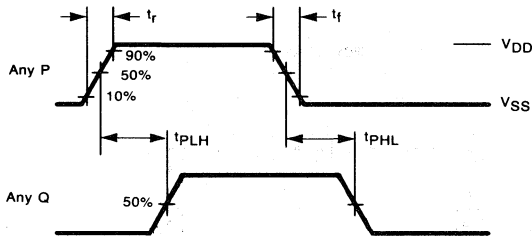


FIGURE 8

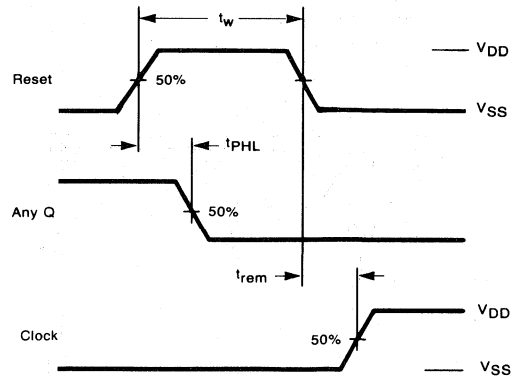


FIGURE 9

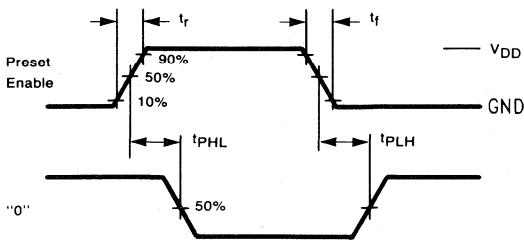
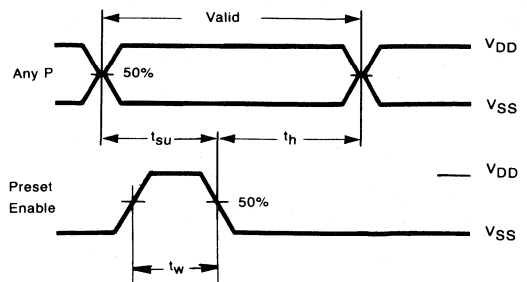


FIGURE 10



MC14522B•MC14526B

PIN DESCRIPTIONS

Preset Enable (Pin 3) — If Reset is low, a high level on the Preset Enable input asynchronously loads the counter with the programmed values on P0, P1, P2, and P3.

Inhibit (Pin 4) — A high level on the Inhibit input prevents the Clock from decrementing the counter. With Clock (pin 6) held high, Inhibit may be used as a negative edge clock input.

Clock (Pin 6) — The counter decrements by one for each rising edge of Clock. See the Function Table for level requirements on the other inputs.

Reset (Pin 10) — A high level on Reset asynchronously forces Q0, Q1, Q2, and Q3 low and, if Cascade Feedback is high, causes the "0" output to go high.

"0" (Pin 12) — The "0" (Zero) output issues a pulse one clock period wide when the counter reaches terminal count (Q0 = Q1 = Q2 = Q3 = low) if Cascade Feedback is high and Preset Enable is low. When presetting the

counter to a value other than all zeroes, the "0" output is valid after the rising edge of Preset Enable (when Cascade Feedback is high). See the Function Table.

Cascade Feedback (Pin 13) — If the Cascade Feedback input is high, a high level is generated at the "0" output when the count is all zeroes. If Cascade Feedback is low, the "0" output depends on the Preset Enable input level. See the Function Table.

P0, P1, P2, P3 (Pins 5, 11, 14, 2) — These are the preset data inputs. P0 is the LSB.

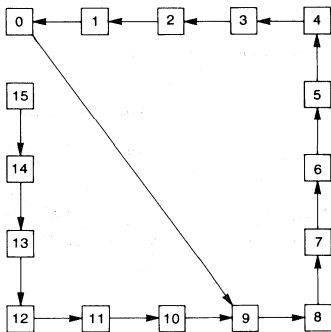
Q0, Q1, Q2, Q3 (Pins 7, 9, 15, 1) — These are the synchronous counter outputs. Q0 is the LSB.

VSS (Pin 8) — The most negative power supply potential. This pin is usually ground.

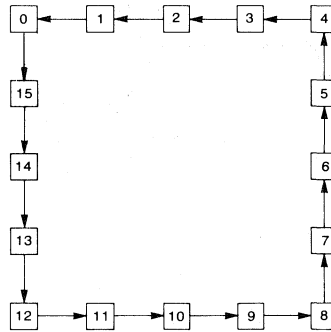
VDD (Pin 16) — The most positive power supply potential. VDD may range from 3 to 18 V with respect to VSS.

STATE DIAGRAMS

MC14522B



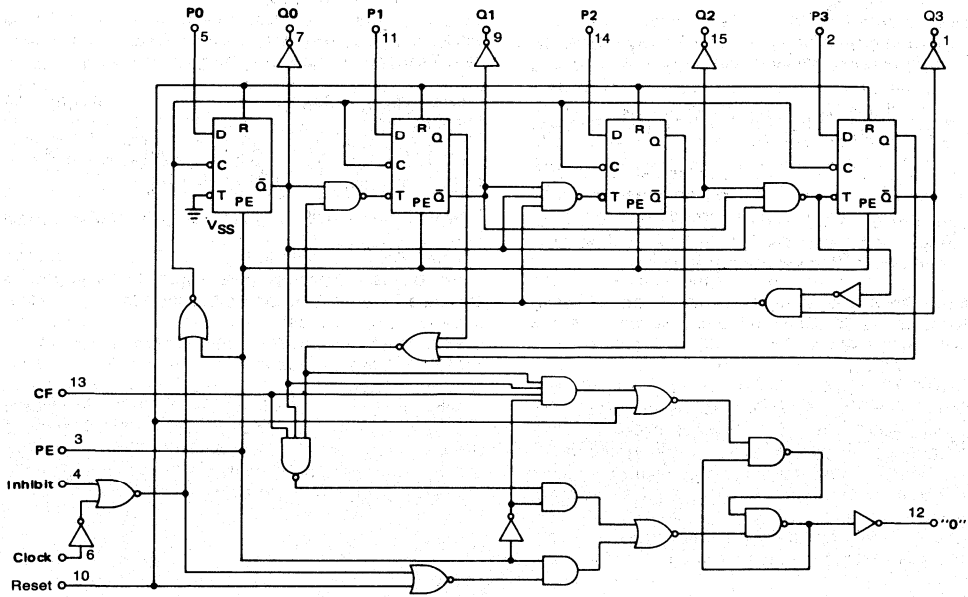
MC14526B



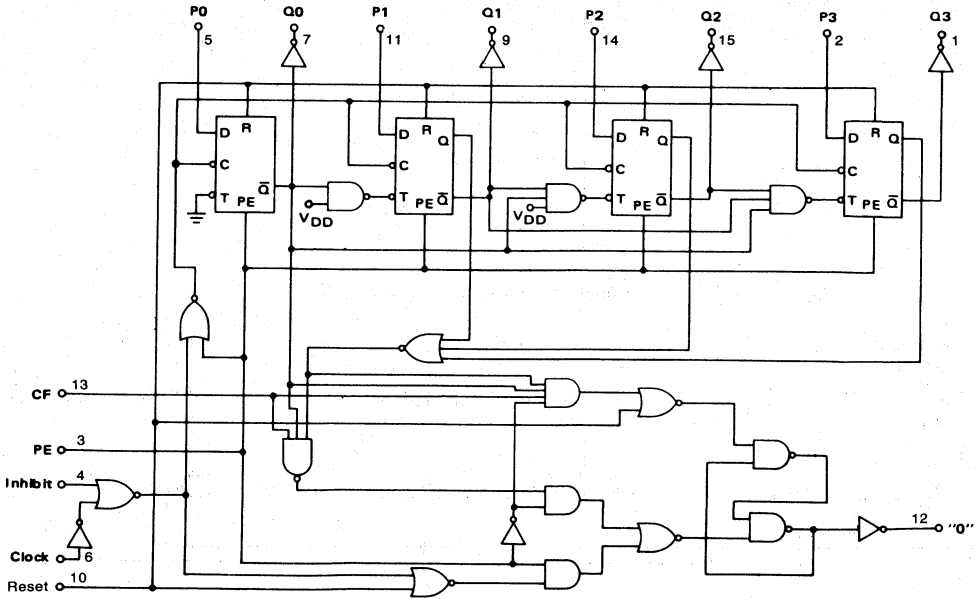
6

MC14522B•MC14526B

MC14522B LOGIC DIAGRAM (BCD Down Counter)



MC14526B LOGIC DIAGRAM (Binary Down Counter)



MC14522B•MC14526B

APPLICATIONS INFORMATION

Divide-By-N, Single Stage

Figure 11 shows a single stage divide-by-N application. The MC14522B (BCD version) can accept a number greater than 9 and count down in binary fashion. Hence, the BCD and binary single stage divide-by-N counters (as shown in Figure 11) function the same.

To initialize counting a number, N is set on the parallel inputs (P0, P1, P2, and P3) and reset is taken high asynchronously. A zero is forced into the master and slave of each bit and, at the same time, the "0" output goes high. Because Preset Enable is tied to the "0" output, preset is enabled. Reset must be released while the Clock is high so the slaves of each bit may receive N before the Clock goes low. When the Clock goes low and Reset is low, the "0" output goes low (if P0 through P3 are unequal to zero).

The counter downcounts with each rising edge of the Clock. When the counter reaches the zero state, an output pulse occurs on "0" which presets N. The propagation delays from the Clock's rising and falling edges to the "0" output's rising and falling edges are about equal, making the "0" output pulse approximately equal to that of the Clock pulse.

The Inhibit pin may be used to stop pulse counting. When this pin is taken high, decrementing is inhibited.

Cascaded, Presetable Divide-By-N

Figure 12 shows a three stage cascade application. Taking Reset high loads N. Only the first stage's Reset pin (least significant counter) must be taken high to cause the preset for all stages, but all pins could be tied together, as shown.

When the first stage's Reset pin goes high, the "0" output is latched in a high state. Reset must be released while Clock is high and time allowed for Preset Enable to load N into all stages before Clock goes low.

When Preset Enable is high and Clock is low, time must be allowed for the zero digits to propagate a Cascade Feedback to the first non-zero stage. Worst case is from the most significant bit (M.S.B.) to the L.S.B., when the L.S.B. is equal to one (i.e. $N=1$).

After N is loaded, each stage counts down to zero with each rising edge of Clock. When any stage reaches zero and the leading stages (more significant bits) are zero, the "0" output goes high and feeds back to the preceding stage. When all stages are zero, the Preset Enable automatically loads N while the Clock is high and the cycle is renewed.

FIGURE 11 — ÷N COUNTER

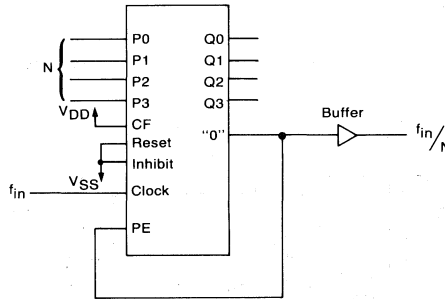
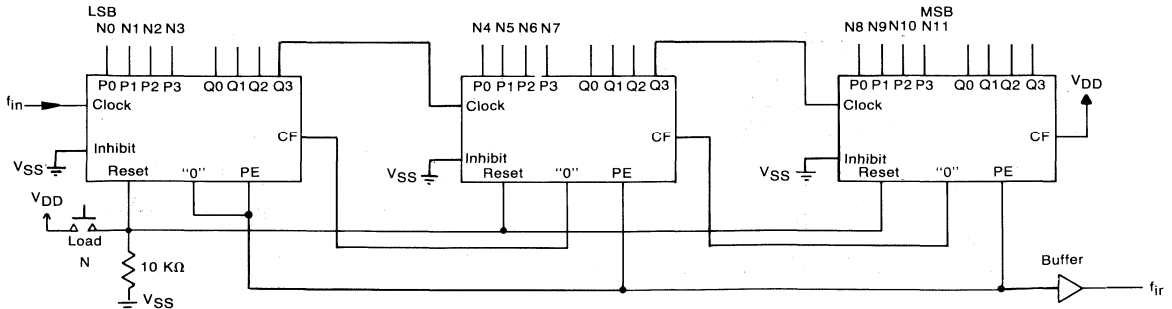


FIGURE 12 — 3 STAGES CASCADED





MOTOROLA

MC14527B

BCD RATE MULTIPLIER

The MC14527B BCD rate multiplier (DRM) provides an output pulse rate based upon the BCD input number. For example, if 6 is the BCD input number, there will be six output pulses for every ten input pulses. This part may be used for arithmetic operations including multiplication and division. Typical applications include digital filters, motor speed control and frequency synthesizers.

- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Output Clocked on the Negative Going Edge of Clock
- Strobe for Inhibiting or Enabling Outputs
- Enable and Cascade Inputs for Cascade Operation of Two or More DRM's
- "9" Output for the Parallel Enable Configuration and DRM's in Cascade
- Complementary Outputs
- Clear and Set to Nine Inputs

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V _{DD}	DC Supply Voltage	-0.5 to +18.0	V
V _{in} , V _{out}	Input or Output Voltage (DC or Transient)	-0.5 to V _{DD} + 0.5	V
I _{in} , I _{out}	Input or Output Current (DC or Transient), per Pin	± 10	mA
P _D	Power Dissipation, per Package†	500	mW
T _{stg}	Storage Temperature	-65 to +150	°C
T _L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.

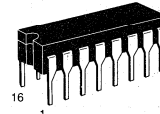
†Temperature Derating: Plastic "P and D/DW" Packages: -7.0 mW/°C From 65°C To 125°C
Ceramic "L" Packages: -12 mW/°C From 100°C To 125°C

TRUTH TABLE

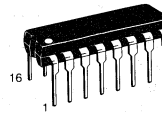
INPUTS										OUTPUT				
D*	C	B	A	No. of Clock Pulses	E _{in}	STROBE	CASCADE	CLEAR	SET	LOGIC LEVEL				
										NUMBER OF PULSES				
										OUT	OUT	E _{out}	"9"	
0	0	0	0	10	0	0	0	0	0	0	1	1	1	1
0	0	0	1	10	0	0	0	0	0	1	1	1	1	1
0	0	1	0	10	0	0	0	0	0	2	2	1	1	1
0	0	1	1	10	0	0	0	0	0	3	3	1	1	1
0	1	0	0	10	0	0	0	0	0	4	4	1	1	1
0	1	0	1	10	0	0	0	0	0	5	5	1	1	1
0	1	1	0	10	0	0	0	0	0	6	6	1	1	1
0	1	1	1	10	0	0	0	0	0	7	7	1	1	1
1	0	0	0	10	0	0	0	0	0	8	8	1	1	1
1	0	0	1	10	0	0	0	0	0	9	9	1	1	1
1	0	1	0	10	0	0	0	0	0	8	8	1	1	1
1	0	1	1	10	0	0	0	0	0	9	9	1	1	1
1	1	0	0	10	0	0	0	0	0	8	8	1	1	1
1	1	0	1	10	0	0	0	0	0	9	9	1	1	1
1	1	1	0	10	0	0	0	0	0	8	8	1	1	1
1	1	1	1	10	0	0	0	0	0	9	9	1	1	1
X	X	X	X	10	1	0	0	0	0	-	-	-	-	-
X	X	X	X	10	0	1	0	0	0	0	1	1	1	1
X	X	X	X	10	0	0	1	0	0	0	0	1	1	1
0	X	X	X	10	0	0	0	1	0	10	10	1	0	0
0	X	X	X	10	0	0	0	1	0	0	1	1	0	0
X	X	X	X	10	0	0	0	0	1	0	1	0	1	1

X = Don't Care

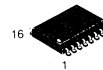
*D = Most Significant Bit



L SUFFIX
CERAMIC
CASE 620



P SUFFIX
PLASTIC
CASE 648



DW SUFFIX
SOIC
CASE 751G

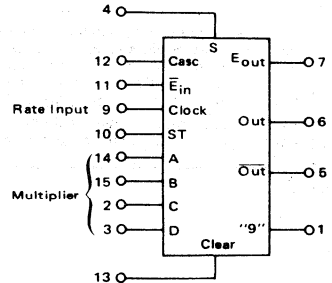
ORDERING INFORMATION

MC14XXXBCP Plastic
MC14XXXBCL Ceramic
MC14XXXBDW SOIC

T_A = -55° to 125°C for all packages.

6

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

MC14527B

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V _{DD} Vdc	-55°C		25°C			125°C		Unit
			Min	Max	Min	Typ #	Max	Min	Max	
Output Voltage V _{in} = V _{DD} or 0	V _{OL}	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
		10	—	0.05	—	0	0.05	—	0.05	
V _{in} = 0 or V _{DD}	V _{OH}	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc
		10	9.95	—	9.95	10	—	9.95	—	
Input Voltage (V _O = 4.5 or 0.5 Vdc) (V _O = 9.0 or 1.0 Vdc) (V _O = 13.5 or 1.5 Vdc)	V _{IL}	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc
		10	—	3.0	—	4.50	3.0	—	3.0	
		15	—	4.0	—	6.75	4.0	—	4.0	
(V _O = 0.5 or 4.5 Vdc) (V _O = 1.0 or 9.0 Vdc) (V _O = 1.5 or 13.5 Vdc)	V _{IH}	5.0	3.5	—	3.5	2.75	—	3.5	—	Vdc
		10	7.0	—	7.0	5.50	—	7.0	—	
		15	11	—	11	8.25	—	11	—	
Output Drive Current (V _{OH} = 2.5 Vdc) (V _{OH} = 4.6 Vdc) (V _{OH} = 9.5 Vdc) (V _{OH} = 13.5 Vdc)	Source I _{OH}	5.0	-3.0	—	-2.4	-4.2	—	-1.7	—	mA _{dc}
		5.0	-0.64	—	-0.51	-0.88	—	-0.36	—	
		10	-1.6	—	-1.3	-2.25	—	-0.9	—	
		15	-4.2	—	-3.4	-8.8	—	-2.4	—	
	Sink I _{OL}	5.0	0.64	—	0.51	0.88	—	0.36	—	mA _{dc}
		10	1.6	—	1.3	2.25	—	0.9	—	
(V _{OL} = 0.4 Vdc) (V _{OL} = 0.5 Vdc) (V _{OL} = 1.5 Vdc)		15	4.2	—	3.4	8.8	—	2.4	—	
Input Current	I _{in}	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	μA _{dc}
Input Capacitance (V _{in} = 0)	C _{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)	I _{DD}	5.0	—	5.0	—	0.005	5.0	—	150	μA _{dc}
		10	—	10	—	0.010	10	—	300	
		15	—	20	—	0.015	20	—	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C _L = 50 pF on all outputs, all buffers switching)	I _T	5.0	I _T = (0.85 μA/kHz) f + I _{DD} I _T = (1.75 μA/kHz) f + I _{DD} I _T = (2.60 μA/kHz) f + I _{DD}						μA _{dc}	
		10								
		15								

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

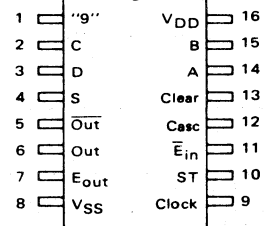
$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) V/k$$

where: I_T is in μA (per package), C_L in pF, V = (V_{DD} - V_{SS}) in volts, f in kHz is input frequency, and k = 0.0012.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range V_{SS} ≤ (V_{in} or V_{out}) ≤ V_{DD}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

PIN ASSIGNMENT



MC14527B

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V _{DD}	Min	Typ #	Max	Unit	
Output Rise and Fall Time t _{TLH} , t _{FHL} = (1.5 ns/pF) C _L + 25 ns t _{TLH} , t _{FHL} = (0.75 ns/pF) C _L + 12.5 ns t _{TLH} , t _{FHL} = (0.55 ns/pF) C _L + 9.5 ns	t _{TLH} , t _{FHL}	5.0	—	100	200	ns	
		10	—	50	100		
		15	—	40	80		
Propagation Delay Time Clock to Out t _{PLH} , t _{PHL} = (1.7 ns/pF) C _L + 115 ns t _{PLH} , t _{PHL} = (0.66 ns/pF) C _L + 67 ns t _{PLH} , t _{PHL} = (0.5 ns/pF) C _L + 45 ns Clock to Out t _{PLH} , t _{PHL} = (1.7 ns/pF) C _L + 40 ns t _{PLH} , t _{PHL} = (0.66 ns/pF) C _L + 32 ns t _{PLH} , t _{PHL} = (0.5 ns/pF) C _L + 20 ns Clock to E _{out} t _{PLH} , t _{PHL} = (1.7 ns/pF) C _L + 210 ns t _{PLH} , t _{PHL} = (0.66 ns/pF) C _L + 97 ns t _{PLH} , t _{PHL} = (0.5 ns/pF) C _L + 60 ns Clock to '9' t _{PLH} , t _{PHL} = (1.7 ns/pF) C _L + 315 ns t _{PLH} , t _{PHL} = (0.66 ns/pF) C _L + 122 ns t _{PLH} , t _{PHL} = (0.5 ns/pF) C _L + 85 ns Set or Clear to Out t _{PHL} = (1.7 ns/pF) C _L + 295 ns t _{PHL} = (0.66 ns/pF) C _L + 132 ns t _{PHL} = (0.5 ns/pF) C _L + 85 ns Cascade to Out t _{PHL} = (1.7 ns/pF) C _L + 40 ns t _{PHL} = (0.66 ns/pF) C _L + 32 ns t _{PHL} = (0.5 ns/pF) C _L + 20 ns Strobe to Out t _{PHL} = (1.7 ns/pF) C _L + 145 ns t _{PHL} = (0.66 ns/pF) C _L + 72 ns t _{PHL} = (0.5 ns/pF) C _L + 45 ns	t _{PHL} , t _{PHL}	5.0	—	200	400	ns	
		10	—	100	200		
		15	—	70	140		
		t _{PLH} , t _{PHL}	5.0	—	125	250	ns
			10	—	65	130	
			15	—	45	90	
		t _{PLH} , t _{PHL}	5.0	—	295	590	ns
			10	—	130	260	
			15	—	85	170	
		t _{PLH} , t _{PHL}	5.0	—	400	800	ns
			10	—	155	310	
			15	—	110	220	
		t _{PHL}	5.0	—	380	760	ns
			10	—	165	330	
			15	—	110	220	
		t _{PLH}	5.0	—	125	250	ns
			10	—	65	130	
			15	—	45	90	
		t _{PLH}	5.0	—	230	260	ns
			10	—	105	210	
			15	—	70	140	
	Clock Pulse Width	t _{WH}	5.0	500	250	—	ns
			10	200	110	—	
			15	150	80	—	
Clock Pulse Frequency	f _{cl}	5.0	—	2.0	1.2	MHz	
		10	—	4.5	2.5		
		15	—	6.0	3.5		
Clock Pulse Rise and Fall Time	t _{TLH} , t _{FHL}	5.0	—	—	15	μs	
		10	—	—	5		
		15	—	—	4		
Set or Clear Pulse Width	t _{WH}	5.0	240	80	—	ns	
		10	100	35	—		
		15	75	30	—		
Set Removal Time	t _{rem}	5.0	0	-20	—	ns	
		10	0	-10	—		
		15	0	-7.5	—		
Enable In Setup Time	t _{su}	5.0	400	175	—	ns	
		10	150	60	—		
		15	120	45	—		

*The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

MC14527B

FIGURE 1 – TEST CIRCUIT AND TIMING DIAGRAM

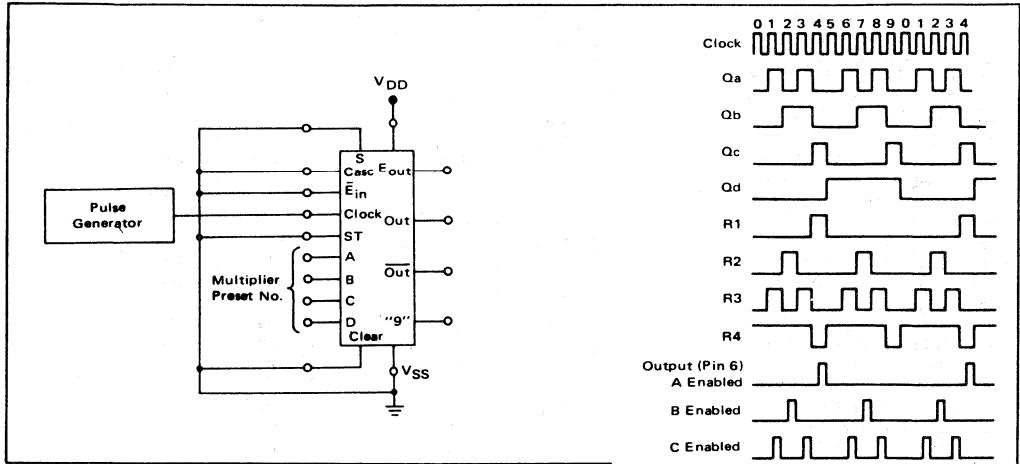
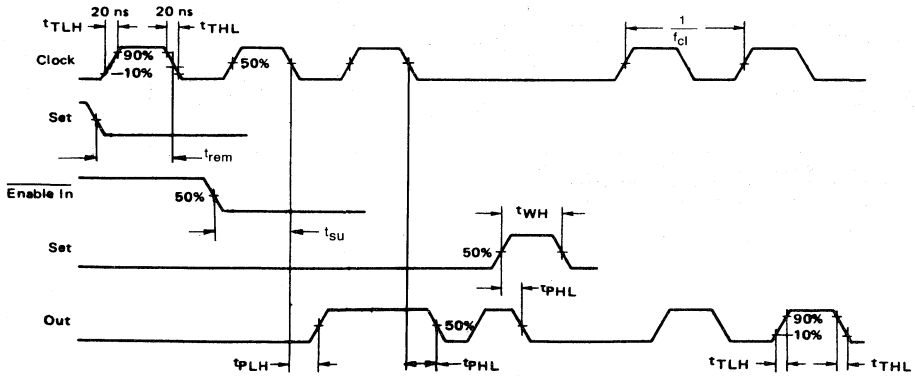
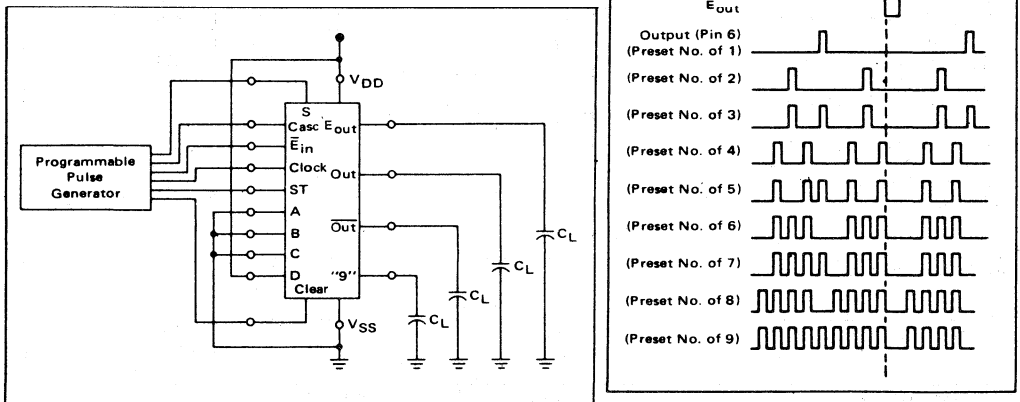


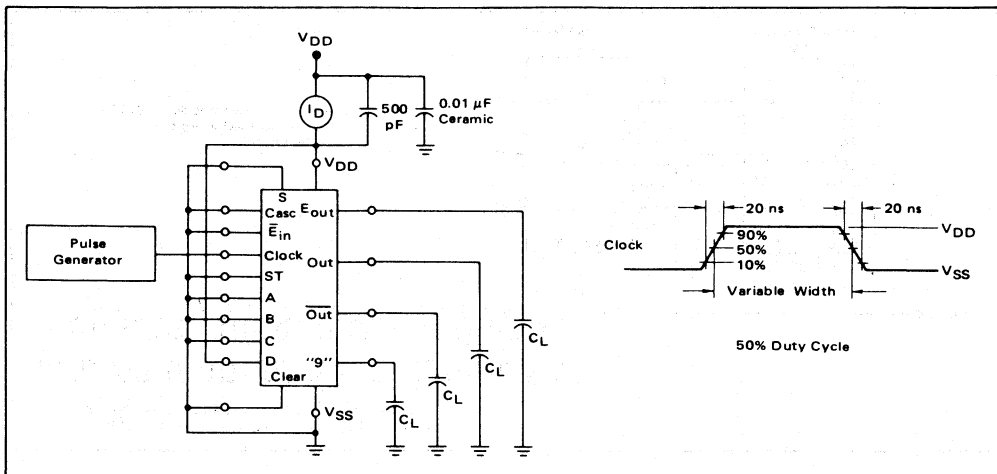
FIGURE 2 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



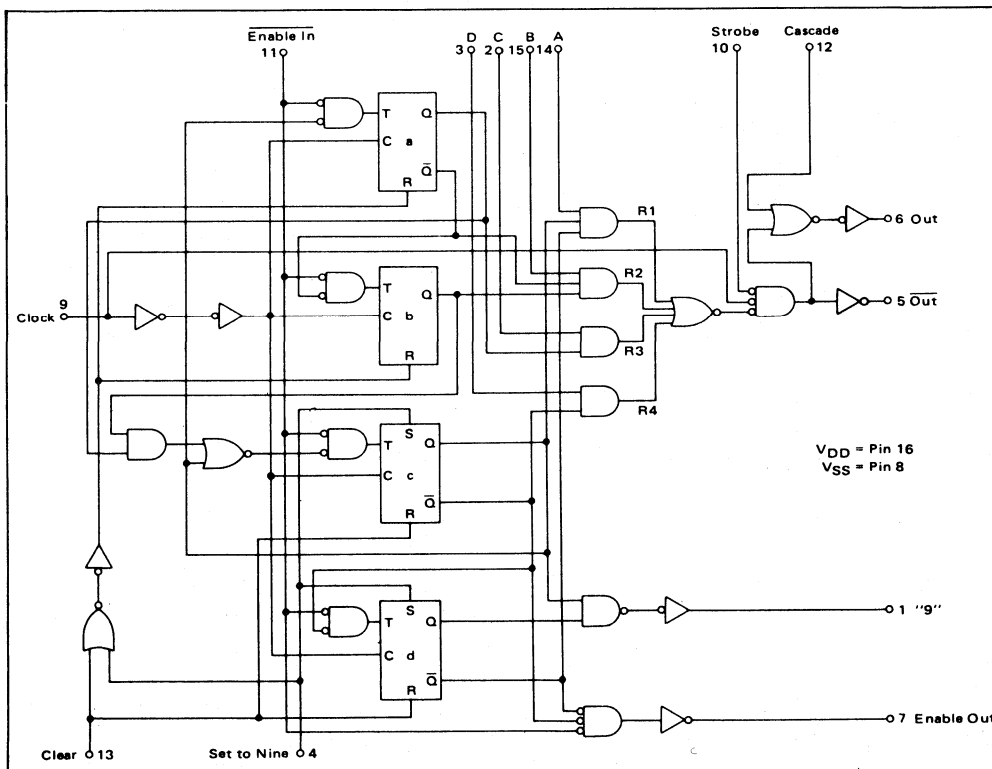
6

MC14527B

FIGURE 3 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

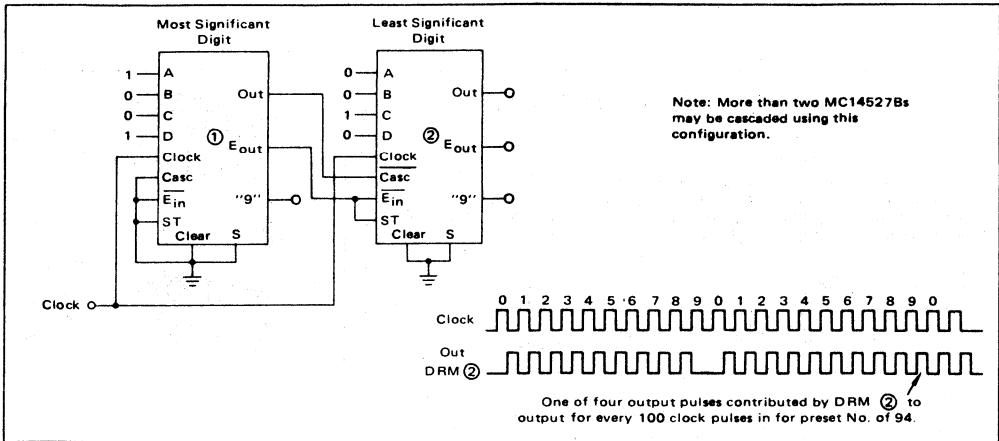


LOGIC DIAGRAM



MC14527B

FIGURE 4 – TWO MC14527Bs IN CASCADE WITH PRESET NO. of 94





MC14528B

DUAL MONOSTABLE MULTIVIBRATOR

The MC14528B is a dual, retriggerable, resettable monostable multivibrator. It may be triggered from either edge of an input pulse, and produces an output pulse over a wide range of widths, the duration of which is determined by the external timing components, C_X and R_X .

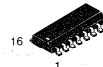
- Separate Reset Available
- Diode Protection on All Inputs
- Triggerable from Leading or Trailing Edge Pulse
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range
- Pin-for-Pin Replacement with the MC14538B



L SUFFIX
CERAMIC
CASE 620



P SUFFIX
PLASTIC
CASE 648



D SUFFIX
SOIC
CASE 751B

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	-0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	-0.5 to $V_{DD} + 0.5$	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	± 10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.

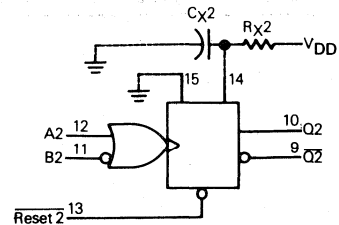
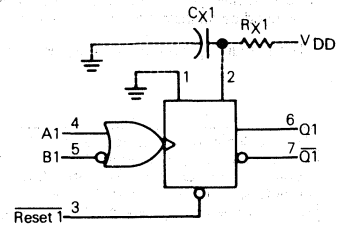
†Temperature Derating: Plastic "P and D/DW" Packages: -7.0 mW/°C From 65°C To 125°C
Ceramic "L" Packages: -12 mW/°C From 100°C To 125°C

ORDERING INFORMATION

MC14XXXBCP Plastic
MC14XXXBCL Ceramic
MC14XXXBD SOIC

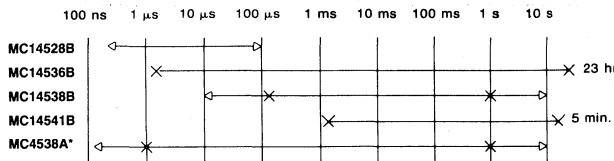
$T_A = -55^\circ$ to 125° C for all packages.

BLOCK DIAGRAM



V_{DD} = Pin 16
 V_{SS} = Pin 1, Pin 8, Pin 15
 R_X and C_X are external components

ONE-SHOT SELECTION GUIDE



*LIMITED OPERATING VOLTAGE (2-6V)

Total Output Pulse Width Range \longleftrightarrow
Recommended Pulse Width Range $\times \times \times$

MC14528B

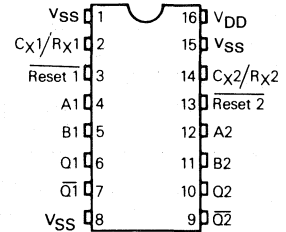
ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V _{DD} Vdc	-55°C		25°C			125°C		Unit
			Min	Max	Min	Typ #	Max	Min	Max	
Output Voltage V _{in} = V _{DD} or 0 "0" Level	V _{OL}	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
		10	—	0.05	—	0	0.05	—	0.05	
15		—	0.05	—	0	0.05	—	0.05		
V _{in} = 0 or V _{DD} "1" Level	V _{OH}	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc
		10	9.95	—	9.95	10	—	9.95	—	
		15	14.95	—	14.95	15	—	14.95	—	
Input Voltage (V _O = 4.5 or 0.5 Vdc) (V _O = 9.0 or 1.0 Vdc) (V _O = 13.5 or 1.5 Vdc) "0" Level	V _{IL}	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc
		10	—	3.0	—	4.50	3.0	—	3.0	
15		—	4.0	—	6.75	4.0	—	4.0		
(V _O = 0.5 or 4.5 Vdc) (V _O = 1.0 or 9.0 Vdc) (V _O = 1.5 or 13.5 Vdc) "1" Level	V _{IH}	5.0	3.5	—	3.5	2.75	—	3.5	—	Vdc
		10	7.0	—	7.0	5.50	—	7.0	—	
		15	11	—	11	8.25	—	11	—	
Output Drive Current (V _{OH} = 2.5 Vdc) (V _{OH} = 4.6 Vdc) (V _{OH} = 9.5 Vdc) (V _{OH} = 13.5 Vdc) Source	I _{OH}	5.0	-1.2	—	-1.0	-1.7	—	-0.7	—	mAdc
		5.0	-0.64	—	-0.51	-0.88	—	-0.36	—	
10		-1.6	—	-1.3	-2.25	—	-0.9	—		
15		-4.2	—	-3.4	-8.8	—	-2.4	—		
(V _{OL} = 0.4 Vdc) (V _{OL} = 0.5 Vdc) (V _{OL} = 1.5 Vdc) Sink	I _{OL}	5.0	0.64	—	0.51	0.88	—	0.36	—	mAdc
10		1.6	—	1.3	2.25	—	0.9	—		
15		4.2	—	3.4	8.8	—	2.4	—		
Input Current	I _{in}	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	μAdc
Input Capacitance (V _{in} = 0)	C _{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)	I _{DD}	5.0	—	5.0	—	0.005	5.0	—	150	μAdc
		10	—	10	—	0.010	10	—	300	
		15	—	20	—	0.015	20	—	600	
**Total Supply Current at an external load Capacitance (C _L) and at external timing capacitance (C _X), use the formula —	I _T	—	$I_T(C_L, C_X) = [(C_L + 0.36C_X)V_{DD}f + 2 \times 10^{-8} R_X C_X (V_{DD} - 2)^2] \times 10^{-3}$ where: I _T in μA (per circuit), C _L and C _X in pF, R _X in megohms, V _{DD} in Vdc, f in kHz is input frequency.						μAdc	

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C.

PIN ASSIGNMENT



This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range V_{SS} ≤ (V_{in} or V_{out}) ≤ V_{DD}. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

MC14528B

SWITCHING CHARACTERISTICS** ($C_L = 50 \text{ pF}$, $T_A = 25^\circ\text{C}$)

Characteristic	Symbol	C_X pF	R_X k Ω	V_{DD} Vdc	Min	Typ #	Max	Unit
Output Rise and Fall Time $t_{TLH}, t_{THL} = (1.5 \text{ ns/pF}) C_L + 25 \text{ ns}$ $t_{TLH}, t_{THL} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$ $t_{TLH}, t_{THL} = (0.55 \text{ ns/pF}) C_L + 9.5 \text{ ns}$	t_{TLH}, t_{THL}	—	—	5.0 10 15	— — —	100 50 40	200 100 80	ns
Turn-Off, Turn-On Delay Time — A or B to Q or \bar{Q} $t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 240 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 87 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 65 \text{ ns}$	t_{PLH}, t_{PHL}	15	5.0	5.0 10 15	— — —	325 120 90	650 240 180	ns
Turn-Off, Turn-On Delay Time — A or B to Q or \bar{Q} $t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 620 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 257 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 185 \text{ ns}$	t_{PLH}, t_{PHL}	1000	10	5.0 10 15	— — —	705 290 210	— — —	ns
Input Pulse Width — A or B	t_{WH}	15	5.0	5.0 10 15	150 75 55	70 30 30	— — —	ns
	t_{WL}	1000	10	5.0 10 15	— — —	70 30 30	— — —	ns
Output Pulse Width — Q or \bar{Q} (For $C_X < 0.01 \mu\text{F}$ use graph for appropriate V_{DD} level.)	t_W	15	5.0	5.0 10 15	— — —	550 350 300	— — —	ns
Output Pulse Width — Q or \bar{Q} (For $C_X > 0.01 \mu\text{F}$ use formula: $t_W = 0.2 R_X C_X \ln (V_{DD} - V_{SS})^\dagger$)	t_W	10,000	10	5.0 10 15	15 10 15	30 50 55	45 90 95	μs
Pulse Width Match between Circuits in the same package	t1 - t2	10,000	10	5.0 10 15	— — —	6.0 8.0 8.0	25 35 35	%
Reset Propagation Delay — Reset to Q or \bar{Q}	t_{PLH}, t_{PHL}	15	5.0	5.0 10 15	— — —	325 90 60	600 225 170	ns
		1000	10	5.0 10 15	— — —	1000 300 250	— — —	ns
Retrigger Time	t_{rr}	15	5.0	5.0 10 15	0 0 0	— — —	— — —	ns
		1000	10	5.0 10 15	0 0 0	— — —	— — —	ns
External Timing Resistance	R_X	—	—	—	5.0	—	1000	k Ω
External Timing Capacitance	C_X	—	—	—	—	No Limits*		μF

† R_X is in Ohms, C_X is in farads, V_{DD} and V_{SS} in volts, PW_{out} in seconds.

* If $C_X > 15 \mu\text{F}$, Use Discharge Protection Diode D_X , per Fig. 9.

**The formulas given are for the typical characteristics only at 25°C .

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

FUNCTION TABLE

Reset	Inputs		Outputs	
	A	B	Q	\bar{Q}
H		H		
H	L			
H		L	Not Triggered	Not Triggered
H	H		Not Triggered	Not Triggered
H	L, H,	H	Not Triggered	Not Triggered
H	L	L, H,	Not Triggered	Not Triggered
L	X	X	L	H
	X	X	Not Triggered	

MC14528B

FIGURE 1 – OUTPUT SOURCE CURRENT TEST CIRCUIT

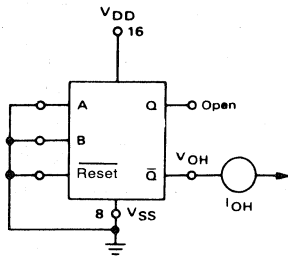


FIGURE 2 – OUTPUT SINK CURRENT TEST CIRCUIT

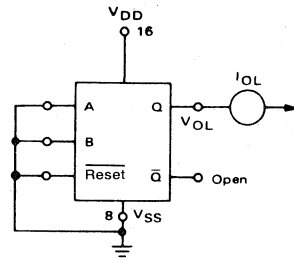


FIGURE 3 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORMS

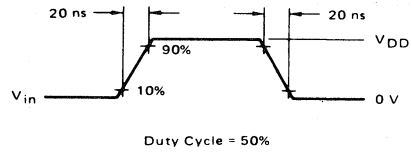
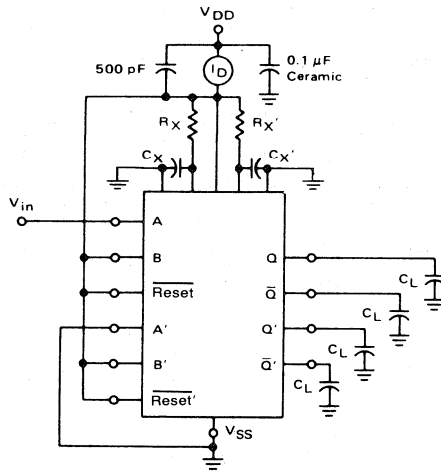
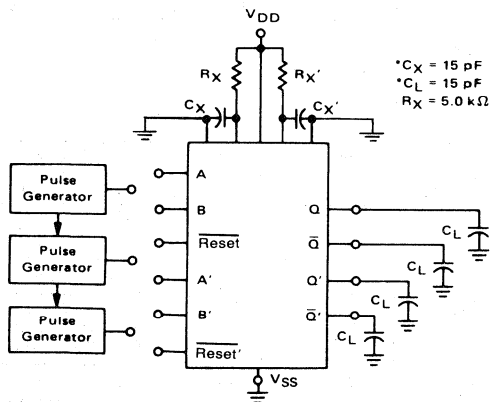


FIGURE 4 – AC TEST CIRCUIT

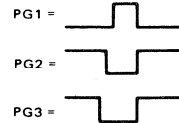


INPUT CONNECTIONS

CHARACTERISTICS	Reset	A	B
t_{PLH} , t_{PHL} , t_{TLH} , t_{THL} t_W	V_{DD}	PG1	V_{DD}
t_{PLH} , t_{PHL} , t_{TLH} , t_{THL} t_W	V_{DD}	V_{SS}	PG2
$t_{PLH(R)}$, $t_{PHL(R)}$, t_W	PG3	PG1	PG2

*Includes capacitance of probes, wiring, and fixture parasitic.

NOTE: AC test waveforms for PG1, PG2, and PG3 on next page.



MC14528B

FIGURE 5 – AC TEST WAVEFORMS

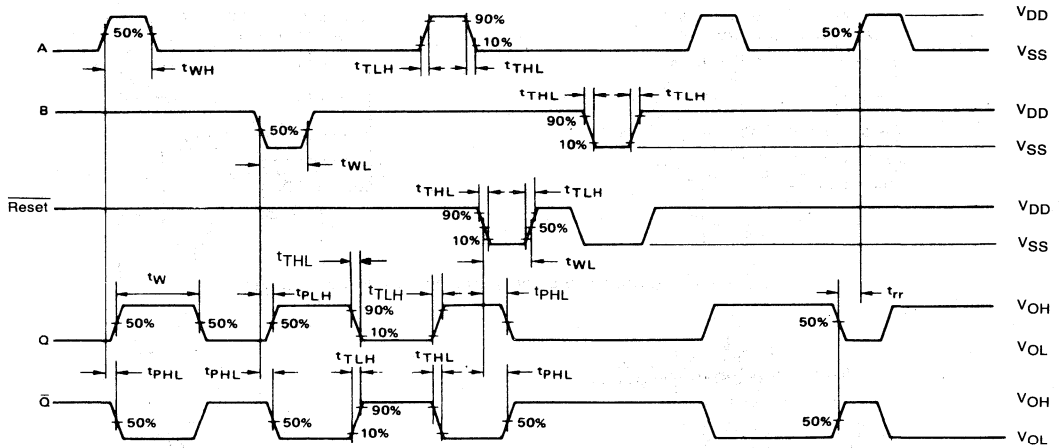
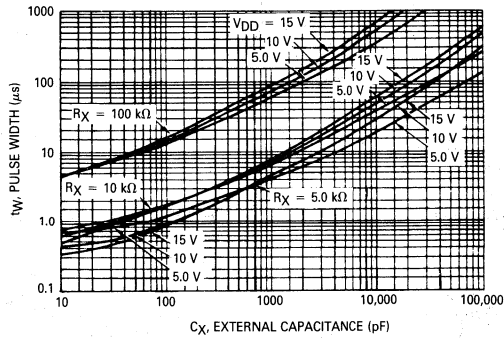


FIGURE 6 – PULSE WIDTH versus C_X



MC14528B

TYPICAL APPLICATIONS

FIGURE 7 — RETRIGGERABLE MONOSTABLES CIRCUITRY

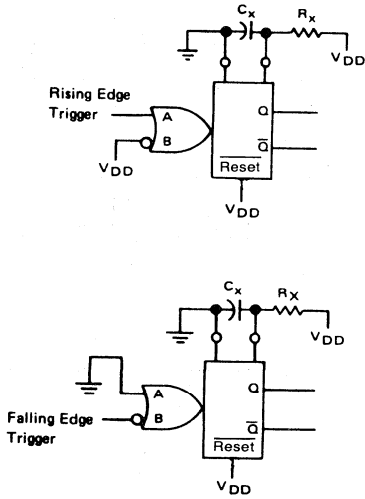


FIGURE 8 — NON-RETRIGGERABLE MONOSTABLES CIRCUITRY

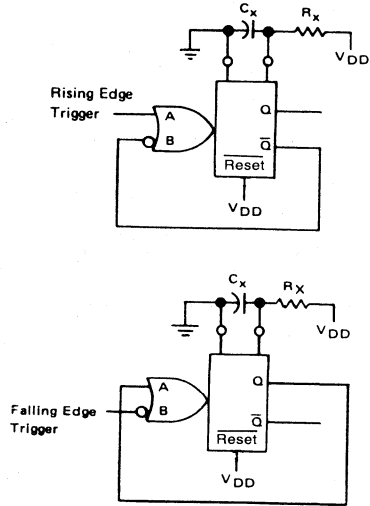


FIGURE 9 — USE OF A DIODE TO LIMIT POWER DOWN CURRENT SURGE

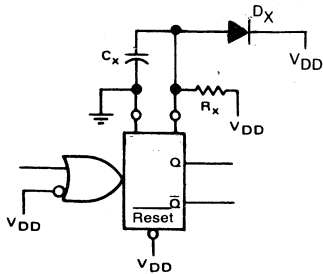
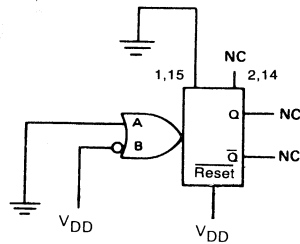


FIGURE 10 — CONNECTION OF UNUSED SECTIONS





MOTOROLA

MC14529B

DUAL 4-CHANNEL ANALOG DATA SELECTOR

The MC14529B analog data selector is a dual 4-channel or single 8-channel device depending on the input coding. The device is suitable for digital as well as analog application, including various one-of-four and one-of-eight data selector functions. Since the device has bidirectional analog characteristics it can also be used as a dual binary to 1-of-4 or a binary to 1-of-8 decoder.

- Data Paths Are Bidirectional
- 3-State Outputs
- Linear "On" Resistance
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load over the Rated Temperature Range.

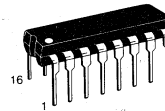
MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	-0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	-0.5 to $V_{DD} + 0.5$	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

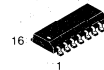
*Maximum Ratings are those values beyond which damage to the device may occur.
 †Temperature Derating: Plastic "P and D/DW" Packages: -7.0 mW/°C From 65°C To 125°C
 Ceramic "L" Packages: -12 mW/°C From 100°C To 125°C



L SUFFIX
 CERAMIC
 CASE 620



P SUFFIX
 PLASTIC
 CASE 648



D SUFFIX
 SOIC
 CASE 751B

ORDERING INFORMATION

MC14XXXBCP Plastic
 MC14XXXBCL Ceramic
 MC14XXXBD SOIC

$T_A = -55^\circ\text{C}$ to 125°C for all packages.

TRUTH TABLE

ST _X	ST _Y	B	A	Z	W
1	1	0	0	X0	Y0
1	1	0	1	X1	Y1
1	1	1	0	X2	Y2
1	1	1	1	X3	Y3
1	0	0	0	X0	
1	0	0	1	X1	
1	0	1	0	X2	
1	0	1	1	X3	
0	1	0	0		Y0
0	1	0	1		Y1
0	1	1	0		Y2
0	1	1	1		Y3
0	0	X	X		High Impedance

Dual 4-Channel Mode
 2 Outputs

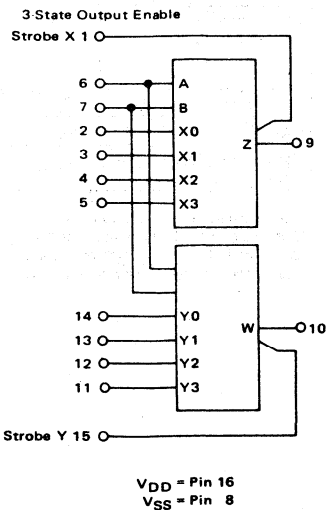
Single 8-Channel Mode
 1 Output
 (Z and W tied together)

X = Don't Care

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

BLOCK DIAGRAM



MC14529B

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V _{DD}	Test Conditions	-55°C		25°C			125°C		Unit
				Min	Max	Min	Typ #	Max	Min	Max	

SUPPLY REQUIREMENTS (Voltages Referenced to V_{EE})

Power Supply Voltage Range	V _{DD}	—	V _{DD} - 3.0 ≥ V _{SS} ≥ V _{EE}	3.0	18	3.0	—	18	3.0	18	V		
Quiescent Current Per Package	I _{DD}	5.0 10 15	Control Inputs: V _{in} = V _{SS} or V _{DD} , Switch I/O: V _{SS} ≤ V _{I/O} ≤ V _{DD} , and ΔV _{switch} ≤ 500 mV**	— — —	1.0 1.0 2.0	— — —	0.005 0.010 0.015	1.0 1.0 2.0	— — —	60 60 120	μA		
Total Supply Current (Dynamic Plus Quiescent, Per Package)	I _{D(AV)}	5.0 10 15	T _A = 25°C only (The channel component, (V _{in} - V _{out})/R _{on} , is not included.)	Typical (0.07 μA/kHz)f + I _{DD} (0.20 μA/kHz)f + I _{DD} (0.36 μA/kHz)f + I _{DD}						—	—	—	μA

CONTROL INPUTS — INHIBIT, A, B (Voltages Referenced to V_{SS})

Low-Level Input Voltage	V _{IL}	5.0 10 15	R _{on} = per spec, I _{off} = per spec	— — —	1.5 3.0 4.0	— — —	2.25 4.50 6.75	1.5 3.0 4.0	— — —	1.5 3.0 4.0	V
High-Level Input Voltage	V _{IH}	5.0 10 15	R _{on} = per spec, I _{off} = per spec	3.5 7.0 11	— — —	3.5 7.0 11	2.75 5.50 8.25	— — —	3.5 7.0 11	— — —	V
Input Leakage Current	I _{in}	15	V _{in} = 0 or V _{DD}	—	±0.1	—	±0.00001	±0.1	—	±1.0	μA
Input Capacitance	C _{in}	—	—	—	—	—	5.0	7.5	—	—	pF

SWITCHES IN/OUT AND COMMONS OUT/IN — W, Z (Voltages Referenced to V_{EE})

Recommended Peak-to-Peak Voltage Into or Out of the Switch	V _{I/O}	—	Channel On or Off	0	V _{DD}	0	—	V _{DD}	0	V _{DD}	V _{p-p}
Recommended Static or Dynamic Voltage Across the Switch** (Figure 5)	ΔV _{switch}	—	Channel On	0	600	0	—	600	0	300	mV
Output Offset Voltage	V _{OO}	—	V _{in} = 0 V, No Load	—	—	—	10	—	—	—	μV
ON Resistance	R _{on}	10 15	ΔV _{switch} ≤ 500 mV**, V _{in} = V _{IL} or V _{IH} (Control), and V _{in} = 0 to V _{DD} (Switch)	— —	400 240	— —	120 80	480 270	— —	560 350	Ω
ΔON Resistance Between Any Two Channels in the Same Package	ΔR _{on}	10 15	—	— —	— —	— —	15 10	— —	— —	— —	Ω
Off-Channel Leakage Current (Figure 10)	I _{off}	15	V _{in} = V _{IL} or V _{IH} (Control) Channel to Channel or Any One Channel	—	±100	—	±0.05	±100	—	±1000	nA
Capacitance, Switch I/O	C _{I/O}	—	Inhibit = V _{DD}	—	—	—	8.0	—	—	—	pF
Capacitance, Common O/I	C _{O/I}	—	Inhibit = V _{DD}	—	—	—	20	—	—	—	pF
Capacitance, Feedthrough (Channel Off)	C _{I/O}	—	Pins Not Adjacent Pins Adjacent	— —	— —	— —	0.15 0.47	— —	— —	— —	pF

#Data labeled "Typ" is not to be used for design purposes, but is intended as an indication of the IC's potential performance.

**For voltage drops across the switch (ΔV_{switch}) > 600 mV (> 300 mV at high temperature), excessive V_{DD} current may be drawn; i.e. the current out of the switch may contain both V_{DD} and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded. (See first page of this data sheet.)

MC14529B

SWITCHING CHARACTERISTICS (T_A = 25°C)

Characteristic	Figure	Symbol	V _{SS}	V _{DD}	Min	Typ #	Max	Unit
V _{in} to V _{out} Propagation Delay Time (C _L = 50 pF, R _L = 1.0 kΩ)	7	t _{PLH} , t _{PHL}	0.0	5.0 10 15	— — —	20 10 8.0	40 20 15	ns
Propagation Delay Time, Control to Output, V _{in} = V _{DD} or V _{SS} (C _L = 50 pF, R _L = 1.0 kΩ)	8	t _{PLZ} , t _{PZL} , t _{PHZ} , t _{PZH}	0.0	5.0 10 15	— — —	140 70 50	400 160 120	ns
Crosstalk, Control to Output (C _L = 50 pF, R _L = 1.0 kΩ R _{out} = 10 kΩ)	9	—	0.0	5.0 10 15	— — —	5.0 5.0 5.0	— — —	mV
Control Input Pulse Frequency (C _L = 50 pF, R _L = 1.0 kΩ)	10	f _{in}	0.0	5.0 10 15	— — —	5.0 10 12	2.5 6.2 8.3	MHz
Noise Voltage (f = 100 Hz)	11,12	—	0.0	5.0 10 15 5.0 10 15	— — — — — —	24 25 30 12 12 15	— — — — — —	$\frac{\text{nV}}{\sqrt{\text{cycle}}}$
Sine Wave Distortion (V _{in} = 1.77 Vdc RMS Centered @ 0.0 Vdc, R _L = 10 kΩ, f = 1.0 kHz)	—	—	-5.0	5.0	—	0.36	—	%
Off-Channel Leakage Current (V _{in} = +5.0 Vdc, V _{out} = -5.0 Vdc) (V _{in} = -5.0 Vdc, V _{out} = +5.0 Vdc) (V _{in} = +7.5 Vdc, V _{out} = -7.5 Vdc) (V _{in} = -7.5 Vdc, V _{out} = +7.5 Vdc)	—	I _{off}	-5.0 -5.0 -7.5 -7.5	5.0 5.0 7.5 7.5	— — — —	± 0.001 ± 0.001 ± 0.0015 ± 0.0015	± 125 ± 125 ± 250 ± 250	nA
Insertion Loss (V _{in} = 1.77 Vdc RMS centered @ 0.0 Vdc, f = 1.0 MHz) I _{loss} = 20 Log ₁₀ $\frac{V_{out}}{V_{in}}$ (R _L = 1.0 kΩ) (R _L = 10 kΩ) (R _L = 100 kΩ) (R _L = 1.0 MΩ)	13	—	-5.0	5.0	— — — —	— 2.0 0.8 0.25 0.01	— — — —	dB
Bandwidth (-3 dB) (V _{in} = 1.77 Vdc RMS centered @ 0.0 Vdc) (R _L = 1.0 kΩ) (R _L = 10 kΩ) (R _L = 100 kΩ) (R _L = 1.0 MΩ)	—	BW	-5.0	5.0	— — — —	— 35 28 27 26	— — — —	MHz
Feedthrough and Crosstalk 20 Log ₁₀ $\frac{V_{out}}{V_{in}}$ = -50 dB (R _L = 1.0 kΩ) (R _L = 10 kΩ) (R _L = 100 kΩ) (R _L = 1.0 MΩ)	—	—	-5.0	5.0	— — — —	— 850 100 12 1.5	— — — —	MHz

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

FIGURE 1 - OUTPUT VOLTAGE TEST CIRCUIT

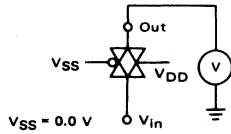
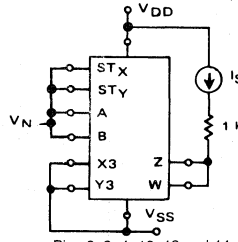


FIGURE 2 - NOISE IMMUNITY TEST CIRCUIT



Pins 2, 3, 4, 12, 13 and 14 are left open.
 V_{IL} : V_C is raised from V_{SS} until $V_C = V_{IL}$.
 at $V_C = V_{IL}$: $I_S = \pm 10 \mu A$ with $V_{in} = V_{SS}$, $V_{out} = V_{DD}$ or $V_{in} = V_{DD}$, $V_{out} = V_{SS}$.

V_{IH} : When $V_C = V_{IH}$ to V_{DD} , the switch is ON and the R_{ON} specifications are met.

FIGURE 3 - QUIESCENT POWER DISSIPATION TEST CIRCUIT

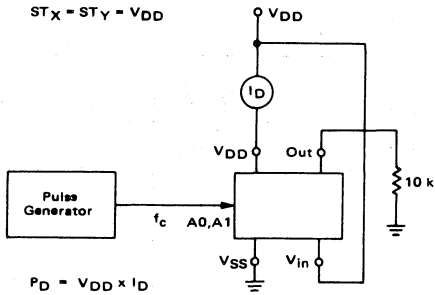
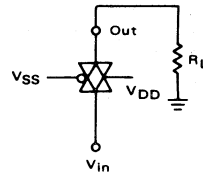


FIGURE 4 - RON CHARACTERISTICS TEST CIRCUIT



TYPICAL RON versus INPUT VOLTAGE

FIGURE 5

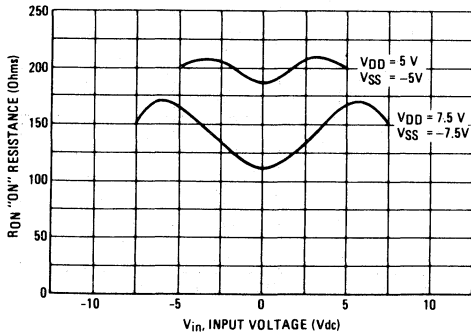
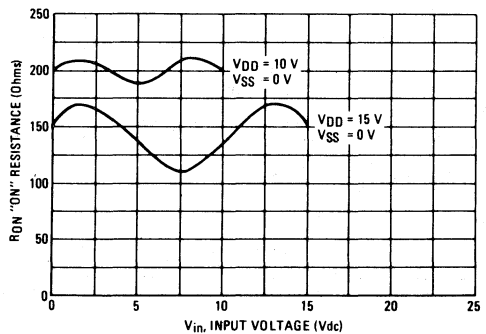


FIGURE 6



MC14529B

FIGURE 7 – PROPAGATION DELAY TEST CIRCUIT AND WAVEFORMS

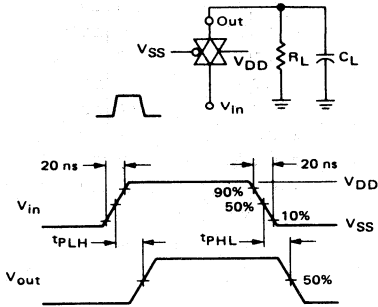


FIGURE 8 – TURN-ON DELAY TIME TEST CIRCUIT AND WAVEFORMS

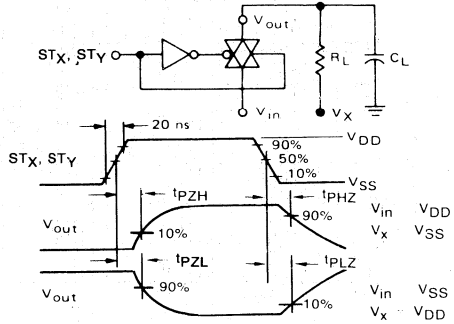


FIGURE 9 – CROSSTALK TEST CIRCUIT

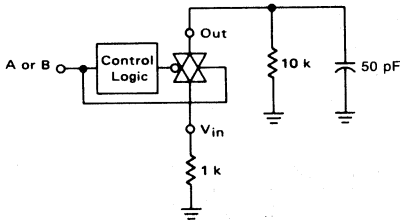


FIGURE 10 – FREQUENCY RESPONSE TEST CIRCUIT

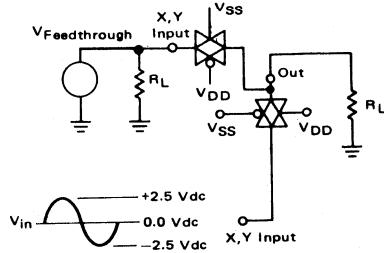


FIGURE 11 – NOISE VOLTAGE TEST CIRCUIT

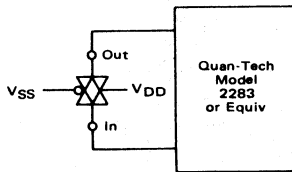
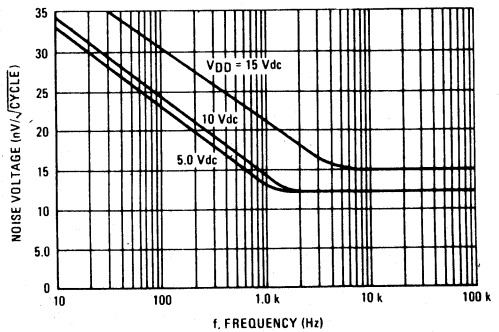
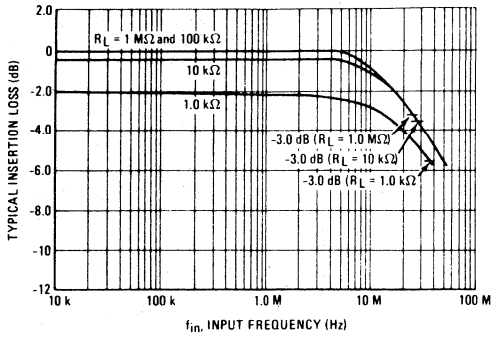


FIGURE 12 – TYPICAL NOISE CHARACTERISTICS

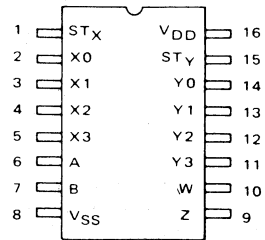


MC14529B

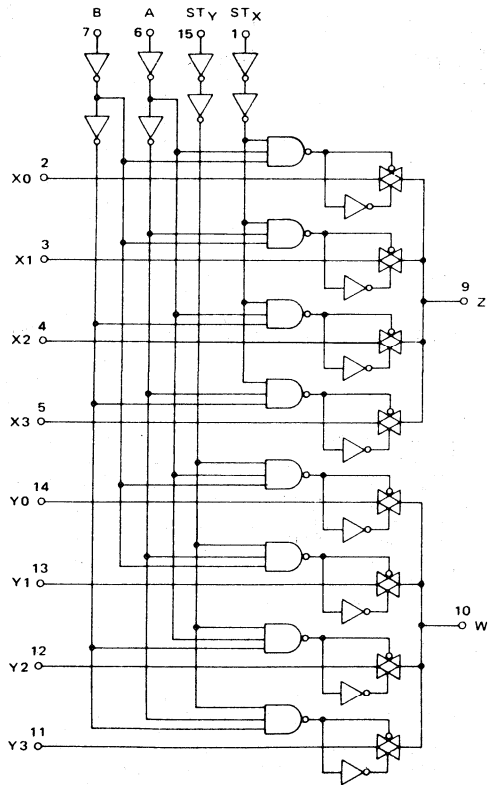
FIGURE 13 – TYPICAL INSERTION LOSS/BANDWIDTH CHARACTERISTICS



PIN ASSIGNMENT



LOGIC DIAGRAM



VDD = Pin 16
VSS = Pin 8



MOTOROLA

DUAL 5-INPUT MAJORITY LOGIC GATE

The MC14530B dual five-input majority logic gate is constructed with P-channel and N-channel enhancement mode devices in a single monolithic structure. Combinational and sequential logic expressions are easily implemented with the majority logic gate, often resulting in fewer components than obtainable with the more basic gates. This device can also provide numerous logic functions by using the W and some of the logic (A thru E) inputs as control inputs.

- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	-0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	-0.5 to $V_{DD} + 0.5$	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	± 10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
 †Temperature Derating: Plastic "P and D/DW" Packages: -7.0 mW/°C From 65°C To 125°C
 Ceramic "L" Packages: -12 mW/°C From 100°C To 125°C

LOGIC TABLE

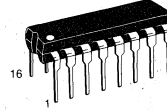
INPUTS A B C D E	W	Z
For all combinations of inputs where three or more inputs are logical "0".	0	1
For all combinations of inputs where three or more inputs are logical "1".	1	0
For all combinations of inputs where three or more inputs are logical "1".	0	0
For all combinations of inputs where three or more inputs are logical "1".	1	1

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

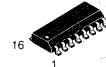
MC14530B



L SUFFIX
CERAMIC
CASE 620



P SUFFIX
PLASTIC
CASE 648



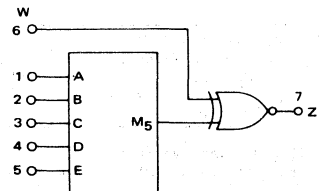
D SUFFIX
SOIC
CASE 751B

ORDERING INFORMATION

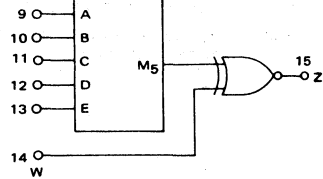
MC14XXXBCP Plastic
 MC14XXXBCL Ceramic
 MC14XXXBD SOIC

$T_A = -55^\circ$ to 125°C for all packages.

BLOCK DIAGRAM



$$Z = M_5 \odot W = (ABC+ABD+ABE+ACD+ACE+ADE+BCD+BCE+BDE+CDE) \odot W$$



*M₅ is a logical "1" if any three or more inputs are logical "1".

⊙ ≡ Exclusive NOR ≡ Exclusive OR

TRUTH TABLE

M ₅	W	Z
0	0	1
0	1	0
1	0	0
1	1	1

$V_{DD} = \text{Pin } 16$
 $V_{SS} = \text{Pin } 8$

MC14530B

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V _{DD} Vdc	-55°C		25°C			125°C		Unit	
			Min	Max	Min	Typ #	Max	Min	Max		
Output Voltage "0" Level V _{in} = V _{DD} or 0	V _{OL}	5.0	—	0.05	—	0	0.05	—	0.05	Vdc	
		10	—	0.05	—	0	0.05	—	0.05		
		15	—	0.05	—	0	0.05	—	0.05		
"1" Level V _{in} = 0 or V _{DD}	V _{OH}	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc	
		10	9.95	—	9.95	10	—	9.95	—		
		15	14.95	—	14.95	15	—	14.95	—		
Input Voltage "0" Level (V _O = 4.5 or 0.5 Vdc) (V _O = 9.0 or 1.0 Vdc) (V _O = 13.5 or 1.5 Vdc)	V _{IL}	5.0	—	1.2	—	2.25	1.25	—	1.15	Vdc	
		10	—	2.5	—	4.50	2.5	—	2.4		
		15	—	3.0	—	6.75	3.0	—	2.9		
	"1" Level (V _O = 0.5 or 4.5 Vdc) (V _O = 1.0 or 9.0 Vdc) (V _O = 1.5 or 13.5 Vdc)	V _{IH}	5.0	3.85	—	3.75	2.75	—	3.75	—	Vdc
			10	7.6	—	7.5	5.50	—	7.5	—	
			15	12.1	—	12	8.25	—	12	—	
Output Drive Current Source (V _{OH} = 2.5 Vdc) (V _{OH} = 4.6 Vdc) (V _{OH} = 9.5 Vdc) (V _{OH} = 13.5 Vdc)	I _{OH}	5.0	-3.0	—	-2.4	-4.2	—	-1.7	—	mAdc	
		5.0	-0.64	—	-0.51	-0.88	—	-0.36	—		
		10	-1.6	—	-1.3	-2.25	—	-0.9	—		
	Sink (V _{OL} = 0.4 Vdc) (V _{OL} = 0.5 Vdc) (V _{OL} = 1.5 Vdc)	I _{OL}	5.0	0.64	—	0.51	0.88	—	0.36	—	mAdc
			10	1.6	—	1.3	2.25	—	0.9	—	
			15	4.2	—	3.4	8.8	—	2.4	—	
Input Current	I _{in}	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	μAdc	
Input Capacitance (V _{in} = 0)	C _{in}	—	—	—	—	5.0	7.5	—	—	pF	
Quiescent Current (Per Package)	I _{DD}	5.0	—	0.25	—	0.0005	0.25	—	7.5	μAdc	
		10	—	0.5	—	0.0010	0.5	—	15		
		15	—	1.0	—	0.0015	1.0	—	30		
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C _L = 50 pF on all outputs, all buffers switching)	I _T	5.0	I _T = (0.75 μA/kHz) f + I _{DD}							μAdc	
		10	I _T = (1.50 μA/kHz) f + I _{DD}								
		15	I _T = (2.25 μA/kHz) f + I _{DD}								

#Data labeled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

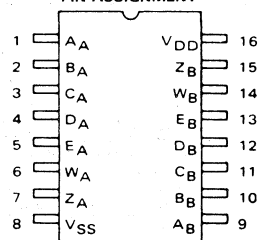
**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) V/k$$

where: I_T is in μA (per package), C_L in pF, V = (V_{DD} - V_{SS}) in volts, f in kHz is input frequency, and k = 0.002.

PIN ASSIGNMENT



MC14530B

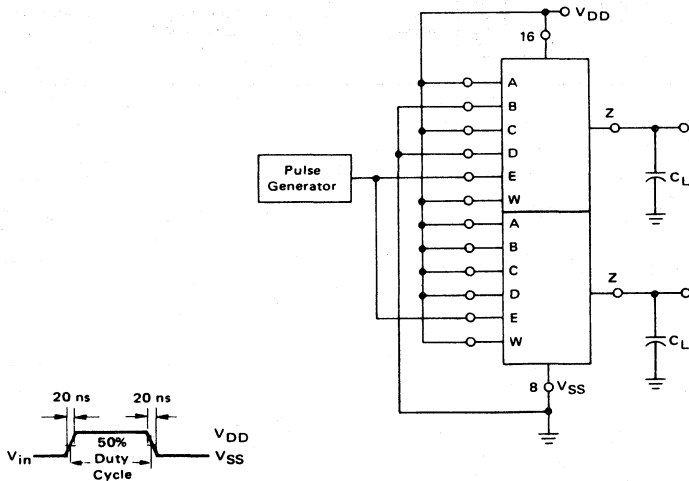
SWITCHING CHARACTERISTICS* ($C_L = 50 \text{ pF}$, $T_A = 25^\circ\text{C}$)

Characteristic	Symbol	VDD	Min	Typ #	Max	Unit
Output Rise and Fall Time $t_{TLH}, t_{THL} = (1.5 \text{ ns/pF}) C_L + 25 \text{ ns}$ $t_{TLH}, t_{THL} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$ $t_{TLH}, t_{THL} = (0.55 \text{ ns/pF}) C_L + 9.5 \text{ ns}$	t_{TLH}, t_{THL}	5.0 10 15	— — —	100 50 40	200 100 80	ns
Propagation Delay Time A, C, W = VDD; B, E = Gnd; D = Pulse Generator $t_{PLH} = (1.7 \text{ ns/pF}) C_L + 290 \text{ ns}$ $t_{PLH} = (0.66 \text{ ns/pF}) C_L + 127 \text{ ns}$ $t_{PLH} = (0.5 \text{ ns/pF}) C_L + 85 \text{ ns}$ $t_{PHL} = (1.7 \text{ ns/pF}) C_L + 345 \text{ ns}$ $t_{PHL} = (0.66 \text{ ns/pF}) C_L + 162 \text{ ns}$ $t_{PHL} = (0.5 \text{ ns/pF}) C_L + 95 \text{ ns}$	t_{PLH} t_{PHL}	5.0 10 15 5.0 10 15	— — — — — — —	375 160 110 430 195 120	960 400 300 1200 540 410	ns ns ns
A, B, C, D, E = Pulse Generator; W = VDD $t_{PLH} = (1.7 \text{ ns/pF}) C_L + 170 \text{ ns}$ $t_{PLH} = (0.66 \text{ ns/pF}) C_L + 87 \text{ ns}$ $t_{PLH} = (0.5 \text{ ns/pF}) C_L + 60 \text{ ns}$ $t_{PHL} = (1.7 \text{ ns/pF}) C_L + 195 \text{ ns}$ $t_{PHL} = (0.66 \text{ ns/pF}) C_L + 92 \text{ ns}$ $t_{PHL} = (0.5 \text{ ns/pF}) C_L + 75 \text{ ns}$	t_{PLH} t_{PHL}	5.0 10 15 5.0 10 15	— — — — — — —	255 120 85 280 125 100	640 300 210 750 330 250	ns ns ns
A, B, C, D, E = Gnd; W = Pulse Generator $t_{PHL}, t_{PLH} = (1.7 \text{ ns/pF}) C_L + 145 \text{ ns}$ $t_{PHL}, t_{PLH} = (0.66 \text{ ns/pF}) C_L + 72 \text{ ns}$ $t_{PHL}, t_{PLH} = (0.5 \text{ ns/pF}) C_L + 50 \text{ ns}$	t_{PLH}, t_{PHL}	5.0 10 15	— — —	230 105 75	575 265 190	ns

*The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

FIGURE 1 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM



MC14530B

SEQUENTIAL LOGIC APPLICATIONS

COINCIDENT FLIP-FLOP

x	y	Q_{n+1}
0	0	0
0	1	0
1	0	0
1	1	1

A flip-flop that will change only when both inputs agree.

ASTABLE MULTIVIBRATOR

x	y	Q_{n+1}
0	0	1
0	1	2τ
1	0	2τ
1	1	0

A flip-flop with three output conditions, where the third state is in oscillation between "1" and "0". The period of oscillation is twice the delay of the gate and the feedback element.

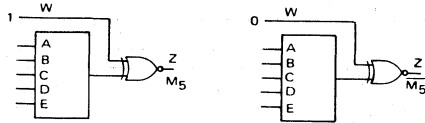
COINCIDENT FLIP-FLOP

x	y	z	Q_{n+1}
0	0	0	0
0	0	1	Q_n
0	1	0	Q_n
0	1	1	Q_n
1	0	0	Q_n
1	0	1	Q_n
1	1	0	Q_n
1	1	1	1

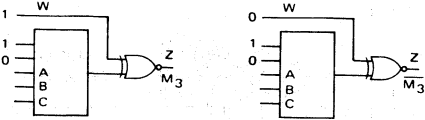
The flip-flop changes state only when all "1's" or all "0's" are entered. This configuration may be extended by cascading M_5 gates to cover n-inputs where all inputs must be "1's" or "0's" before the output will change. As an example, this configuration is useful for controlling an n-stage up/down counter that is to cycle from a minimum to maximum count and back again without flipping over (from all "1's" to all "0's".)

MC14530B

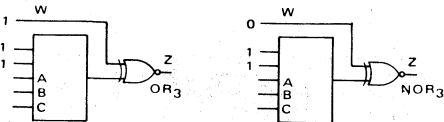
BASIC COMBINATIONAL FUNCTIONS



5-Input Majority Gates

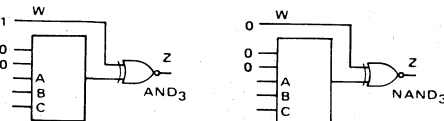


3-Input Majority Gates



3-Input OR Gate

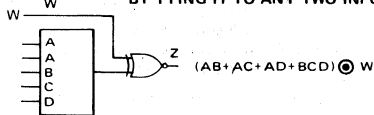
3-Input NOR Gate



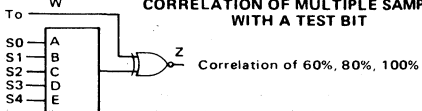
3-Input AND Gate

3-Input NAND Gate

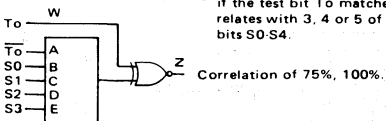
DOUBLING THE WEIGHT OF INPUT VARIABLE A BY TYING IT TO ANY TWO INPUTS



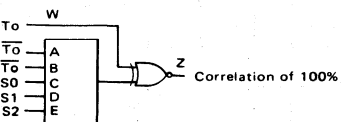
CORRELATION OF MULTIPLE SAMPLES WITH A TEST BIT



Correlation of 60%, 80%, 100%



Correlation of 75%, 100%



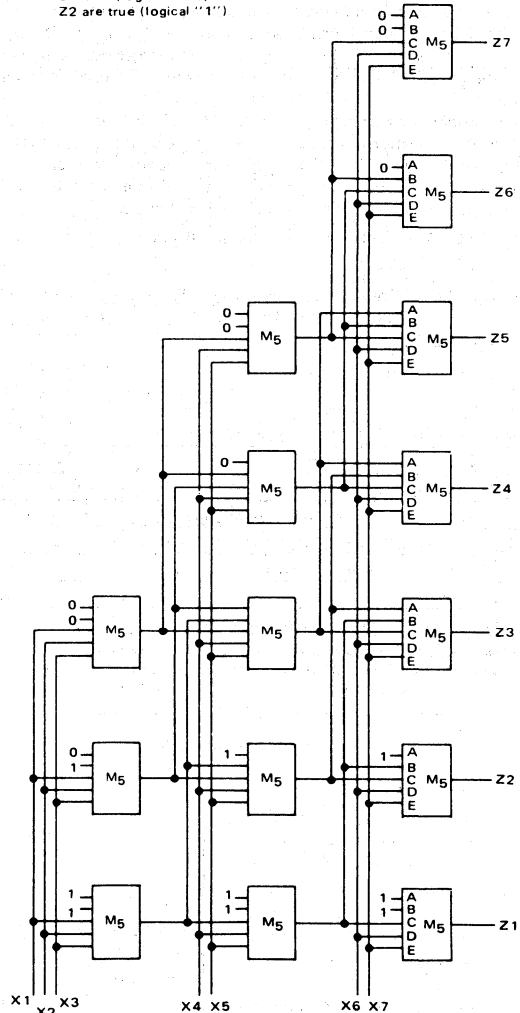
Correlation of 100%

5-INPUT MAJORITY LOGIC GATE APPLICATIONS

Each package labeled M₅ is a single majority logic gate using five inputs, A thru E, and one output Z.

- Majority Logic Gate Array yielding the symmetric function of 1 thru 7 variables true, out of 7 input variables (X₁ ... X₇)

(e.g., if any two input variables are true (logical "1"), Z₁ and Z₂ are true (logical "1"))





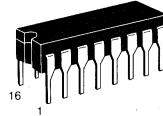
MOTOROLA

MC14531B

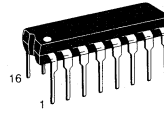
12-BIT PARITY TREE

The MC14531B 12-bit parity tree is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. The circuit consists of 12 data-bit inputs (D0 thru D11), and even or odd parity selection input (W) and an output (Q). The parity selection input can be considered as an additional bit. Words of less than 13 bits can generate an even or odd parity output if the remaining inputs are selected to contain an even or odd number of ones, respectively. Words of greater than 12-bits can be accommodated by cascading other MC14531B devices by using the W input. Applications include checking or including a redundant (parity) bit to a word for error detection/correction systems, controller for remote digital sensors or switches (digital event detection/correction), or as a multiple input summer without carries.

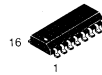
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- All Outputs Buffered
- Capable of Driving Two Low-Power TTL Loads or One Low-Power Schottky TTL Load Over the Rated Temperature Range
- Variable Word Length
- Diode Protection on All Inputs



L SUFFIX
CERAMIC
CASE 620



P SUFFIX
PLASTIC
CASE 648



D SUFFIX
SOIC
CASE 751B

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V _{DD}	DC Supply Voltage	-0.5 to +18.0	V
V _{in} , V _{out}	Input or Output Voltage (DC or Transient)	-0.5 to V _{DD} + 0.5	V
I _{in} , I _{out}	Input or Output Current (DC or Transient), per Pin	± 10	mA
P _D	Power Dissipation, per Package†	500	mW
T _{stg}	Storage Temperature	-65 to +150	°C
T _L	Lead Temperature (8-Second Soldering)	260	°C

ORDERING INFORMATION

- MC14XXBCP Plastic
- MC14XXBCL Ceramic
- MC14XXBD SOIC

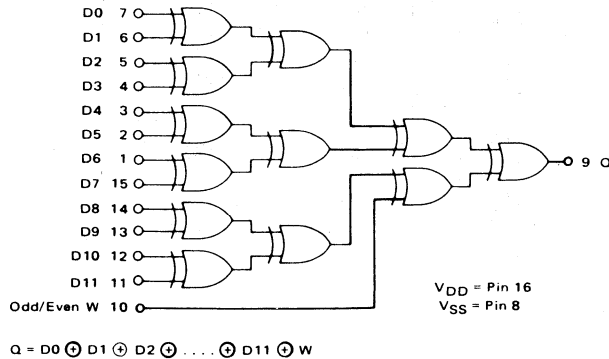
T_A = -55° to 125°C for all packages.

6

*Maximum Ratings are those values beyond which damage to the device may occur.

†Temperature Derating: Plastic "P and D/DW" Packages: -7.0 mW/°C From 65°C To 125°C
Ceramic "L" Packages: -12 mW/°C From 100°C To 125°C

LOGIC DIAGRAM



TRUTH TABLE

INPUTS								OUTPUT
W	D11	D10	...	D2	D1	D0	DECIMAL (OCTAL) EQUIVALENT	Q*
0	0	0	...	0	0	0	0 (0)	0
0	0	0	...	0	0	1	1 (1)	1
0	0	0	...	0	1	0	2 (2)	1
0	0	0	...	0	1	1	3 (3)	0
0	0	0	...	1	0	0	4 (4)	1
0	0	0	...	1	0	1	5 (5)	0
0	0	0	...	1	1	0	6 (6)	1
0	0	0	...	1	1	1	7 (7)	0
...
1	1	1	...	0	0	0	8184 (17770)	0
1	1	1	...	0	0	1	8185 (17771)	1
1	1	1	...	0	1	0	8186 (17772)	1
1	1	1	...	0	1	1	8187 (17773)	0
1	1	1	...	1	0	0	8188 (17774)	1
1	1	1	...	1	0	1	8189 (17775)	0
1	1	1	...	1	1	0	8190 (17776)	0
1	1	1	...	1	1	1	8191 (17777)	1

0 = Even Parity Note: May redefine to suit application by manipulating W and/or other available D's
1 = Odd Parity

MC14531B

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V _{DD} Vdc	-55°C		25°C			125°C		Unit	
			Min	Max	Min	Typ #	Max	Min	Max		
Output Voltage V _{in} = V _{DD} or 0	V _{OL}	5.0	—	0.05	—	0	0.05	—	0.05	Vdc	
		10	—	0.05	—	0	0.05	—	0.05		
		15	—	0.05	—	0	0.05	—	0.05		
	V _{in} = 0 or V _{DD}	V _{OH}	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc
			10	9.95	—	9.95	10	—	9.95	—	
			15	14.95	—	14.95	15	—	14.95	—	
Input Voltage (V _O = 4.5 or 0.5 Vdc) (V _O = 9.0 or 1.0 Vdc) (V _O = 13.5 or 1.5 Vdc)	V _{IL}	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc	
		10	—	3.0	—	4.50	3.0	—	3.0		
		15	—	4.0	—	6.75	4.0	—	4.0		
	V _{in} = 0 or V _{DD}	V _{IH}	5.0	3.5	—	3.5	2.75	—	3.5	—	Vdc
			10	7.0	—	7.0	5.50	—	7.0	—	
			15	11	—	11	8.25	—	11	—	
Output Drive Current (V _{OH} = 2.5 Vdc) (V _{OH} = 4.6 Vdc) (V _{OH} = 9.5 Vdc) (V _{OH} = 13.5 Vdc)	Source I _{OH}	5.0	-3.0	—	-2.4	-4.2	—	-1.7	—	mAdc	
		5.0	-0.64	—	-0.51	-0.88	—	-0.36	—		
		10	-1.6	—	-1.3	-2.25	—	-0.9	—		
	Sink I _{OL}	5.0	0.64	—	0.51	0.88	—	0.36	—	mAdc	
		10	1.6	—	1.3	2.25	—	0.9	—		
		15	4.2	—	3.4	8.8	—	2.4	—		
Input Current	I _{in}	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	μAdc	
Input Capacitance (V _{in} = 0)	C _{in}	—	—	—	—	5.0	7.5	—	—	pF	
Quiescent Current (Per Package)	I _{DD}	5.0	—	5.0	—	0.005	5.0	—	150	μAdc	
		10	—	10	—	0.010	10	—	300		
		15	—	20	—	0.015	20	—	600		
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C _L = 50 pF on all outputs, all buffers switching)	I _T	5.0	I _T = (0.25 μA/kHz) f + I _{DD}							μAdc	
		10	I _T = (0.50 μA/kHz) f + I _{DD}								
		15	I _T = (0.75 μA/kHz) f + I _{DD}								

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C.

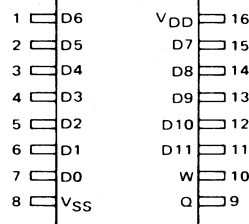
†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) V/k$$

where: I_T is in μA (per package), C_L in pF, V = (V_{DD} - V_{SS}) in volts, f in kHz is input frequency, and k = 0.001.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range V_{SS} ≤ (V_{in} or V_{out}) ≤ V_{DD}. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

PIN ASSIGNMENT



MC14531B

SWITCHING CHARACTERISTICS* ($C_L = 50 \text{ pF}$, $T_A = 25^\circ\text{C}$)

Characteristic	Symbol	V _{DD}	Min	Typ #	Max	Unit
Output Rise and Fall Time	t_{TLH} , t_{THL}					ns
t_{TLH} , $t_{THL} = (1.5 \text{ ns/pF}) C_L + 25 \text{ ns}$		5.0	—	100	200	
t_{TLH} , $t_{THL} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$		10	—	50	100	
t_{TLH} , $t_{THL} = (0.55 \text{ ns/pF}) C_L + 9.5 \text{ ns}$		15	—	40	80	
Propagation Delay Time	t_{PLH} , t_{PHL}					ns
Data to Q						
t_{PLH} , $t_{PHL} = (1.7 \text{ ns/pF}) C_L + 355 \text{ ns}$		5.0	—	440	1320	
t_{PLH} , $t_{PHL} = (0.66 \text{ ns/pF}) C_L + 142 \text{ ns}$		10	—	175	525	
t_{PLH} , $t_{PHL} = (0.5 \text{ ns/pF}) C_L + 95 \text{ ns}$		15	—	120	360	
Odd/Even to Q						
t_{PLH} , $t_{PHL} = (1.7 \text{ ns/pF}) C_L + 165 \text{ ns}$		5.0	—	250	750	
t_{PLH} , $t_{PHL} = (0.66 \text{ ns/pF}) C_L + 67 \text{ ns}$		10	—	100	300	
t_{PLH} , $t_{PHL} = (0.5 \text{ ns/pF}) C_L + 45 \text{ ns}$		15	—	70	210	

*The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

FIGURE 1 – DYNAMIC POWER DISSIPATION SIGNAL WAVEFORM

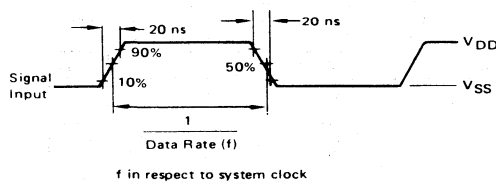
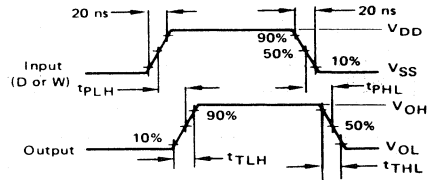


FIGURE 2 – DYNAMIC SIGNAL WAVEFORMS





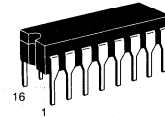
MOTOROLA

MC14532B

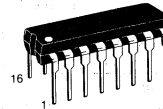
8-BIT PRIORITY ENCODER

The MC14532B is constructed with complementary MOS (CMOS) enhancement mode devices. The primary function of a priority encoder is to provide a binary address for the active input with the highest priority. Eight data inputs (D0 thru D7) and an enable input (E_{in}) are provided. Five outputs are available, three are address outputs (Q0 thru Q2), one group select (GS) and one enable output (E_{out}).

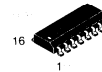
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-Power Schottky TTL Load over the Rated Temperature Range



**L SUFFIX
CERAMIC
CASE 620**



**P SUFFIX
PLASTIC
CASE 648**



**D SUFFIX
SOIC
CASE 751B**

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V _{DD}	DC Supply Voltage	-0.5 to +18.0	V
V _{in} , V _{out}	Input or Output Voltage (DC or Transient)	-0.5 to V _{DD} + 0.5	V
I _{in} , I _{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
P _D	Power Dissipation, per Package†	500	mW
T _{stg}	Storage Temperature	-65 to +150	°C
T _L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P and D/DW" Packages: -7.0 mW/°C From 65°C To 125°C
Ceramic "L" Packages: -12 mW/°C From 100°C To 125°C

ORDERING INFORMATION

MC14XXXBCP Plastic
MC14XXXBCL Ceramic
MC14XXXBD SOIC

T_A = -55° to 125°C for all packages.

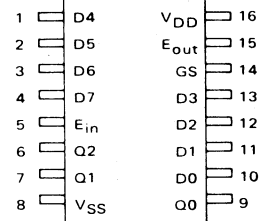
TRUTH TABLE

INPUT									OUTPUT				
E _{in}	D7	D6	D5	D4	D3	D2	D1	D0	GS	Q2	Q1	Q0	E _{out}
0	X	X	X	X	X	X	X	X	0	0	0	0	0
1	X	0	0	0	0	0	X	X	0	0	0	0	1
1	1	X	X	X	X	X	X	X	1	1	1	1	0
1	0	1	X	X	X	X	X	X	1	1	1	0	0
1	0	0	1	X	X	X	X	X	1	1	0	1	0
1	0	0	0	1	X	X	X	X	1	1	0	0	0
1	0	0	0	0	1	X	X	X	1	0	1	1	0
1	0	0	0	0	0	1	X	X	1	0	0	1	0
1	0	0	0	0	0	0	1	X	1	0	0	1	0
1	0	0	0	0	0	0	0	1	1	0	0	0	0

X = Don't Care

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range V_{SS} ≤ (V_{in} or V_{out}) ≤ V_{DD}. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

PIN ASSIGNMENT



MC14532B

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V _{DD} Vdc	-55°C		25°C			125°C		Unit	
			Min	Max	Min	Typ #	Max	Min	Max		
Output Voltage V _{in} = V _{DD} or 0	V _{OL}	5.0	—	0.05	—	0	0.05	—	0.05	Vdc	
		10	—	0.05	—	0	0.05	—	0.05		
15		—	0.05	—	0	0.05	—	0.05			
V _{in} = 0 or V _{DD}	V _{OH}	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc	
		10	9.95	—	9.95	10	—	9.95	—		
		15	14.95	—	14.95	15	—	14.95	—		
Input Voltage (V _O = 4.5 or 0.5 Vdc) (V _O = 9.0 or 1.0 Vdc) (V _O = 13.5 or 1.5 Vdc)	V _{IL}	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc	
		10	—	3.0	—	4.50	3.0	—	3.0		
		15	—	4.0	—	6.75	4.0	—	4.0		
(V _O = 0.5 or 4.5 Vdc) (V _O = 1.0 or 9.0 Vdc) (V _O = 1.5 or 13.5 Vdc)	V _{IH}	5.0	3.5	—	3.5	2.75	—	3.5	—	Vdc	
		10	7.0	—	7.0	5.50	—	7.0	—		
		15	11	—	11	8.25	—	11	—		
Output Drive Current (V _{OH} = 2.5 Vdc) (V _{OH} = 4.6 Vdc) (V _{OH} = 9.5 Vdc) (V _{OH} = 13.5 Vdc)	Source	I _{OH}	5.0	-3.0	—	-2.4	-4.2	—	-1.7	—	mAdc
			10	-0.64	—	-0.51	-0.88	—	-0.36	—	
			15	-1.6	—	-1.3	-2.25	—	-0.9	—	
	Sink	I _{OL}	5.0	0.64	—	0.51	0.88	—	0.36	—	mAdc
			10	1.6	—	1.3	2.25	—	0.9	—	
			15	4.2	—	3.4	8.8	—	2.4	—	
Input Current	I _{in}	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	μAdc	
Input Capacitance (V _{in} = 0)	C _{in}	—	—	—	—	5.0	7.5	—	—	pF	
Quiescent Current (Per Package)	I _{DD}	5.0	—	5.0	—	0.005	5.0	—	150	μAdc	
		10	—	10	—	0.010	10	—	300		
		15	—	20	—	0.015	20	—	600		
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C _L = 50 pF on all outputs, all buffers switching)	I _T	5.0	I _T = (1.74 μA/kHz) f + I _{DD}							μAdc	
		10	I _T = (3.65 μA/kHz) f + I _{DD}								
		15	I _T = (5.73 μA/kHz) f + I _{DD}								

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) V f k$$

where: I_T is in μA (per package), C_L in pF, V = (V_{DD} - V_{SS}) in volts, f in kHz is input frequency, and k = 0.005.

MC14532B

SWITCHING CHARACTERISTICS* ($C_L = 50 \text{ pF}$, $T_A = 25^\circ\text{C}$)

Characteristic	Symbol	V _{DD}	Min	Typ #	Max	Unit
Output Rise and Fall Time $t_{TLH}, t_{THL} = (1.5 \text{ ns/pF}) C_L + 25 \text{ ns}$ $t_{TLH}, t_{THL} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$ $t_{TLH}, t_{THL} = (0.55 \text{ ns/pF}) C_L + 9.5 \text{ ns}$	t_{TLH} , t_{THL}	5.0 10 15	— — —	100 50 40	200 100 80	ns
Propagation Delay Time – E _{in} to E _{out} $t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 120 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 77 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 55 \text{ ns}$	t_{PLH} , t_{PHL}	5.0 10 15	— — —	205 110 80	410 220 160	ns
Propagation Delay Time (E _{in} to G _S) $t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 90 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 57 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 40 \text{ ns}$	t_{PLH} , t_{PHL}	5.0 10 15	— — —	175 90 65	350 180 130	ns
Propagation Delay Time – E _{in} to Q _n $t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 195 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 107 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 75 \text{ ns}$	t_{PHL} , t_{PLH}	5.0 10 15	— — —	280 140 100	560 280 200	ns
Propagation Delay Time – D _n to Q _n $t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 265 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 137 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 85 \text{ ns}$	t_{PLH} , t_{PHL}	5.0 10 15	— — —	300 170 110	600 340 220	ns
Propagation Delay Time – D _n to G _S $t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 195 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 107 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 75 \text{ ns}$	t_{PLH} , t_{PHL}	5.0 10 15	— — —	280 140 100	560 280 200	ns

*The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

FIGURE 1 – TYPICAL SINK AND SOURCE CURRENT CHARACTERISTICS

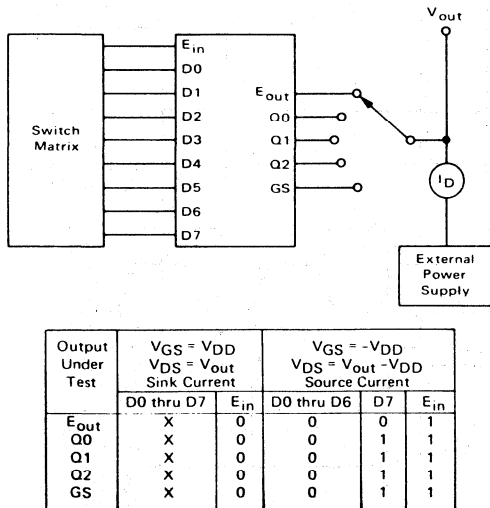
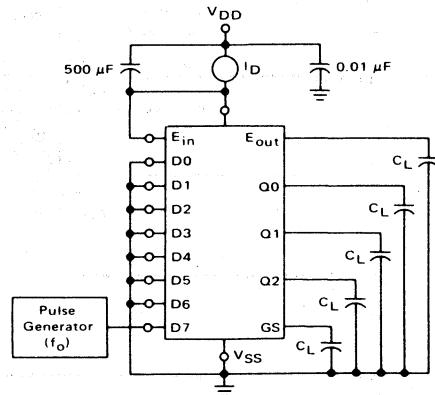
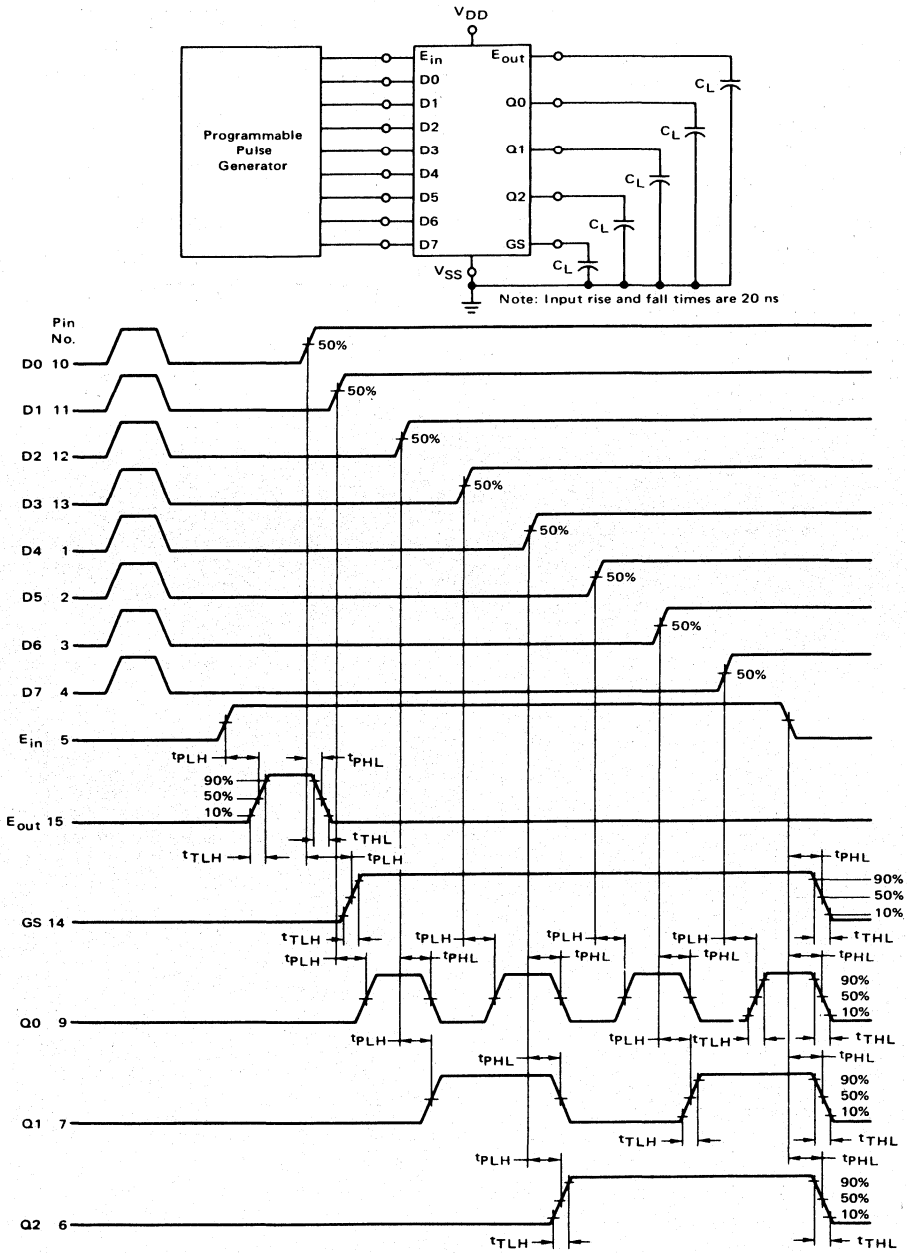


FIGURE 2 – TYPICAL POWER DISSIPATION TEST CIRCUIT



MC14532B

FIGURE 3 – AC TEST CIRCUIT AND WAVEFORMS



6

MC14532B

LOGIC DIAGRAM (Positive Logic)

LOGIC EQUATIONS

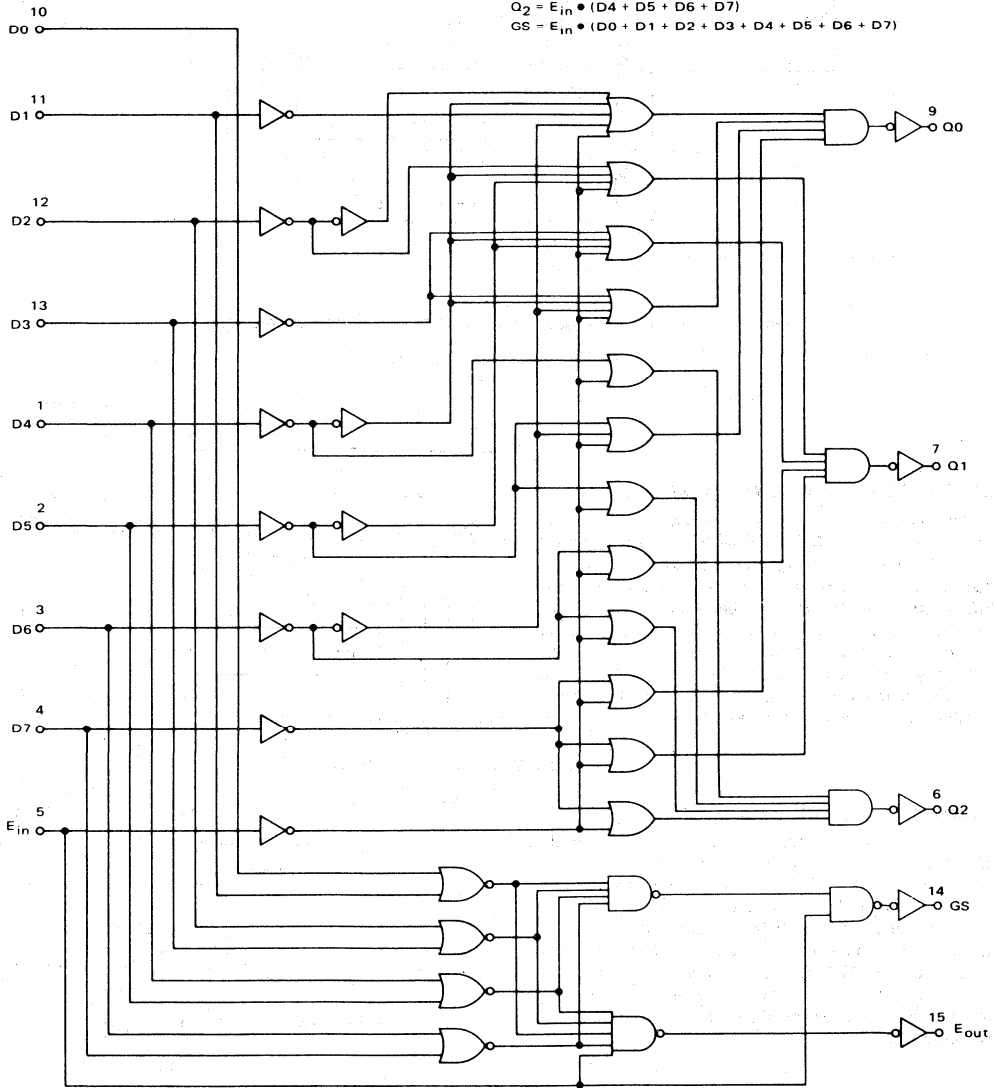
$$E_{out} = E_{in} \bullet \bar{D0} \bullet \bar{D1} \bullet \bar{D2} \bullet \bar{D3} \bullet \bar{D4} \bullet \bar{D5} \bullet \bar{D6} \bullet \bar{D7}$$

$$Q0 = E_{in} \bullet (D1 \bullet \bar{D2} \bullet \bar{D4} \bullet \bar{D6} + D3 \bullet \bar{D4} \bullet \bar{D6} + D5 \bullet \bar{D6} + D7)$$

$$Q1 = E_{in} \bullet (D2 \bullet \bar{D4} \bullet \bar{D5} + D3 \bullet \bar{D4} \bullet \bar{D5} + D6 + D7)$$

$$Q2 = E_{in} \bullet (D4 + D5 + D6 + D7)$$

$$GS = E_{in} \bullet (D0 + D1 + D2 + D3 + D4 + D5 + D6 + D7)$$



MC14532B

FIGURE 4 – TWO MC14532B's CASCADED FOR 4-BIT OUTPUT

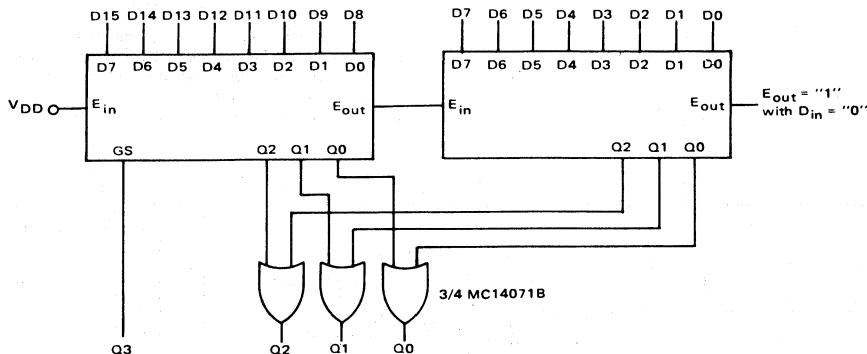


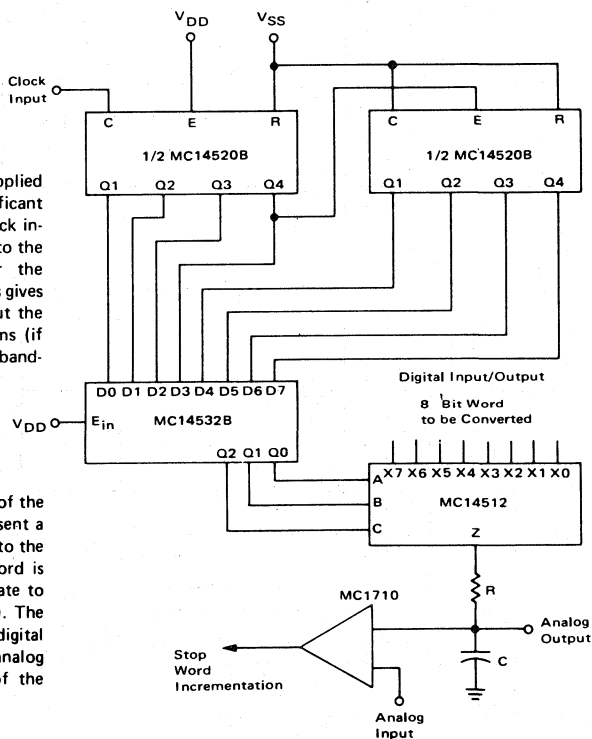
FIGURE 5 – DIGITAL TO ANALOG AND ANALOG TO DIGITAL CONVERTER

DIGITAL TO ANALOG CONVERSION

The digital eight-bit word to be converted is applied to the inputs of the MC14512 with the most significant bit at X7 and the least significant bit at X0. A clock input of up to 2.5 MHz (at $V_{DD} = 10\text{ V}$) is applied to the MC14520B. A compromise between I_{bias} for the MC1710 and ΔR between N and P-channel outputs gives a value of R of 33 k ohms. In order to filter out the switching frequencies, RC should be about 1.0 ms (if $R = 33\text{ k ohms}$, $C \approx 0.03\text{ }\mu\text{F}$). The analog 3.0 dB bandwidth would then be dc to 1.0 kHz.

ANALOG TO DIGITAL CONVERSION

An analog signal is applied to the analog input of the MC1710. A digital eight-bit word known to represent a digitized level less than the analog input is applied to the MC14512 as in the D to A conversion. The word is incremented at rates sufficient to allow steady state to be reached between incrementations (i.e. 3.0 ms). The output of the MC1710 will change when the digital input represents the first digitized level above the analog input. This word is the digital representation of the analog word.





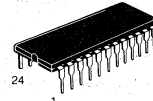
MOTOROLA

MC14534B

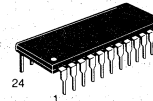
5 CASCADED BCD COUNTERS

The MC14534B is composed of five BCD ripple counters that have their respective outputs multiplexed using an internal scanner. Outputs of each counter are selected by the scanner and appear on four (BCD) pins. Selection is indicated by a logic high on the appropriate digit select pin. Both BCD and digit select outputs have three-state controls providing an "open-circuit" when these controls are high and allowing multiplexing. Cascading may be accomplished by using the carry-out pin. The counters and scanner can be independently reset by applying a high to the counter master reset (MR) and the scanner reset (SR). The MC14534B was specifically designed for application in real time or event counters where continual updating and multiplexed displays are used.

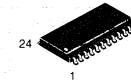
- Four Operating Modes (See truth table)
- Input Error Detection Circuit
- Clock Conditioning Circuits for Slow Transition Inputs
- Counter Sequences on Positive Transition of Clock A
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range



L SUFFIX
CERAMIC
CASE 623



P SUFFIX
PLASTIC
CASE 709



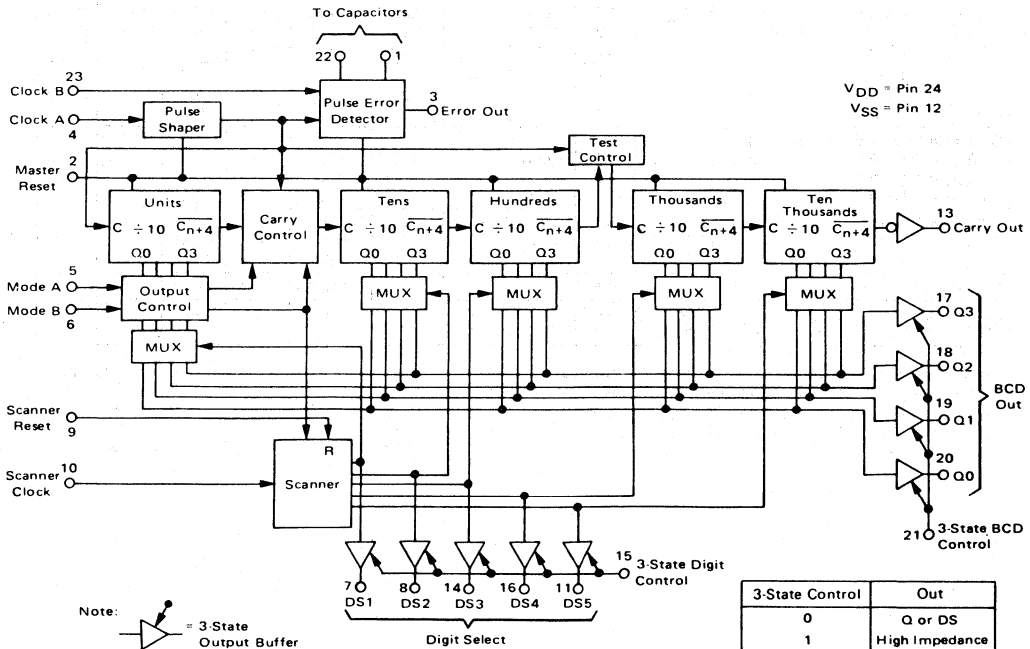
DW SUFFIX
SOIC
CASE 751E

ORDERING INFORMATION

MC14XXXBCP Plastic
MC14XXXBCL Ceramic
MC14XXXBDW SOIC

T_A = -55° to 125°C for all packages.

BLOCK DIAGRAM



MC14534B

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	-0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	-0.5 to $V_{DD} + 0.5$	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	± 10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

*Maximum Ratings are those values beyond which damage to the device may occur.

†Temperature Derating: Plastic "P and D/DW" Packages: -7.0 mW/°C From 65°C To 125°C
Ceramic "L" Packages: -12 mW/°C From 100°C To 125°C

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	-55°C		25°C			125°C		Unit	
			Min	Max	Min	Typ #	Max	Min	Max		
Output Voltage $V_{in} = V_{DD}$ or 0	V_{OL}	5.0	—	0.05	—	0	0.05	—	0.05	Vdc	
		10	—	0.05	—	0	0.05	—	0.05		
		15	—	0.05	—	0	0.05	—	0.05		
	$V_{in} = 0$ or V_{DD}	V_{OH}	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc
			10	9.95	—	9.95	10	—	9.95	—	
			15	14.95	—	14.95	15	—	14.95	—	
Input Voltage ($V_O = 4.5$ or 0.5 Vdc) ($V_O = 9.0$ or 1.0 Vdc) ($V_O = 13.5$ or 1.5 Vdc)	V_{IL}	5.0	—	1.0	—	1.5	1.0	—	1.0	Vdc	
		10	—	2.0	—	3.0	2.0	—	2.0		
		15	—	3.0	—	4.5	3.0	—	3.0		
	V_{IH}	5.0	4.0	—	4.0	3.5	—	4.0	—	Vdc	
		10	8.0	—	8.0	7.0	—	8.0	—		
		15	12	—	12	11	—	12	—		
Output Drive Current ($V_{OH} = 2.5$ Vdc) ($V_{OH} = 4.6$ Vdc) ($V_{OH} = 9.5$ Vdc) ($V_{OH} = 13.5$ Vdc)	Source	I_{OH}	5.0	-3.0	—	-2.4	-4.2	—	-1.7	—	mAdc
			10	-0.64	—	-0.51	-0.88	—	-0.36	—	
			15	-1.6	—	-1.3	-2.25	—	-0.9	—	
	Sink	I_{OL}	5.0	0.64	—	0.51	0.88	—	0.36	—	mAdc
			10	1.6	—	1.3	2.25	—	0.9	—	
			15	4.2	—	3.4	8.8	—	2.4	—	
Output Drive Current — Pins 1 and 22 ($V_{OH} = 2.5$ Vdc) ($V_{OH} = 9.5$ Vdc) ($V_{OH} = 13.5$ Vdc)	Source	I_{OH}	5.0	-0.31	—	-0.25	-0.8	—	-0.17	—	mAdc
			10	-0.31	—	-0.25	-0.4	—	-0.17	—	
			15	-0.9	—	-0.75	-1.6	—	-0.51	—	
	Sink	I_{OL}	5.0	0.024	—	0.02	0.03	—	0.014	—	mAdc
			10	0.06	—	0.05	0.09	—	0.035	—	
			15	1.3	—	0.25	1.63	—	0.175	—	
Input Current	I_{in}	15	—	± 0.1	—	± 0.00001	± 0.1	—	± 1.0	μ Adc	
Input Capacitance ($V_{in} = 0$)	C_{in}	—	—	—	—	5.0	7.5	—	—	pF	

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

(continued)

MC14534B

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS}) (continued)

Characteristic	Symbol	V _{DD} V _{dC}	-55°C		25°C			125°C		Unit
			Min	Max	Min	Typ #	Max	Min	Max	
Quiescent Current (Per Package)	I _{DD}	5.0	—	5.0	—	0.010	5.0	—	150	μA _{dC}
		10	—	10	—	0.020	10	—	300	
		15	—	20	—	0.030	20	—	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C _L = 50 pF on all outputs, all buffers switching)	I _T	5.0	I _T = (0.5 μA/kHz) f + I _{DD} Scan Oscillator I _T = (1.0 μA/kHz) f + I _{DD} Frequency = 1.0 kHz I _T = (1.5 μA/kHz) f + I _{DD}							μA _{dC}
		10								
		15								
Three-State Leakage Current	I _{TL}	15	—	±0.1	—	±0.00001	±0.1	—	±3.0	μA _{dC}

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) Vfk$$

where: I_T is in μA (per package), C_L in pF, V = (V_{DD} - V_{SS}) in volts, f in kHz is input frequency, and k = 0.001.

MC14534B

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C, See Figure 1)

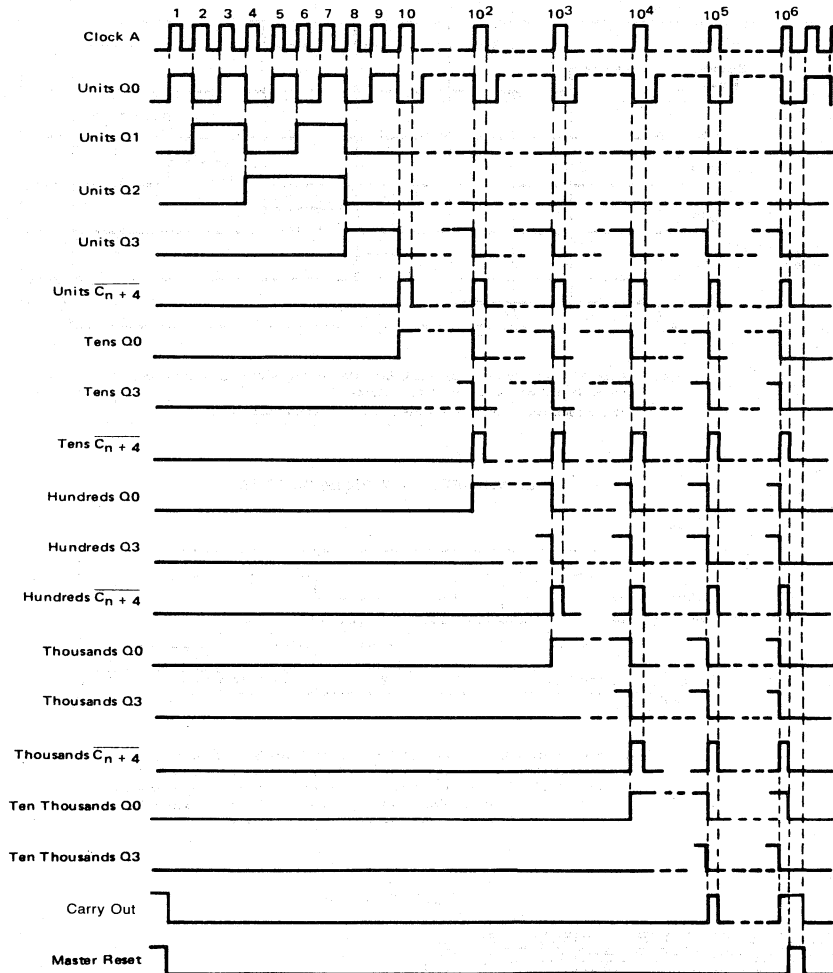
Characteristic	Symbol	V _{DD} Vdc	Min	Typ #	Max	Unit	
Output Rise and Fall Time	t _{TLH} , t _{THL}	5.0	—	100	200	ns	
		10	—	50	100		
		15	—	40	80		
Propagation Delay Time, Clock to Q t _{PLH} , t _{PHL} = (1.8 ns/pF) C _L + 4.0 μs t _{PLH} , t _{PHL} = (0.8 ns/pF) C _L + 1.5 μs t _{PLH} , t _{PHL} = (0.6 ns/pF) C _L + 1.0 μs Clock to Carry Out t _{PLH} = (1.8 ns/pF) C _L + 3.3 μs t _{PLH} = (0.8 ns/pF) C _L + 1.1 μs t _{PLH} = (0.6 ns/pF) C _L + 0.8 μs Master Reset to Q t _{PHL} = (1.8 ns/pF) C _L + 1.8 μs t _{PHL} = (0.8 ns/pF) C _L + 0.6 μs t _{PHL} = (0.6 ns/pF) C _L + 0.5 μs Master Reset to Error Out t _{PHL} = (1.8 ns/pF) C _L + 0.57 μs t _{PHL} = (0.8 ns/pF) C _L + 0.19 μs t _{PHL} = (0.6 ns/pF) C _L + 0.11 μs Scanner Clock to Q t _{PLH} , t _{PHL} = (1.8 ns/pF) C _L + 1.8 μs t _{PLH} , t _{PHL} = (0.8 ns/pF) C _L + 0.6 μs t _{PLH} , t _{PHL} = (0.6 ns/pF) C _L + 0.5 μs Scanner Clock to Digit Select t _{PLH} , t _{PLH} = (1.8 ns/pF) C _L + 1.5 μs t _{PHL} , t _{PLH} = (0.8 ns/pF) C _L + 0.5 μs t _{PHL} , t _{PLH} = (0.6 ns/pF) C _L + 0.4 μs	t _{PLH} , t _{PHL}	5.0	—	4.0	8.0	μs	
		10	—	1.5	3.0		
		15	—	1.0	2.25		
	t _{PLH}	t _{PLH}	5.0	—	3.3	6.6	μs
			10	—	1.1	2.2	
			15	—	0.8	1.7	
	t _{PHL}	t _{PHL}	5.0	—	1.8	3.6	μs
			10	—	0.6	1.2	
			15	—	0.5	0.9	
	t _{PHL}	t _{PHL}	5.0	—	0.6	1.5	μs
			10	—	0.2	.5	
			15	—	0.12	0.38	
t _{PLH} , t _{PHL}	t _{PLH} , t _{PHL}	5.0	—	1.8	3.6	μs	
		10	—	0.6	1.2		
		15	—	0.5	0.9		
t _{PLH} , t _{PLH}	t _{PLH} , t _{PLH}	5.0	—	1.5	3.0	μs	
		10	—	0.5	1.0		
		15	—	0.4	0.75		
Propagation Delay Time 3-State Control to Q	t _{PHZ}	5.0	—	75	150	ns	
		10	—	45	90		
		15	—	40	80		
	t _{PZH}	t _{PZH}	5.0	—	120	240	ns
			10	—	55	110	
			15	—	40	80	
	t _{PLZ}	t _{PLZ}	5.0	—	120	240	ns
			10	—	55	110	
			15	—	45	90	
	t _{PZL}	t _{PZL}	5.0	—	160	320	ns
			10	—	70	140	
			15	—	45	90	
Clock Pulse Frequency	f _{cl}	5.0	—	1.0	0.5	MHz	
		10	—	3.0	1.0		
		15	—	5.0	1.2		
Clock or Scanner Clock Pulse Width	t _{WH}	5.0	1000	500	—	ns	
		10	500	190	—		
		15	375	125	—		
Scanner Reset Pulse Width	t _w	5.0	320	160	—	ns	
		10	130	65	—		
		15	80	40	—		
Scanner Reset Removal Time	t _{rem}	5.0	900	270	—	ns	
		10	150	80	—		
		15	100	50	—		
Master Reset Pulse Width	t _{WH(R)}	5.0	2000	900	—	ns	
		10	600	300	—		
		15	450	250	—		
Master Reset Removal Time	t _{rem}	5.0	1060	550	—	ns	
		10	350	205	—		
		15	250	140	—		

*The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

MC14534B

COUNTER TIMING DIAGRAM

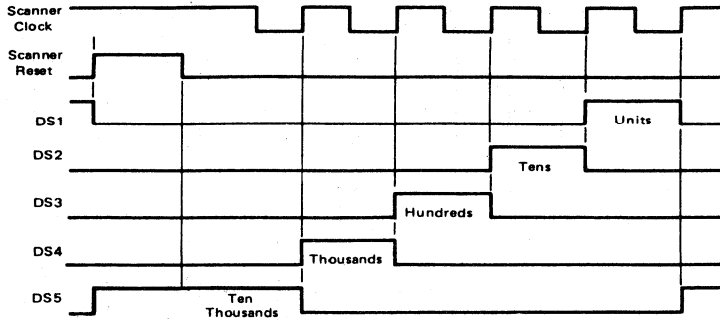


MODE CONTROL TRUTH TABLE

Mode A	Mode B	First Stage Output	Carry to Second Stage	Application
0	0	Normal Count and Display	At 9 to 0 transition of first stage	5-digit Counter
0	1	Inhibited	Input Clock	Test Mode: Clock directly into stages 1, 2, and 4.
1	1	Inhibited	At 4 to 5 transition of first stage	4 digit counter with : 10 and roundoff at front end.
1	0	Counts 3, 4, 5, 6, 7 = 5 Counts 8, 9, 0, 1, 2 = 0	At 7 to 8 transition of first stage	4-digit counter with 1/2 pence capability.

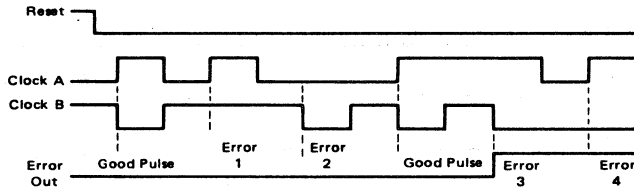
MC14534B

SCANNER TIMING DIAGRAM



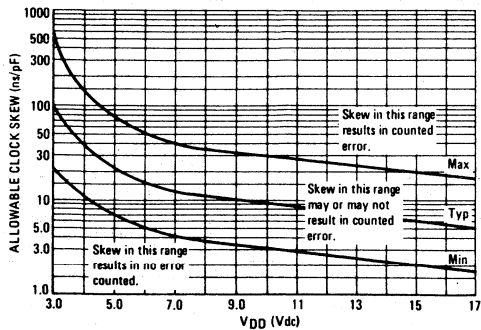
Note: If Mode B = 1, the first decade is inhibited and S1 will not go high, and the cycle will be shortened to four stages.
DS5 is selected automatically when Scanner Reset goes high.

ERROR DETECTION TIMING DIAGRAM



Note: Error detector looks for inverted pulse on Clock B. Whenever a positive edge at Clock A is not accompanied by a negative pulse at Clock B (or vice-versa) within a time period of the one-shots an error is counted. Three errors result in Error Out to go to a "1". If error detection is not needed, tie Clock B high or low and leave Pins 1 and 22 unconnected.

CLOCK SKEW RANGE



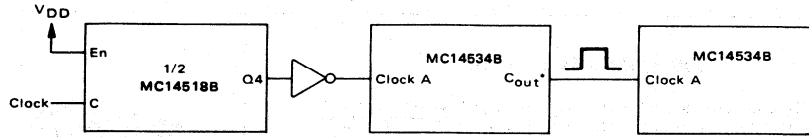
Notes:

1. The skew is the time difference between the low-to-high transition of C_A to the high-to-low transition of C_B or vice-versa. Capacitors $C1 = C22$ tied from pins 1 and 22 to V_{SS} .
2. This graph is accurate for $C1 = C22 \geq 100$ pF.
3. When the error detection circuitry is not used, pins 1 and 22 are left open.

MC14534B

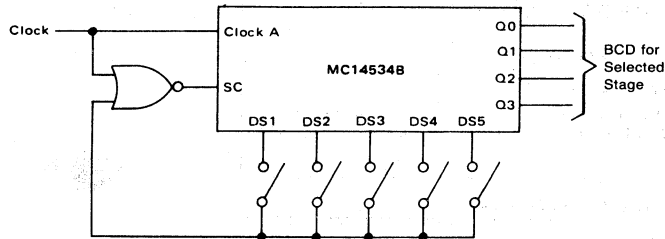
APPLICATIONS INFORMATION

FIGURE 1 – CASCADE OPERATION



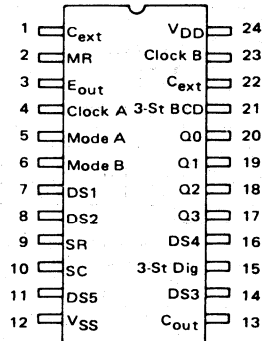
*Carry Out is high for a single clock period when all five BCD stages go to zero. (Carry Out also goes high when MR is applied.)

FIGURE 2 — FORCING A BCD STAGE TO THE Q OUTPUTS



When the Q outputs of a given stage are required, this configuration will lock up the selected stage within four clock cycles. The select line feedback may be hardwired or switched.

PIN ASSIGNMENT



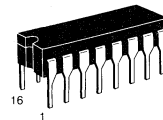


MC14536B

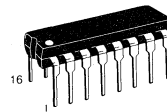
PROGRAMMABLE TIMER

The MC14536B programmable timer is a 24-stage binary ripple counter with 16 stages selectable by a binary code. Provisions for an on-chip RC oscillator or an external clock are provided. An on-chip monostable circuit incorporating a pulse-type output has been included. By selecting the appropriate counter stage in conjunction with the appropriate input clock frequency, a variety of timing can be achieved.

- 24 Flip-Flop Stages -- Will Count From 2^0 to 2^{24}
- Last 16 Stages Selectable By Four-Bit Select Code
- 8-Bypass Input Allows Bypassing of First Eight Stages
- Set and Reset Inputs
- Clock Inhibit and Oscillator Inhibit Inputs
- On-Chip RC Oscillator Provisions
- On-Chip Monostable Output Provisions
- Clock Conditioning Circuit Permits Operation With Very Long Rise and Fall Times
- Test Mode Allows Fast Test Sequence
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range



L SUFFIX
CERAMIC
CASE 620



P SUFFIX
PLASTIC
CASE 648



DW SUFFIX
SOIC
CASE 751G

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	-0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	-0.5 to $V_{DD} + 0.5$	V
i_{in}, i_{out}	Input or Output Current (DC or Transient), per Pin	± 10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.

†Temperature Derating: Plastic "P and D/DW" Packages: -7.0 mW/°C From 65°C To 125°C

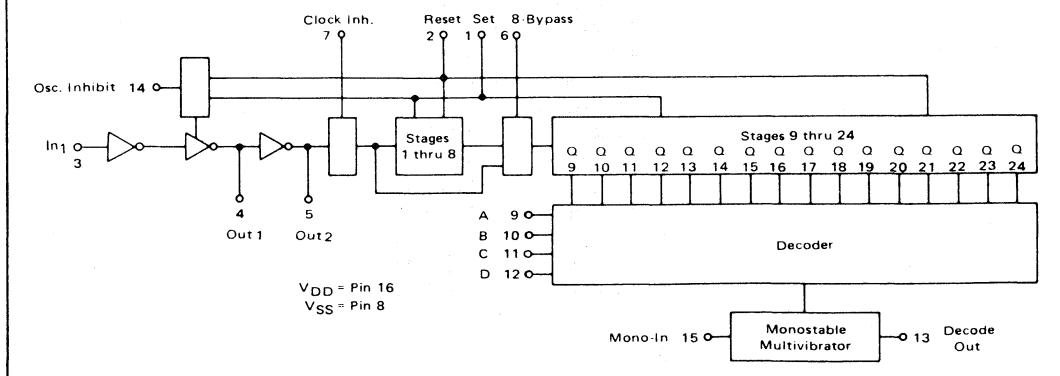
Ceramic "L" Packages: -12 mW/°C From 100°C To 125°C

ORDERING INFORMATION

MC14XXXBCP Plastic
MC14XXXBCL Ceramic
MC14XXXBDW SOIC

$T_A = -55^\circ$ to 125° C for all packages.

BLOCK DIAGRAM



MC14536B

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V _{DD} Vdc	-55°C		25°C			125°C		Unit
			Min	Max	Min	Typ #	Max	Min	Max	
Output Voltage V _{in} = V _{DD} or 0	V _{OL}	5.0 10 15	—	0.05	—	0	0.05	—	0.05	Vdc
			—	0.05	—	0	0.05	—	0.05	
—			0.05	—	0	0.05	—	0.05		
V _{in} = 0 or V _{DD}	V _{OH}	5.0 10 15	4.95	—	4.95	5.0	—	4.95	—	Vdc
			9.95	—	9.95	10	—	9.95	—	
			14.95	—	14.95	15	—	14.95	—	
Input Voltage (V _O = 4.5 or 0.5 Vdc) (V _O = 9.0 or 1.0 Vdc) (V _O = 13.5 or 1.5 Vdc)	V _{IL}	5.0 10 15	—	1.5	—	2.25	1.5	—	1.5	Vdc
			—	3.0	—	4.50	3.0	—	3.0	
—			4.0	—	6.75	4.0	—	4.0		
(V _O = 0.5 or 4.5 Vdc) (V _O = 1.0 or 9.0 Vdc) (V _O = 1.5 or 13.5 Vdc)	V _{IH}	5.0 10 15	3.5	—	3.5	2.75	—	3.5	—	Vdc
			7.0	—	7.0	5.50	—	7.0	—	
			11	—	11	8.25	—	11	—	
Output Drive Current (V _{OH} = 2.5 Vdc) (V _{OH} = 4.6 Vdc) (V _{OH} = 9.5 Vdc) (V _{OH} = 13.5 Vdc)	Source Pins 4 & 5	5.0 5.0 10 15	-1.2	—	-1.0	-1.7	—	-0.7	—	mAdc
			-0.25	—	-0.2	-0.36	—	-0.14	—	
			-0.62	—	-0.5	-0.9	—	-0.35	—	
			-1.8	—	-1.5	-3.5	—	-1.1	—	
	Source Pin 13	5.0 5.0 10 15	-3.0	—	-2.4	-4.2	—	-1.7	—	mAdc
			-0.64	—	-0.51	-0.88	—	-0.36	—	
			-1.6	—	-1.3	-2.25	—	-0.9	—	
	Sink	5.0 10 15	0.64	—	0.51	0.88	—	0.36	—	mAdc
			1.6	—	1.3	2.25	—	0.9	—	
4.2			—	3.4	8.8	—	2.4	—		
Input Current	I _{in}	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	μAdc
Input Capacitance (V _{in} = 0)	C _{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)	I _{DD}	5.0 10 15	—	5.0	—	0.010	5.0	—	150	μAdc
			—	10	—	0.020	10	—	300	
			—	20	—	0.030	20	—	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C _L = 50 pF on all outputs, all buffers switching)	I _T	5.0 10 15	I _T = (1.50 μA/kHz) f + I _{DD}						μAdc	
			I _T = (2.30 μA/kHz) f + I _{DD}							
			I _T = (3.55 μA/kHz) f + I _{DD}							

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) Vfk$$

where: I_T is in μA (per package), C_L in pF, V = (V_{DD} - V_{SS}) in volts, f in kHz is input frequency, and k = 0.003.

MC14536B

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V _{DD}	Min	Typ #	Max	Unit
Output Rise and Fall Time (Pin 13) t _{TLH} , t _{THL} = (1.5 ns/pF) C _L + 25 ns t _{TLH} , t _{THL} = (0.75 ns/pF) C _L + 12.5 ns t _{TLH} , t _{THL} = (0.55 ns/pF) C _L + 9.5 ns	t _{TLH} , t _{THL}	5.0	—	100	200	ns
		10	—	50	100	
		15	—	40	80	
Propagation Delay Time Clock to Q1, 8-Bypass (Pin 6) High t _{PLH} , t _{PHL} = (1.7 ns/pF) C _L + 1715 ns t _{PLH} , t _{PHL} = (0.66 ns/pF) C _L + 617 ns t _{PLH} , t _{PHL} = (0.5 ns/pF) C _L + 425 ns	t _{PLH} , t _{PHL}	5.0	—	1800	3600	ns
		10	—	650	1300	
		15	—	450	1000	
Clock to Q1, 8-Bypass (Pin 6) Low t _{PLH} , t _{PHL} = (1.7 ns/pF) C _L + 3715 ns t _{PLH} , t _{PHL} = (0.66 ns/pF) C _L + 1467 ns t _{PLH} , t _{PHL} = (0.5 ns/pF) C _L + 1075 ns Clock to Q16 t _{PHL} , t _{PLH} = (1.7 ns/pF) C _L + 6915 ns t _{PHL} , t _{PLH} = (0.66 ns/pF) C _L + 2967 ns t _{PHL} , t _{PLH} = (0.5 ns/pF) C _L + 2175 ns Reset to Q _n t _{PHL} = (1.7 ns/pF) C _L + 1415 ns t _{PHL} = (0.66 ns/pF) C _L + 567 ns t _{PHL} = (0.5 ns/pF) C _L + 425 ns	t _{PLH} , t _{PHL}	5.0	—	3.8	7.6	μs
		10	—	1.5	3.0	
		15	—	1.1	2.3	
	t _{PLH} , t _{PHL}	5.0	—	7.0	14	μs
		10	—	3.0	6.0	
		15	—	2.2	4.5	
Reset to Q _n t _{PHL} = (1.7 ns/pF) C _L + 1415 ns t _{PHL} = (0.66 ns/pF) C _L + 567 ns t _{PHL} = (0.5 ns/pF) C _L + 425 ns	t _{PHL}	5.0	—	1500	3000	ns
		10	—	600	1200	
		15	—	450	900	
Clock Pulse Width	t _{WH}	5.0	600	300	—	ns
		10	200	100	—	
		15	170	85	—	
Clock Pulse Frequency (50% Duty Cycle)	f _{cl}	5.0	—	1.2	0.4	MHz
		10	—	3.0	1.5	
		15	—	5.0	2.0	
Clock Rise and Fall Time	t _{TLH} , t _{THL}	5.0	No Limit			—
		10				
		15				
Reset Pulse Width	t _{WH}	5.0	1000	500	—	ns
		10	400	200	—	
		15	300	150	—	

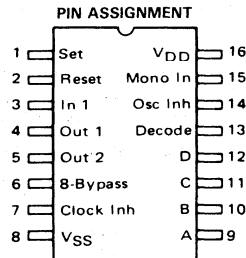
*The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

6

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range V_{SS} ≤ (V_{in} or V_{out}) ≤ V_{DD}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.



MC14536B

PIN DESCRIPTIONS

INPUTS

SET (Pin 1) — A high on Set asynchronously forces Decode Out to a high level. This is accomplished by setting an output conditioning latch to a high level while at the same time resetting the 24 flip-flop stages. After Set goes low (inactive), the occurrence of the first negative clock transition on IN_1 causes Decode Out to go low. The counter's flip-flop stages begin counting on the second negative clock transition of IN_1 . When Set is high, the on-chip RC oscillator is disabled. This allows for very low-power standby operation.

RESET (Pin 2) — A high on Reset asynchronously forces Decode Out to a low level; all 24 flip-flop stages are also reset to a low level. Like the Set input, Reset disables the on-chip RC oscillator for standby operation.

IN_1 (Pin 3) — The device's internal counters advance on the negative-going edge of this input. IN_1 may be used as an external clock input or used in conjunction with OUT_1 and OUT_2 to form an RC oscillator. When an external clock is used, both OUT_1 and OUT_2 may be left unconnected or used to drive 1 LSTTL or several CMOS loads.

8-BYPASS (Pin 6) — A high on this input causes the first 8 flip-flop stages to be bypassed. This device essentially becomes a 16-stage counter with all 16 stages selectable. Selection is accomplished by the A, B, C, and D inputs. (See the truth tables.)

CLOCK INHIBIT (Pin 7) — A high on this input disconnects the first counter stage from the clocking source. This holds the present count and inhibits further counting. However, the clocking source may continue to run. Therefore, when Clock Inhibit is brought low, no oscillator start-up time is required. When Clock Inhibit is low, the counter will start counting on the occurrence of the first negative edge of the clocking source at IN_1 .

OSC INHIBIT (Pin 14) — A high level on this pin stops the RC oscillator which allows for very low-power

standby operation. May also be used, in conjunction with an external clock, with essentially the same results as the Clock Inhibit input.

MONO-IN (Pin 15) — Used as the timing pin for the on-chip monostable multivibrator. If the Mono-In input is connected to V_{SS} , the monostable circuit is disabled, and Decode Out is directly connected to the selected Q output. The monostable circuit is enabled if a resistor is connected between Mono-In and V_{DD} . This resistor and the device's internal capacitance will determine the minimum output pulse widths. With the addition of an external capacitor to V_{SS} , the pulse width range may be extended. For reliable operation the resistor value should be limited to the range of 5 k Ω to 100 k Ω and the capacitor value should be limited to a maximum of 1000 pf. (See figures 3, 4, 5, and 10).

A, B, C, D (Pins 9, 10, 11, 12) — These inputs select the flip-flop stage to be connected to Decode Out. (See the truth tables.)

OUTPUTS

OUT_1 , OUT_2 (Pin 4, 5) — Outputs used in conjunction with IN_1 to form an RC oscillator. These outputs are buffered and may be used for 2^0 frequency division of an external clock.

DECODE OUT (Pin 13) — Output function depends on configuration. When the monostable circuit is disabled, this output is a 50% duty cycle square wave during free run.

TEST MODE

The test mode configuration divides the 24 flip-flop stages into three 8-stage sections to facilitate a fast test sequence. The test mode is enabled when 8-Bypass, Set and Reset are at a high level. (See Figure 8.)

MC14536B

TRUTH TABLES

Input					Stage Selected For Decode Out
8-Bypass	D	C	B	A	
0	0	0	0	0	9
0	0	0	0	1	10
0	0	0	1	0	11
0	0	0	1	1	12
0	0	1	0	0	13
0	0	1	0	1	14
0	0	1	1	0	15
0	0	1	1	1	16
0	1	0	0	0	17
0	1	0	0	1	18
0	1	0	1	0	19
0	1	0	1	1	20
0	1	1	0	0	21
0	1	1	0	1	22
0	1	1	1	0	23
0	1	1	1	1	24

Input					Stage Selected For Decode Out
8-Bypass	D	C	B	A	
1	0	0	0	0	1
1	0	0	0	1	2
1	0	0	1	0	3
1	0	0	1	1	4
1	0	1	0	0	5
1	0	1	0	1	6
1	0	1	1	0	7
1	0	1	1	1	8
1	1	0	0	0	9
1	1	0	0	1	10
1	1	0	1	0	11
1	1	0	1	1	12
1	1	1	0	0	13
1	1	1	0	1	14
1	1	1	1	0	15
1	1	1	1	1	16

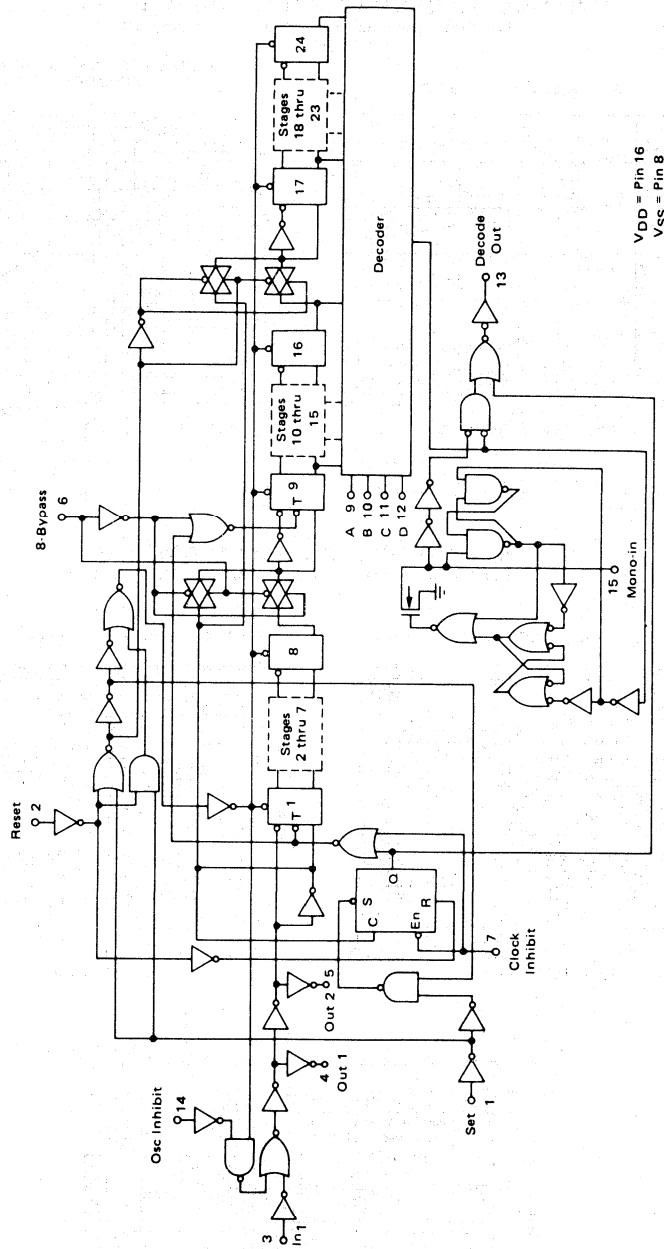
FUNCTION TABLE

In ₁	Set	Reset	Clock Inh	OSC Inh	Out 1	Out 2	Decode Out
	0	0	0	0			No Change
	0	0	0	0			Advance to next state
X	1	0	0	0	0	1	1
X	0	1	0	0	0	1	0
X	0	0	1	0	—	—	No Change
X	0	0	0	1	0	1	No Change
0	0	0	0	X	0	1	No Change
1	0	0	0				Advance to next state

X = Don't Care

MC14536B

LOGIC DIAGRAM



VDD = Pin 16
VSS = Pin 8

TYPICAL RC OSCILLATOR CHARACTERISTICS
(For Circuit Diagram See Figure 11 In Application)

FIGURE 1 — RC OSCILLATOR STABILITY

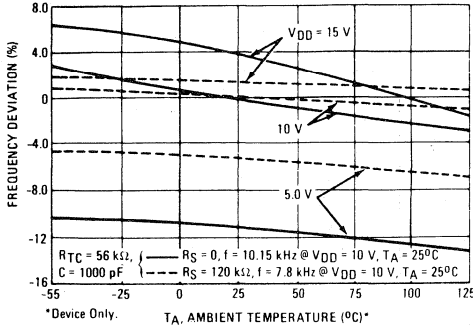
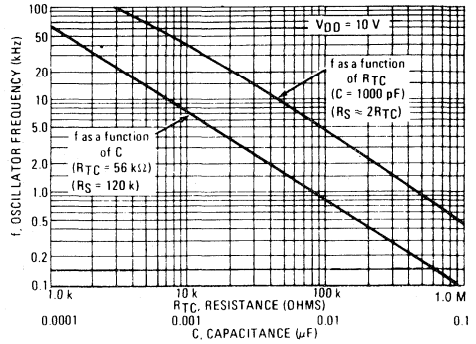


FIGURE 2 — RC OSCILLATOR FREQUENCY AS A FUNCTION OF R_{TC} AND C



MONOSTABLE CHARACTERISTICS
(For Circuit Diagram See Figure 10 In Application)

FIGURE 3 — TYPICAL C_X versus PULSE WIDTH @ $V_{DD} = 5.0 V$

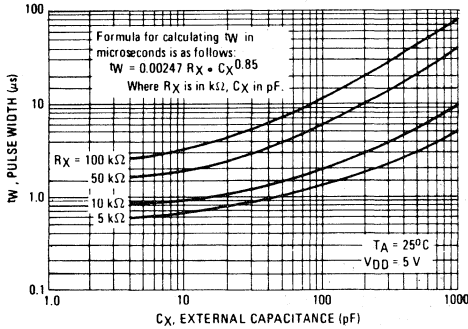


FIGURE 4 — TYPICAL C_X versus PULSE WIDTH @ $V_{DD} = 10 V$

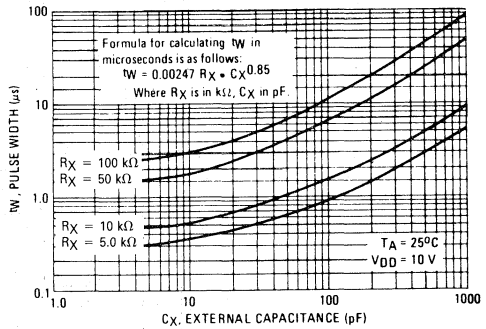
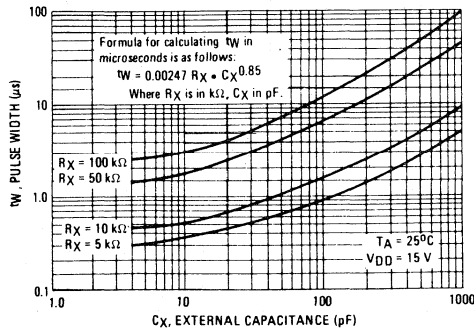


FIGURE 5 — TYPICAL C_X versus PULSE WIDTH @ $V_{DD} = 15 V$



6

MC14536B

FIGURE 6 — POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

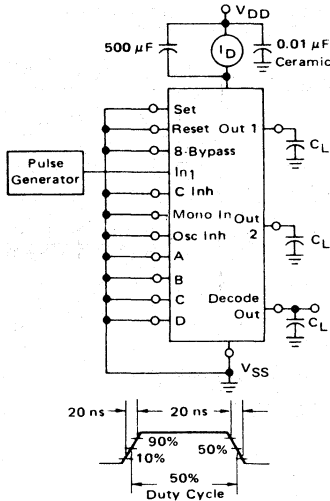
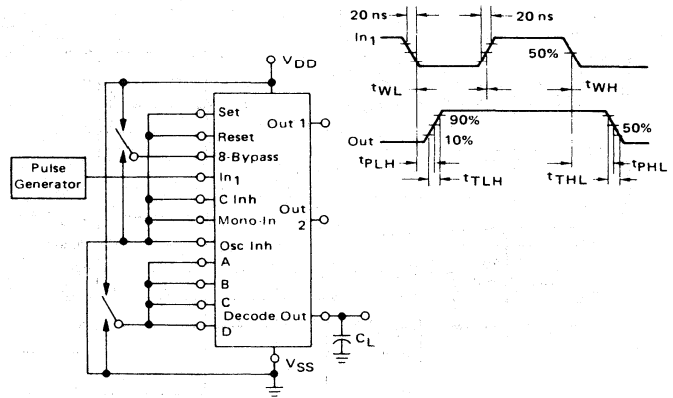


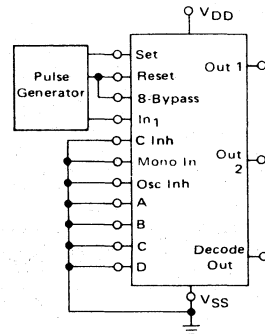
FIGURE 7 — SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



FUNCTIONAL TEST SEQUENCE

Test function (Figure 8) has been included for the reduction of test time required to exercise all 24 counter stages. This test function divides the counter into three 8-stage sections and 255 counts are loaded in each of the 8-stage sections in parallel. All flip-flops are now at a "1". The counter is now returned to the normal 24-stages in series configuration. One more pulse is entered into In₁ which will cause the counter to ripple from an all "1" state to an all "0" state.

FIGURE 8 — FUNCTIONAL TEST CIRCUIT

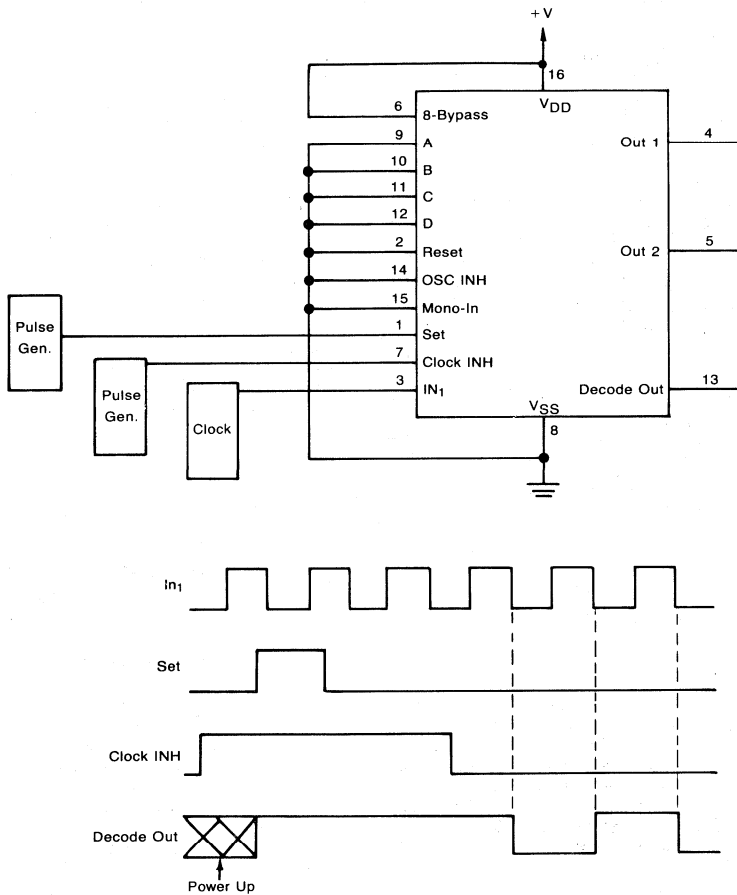


FUNCTIONAL TEST SEQUENCE

INPUTS				OUTPUTS	COMMENTS
In ₁	Set	Reset	8-Bypass	Decode Out Q1 thru Q24	
1	0	1	1	0	All 24 stages are in Reset mode.
1	1	1	1	0	Counter is in three 8 stage sections in parallel mode.
0	1	1	1	0	First "1" to "0" transition of clock.
1	0	1	1		255 "1" to "0" transitions are clocked in the counter.
0	1	1	1	1	The 255 "1" to "0" transition.
0	0	0	0	1	Counter converted back to 24 stages in series mode. Set and Reset must be connected together and simultaneously go from "1" to "0".
1	0	0	0	1	In ₁ Switches to a "1".
0	0	0	0	0	Counter Ripples from an all "1" state to an all "0" state.

MC14536B

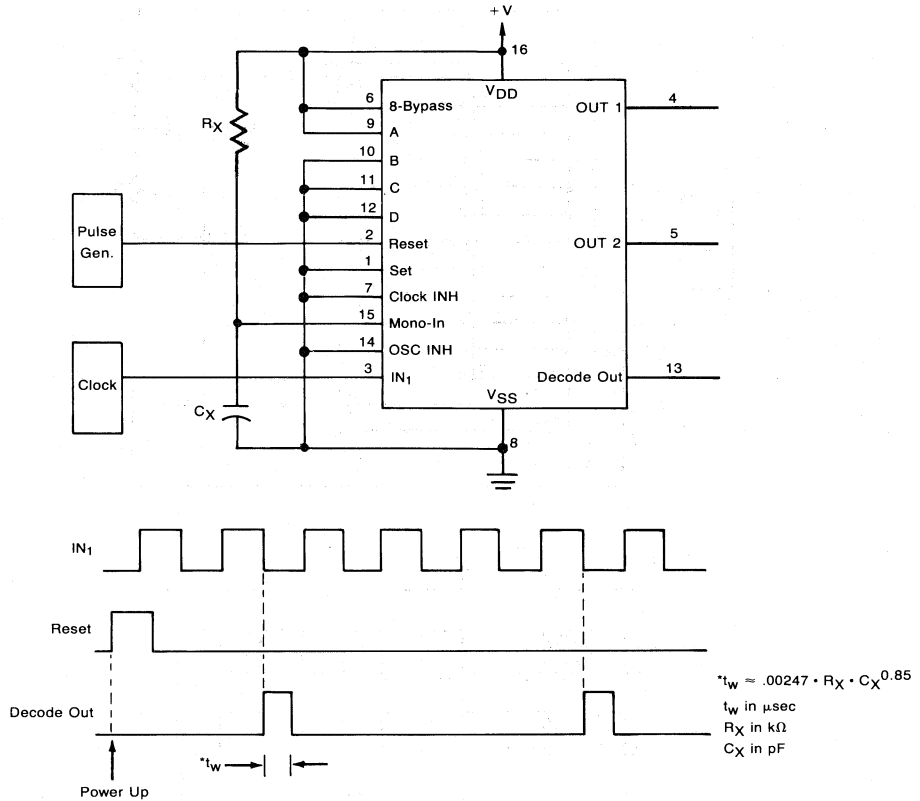
FIGURE 9 — TIME INTERVAL CONFIGURATION USING AN EXTERNAL CLOCK, SET, AND CLOCK INHIBIT FUNCTIONS (DIVIDE-BY-2 CONFIGURED)



Note: When power is first applied to the device, Decode Out can be either at a high or low state. On the rising edge of a Set pulse the output goes high if initially at a low state. The output remains high if initially at a high state. Because Clock Inh is held high, the clock source on the input pin has no effect on the output. Once Clock Inh is taken low, the output goes low on the first negative clock transition. The output returns high depending on the 8-Bypass, A, B, C, and D inputs, and the clock input period. A 2^n frequency division (where n = the number of stages selected from the truth table) is obtainable at Decode Out. A 2^0 -divided output of IN_1 can be obtained at OUT_1 and OUT_2 .

MC14536B

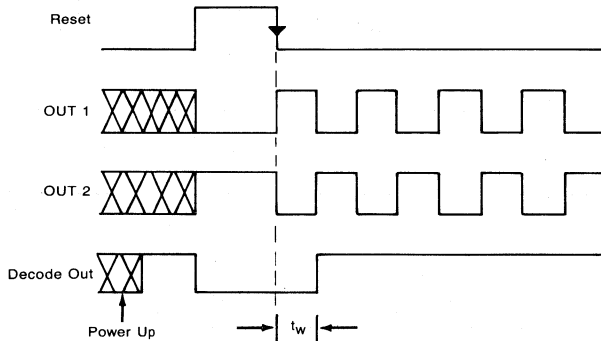
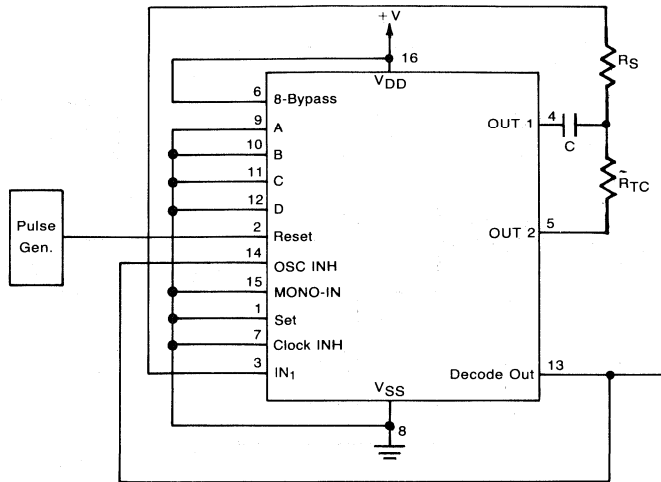
FIGURE 10 — TIME INTERVAL CONFIGURATION USING AN EXTERNAL CLOCK, RESET, AND OUTPUT MONOSTABLE TO ACHIEVE A PULSE OUTPUT. (DIVIDE-BY-4 CONFIGURED).



Note: When Power is first applied to the device with the Reset input going high, Decode Out initializes low. Bringing the Reset input low enables the chip's internal counters. After Reset goes low, the $2^n/2$ negative transition of the clock input causes Decode Out to go high. Since the Mono-In input is being used, the output becomes monostable. The pulse width of the output is dependent on the external timing components. The second and all subsequent pulses occur at $2^n \times$ (the clock period) intervals where n = the number of stages selected from the truth table.

MC14536B

FIGURE 11 — TIME INTERVAL CONFIGURATION USING ON-CHIP RC OSCILLATOR AND RESET INPUT TO INITIATE TIME INTERVAL (DIVIDE-BY-2 CONFIGURED)



$$f_{osc} \approx \frac{1}{2.3 R_{TC} C}$$

$R_S \geq R_{TC}$
 $F = \text{Hz}$
 $R = \text{Ohms}$
 $C = \text{FARADS}$

Note: This circuit is designed to use the on-chip oscillation function. The oscillator frequency is determined by the external R and C components. When power is first applied to the device, Decode Out initializes to a high state. Because this output is tied directly to the Osc-Inh input, the oscillator is disabled. This puts the device in a low-current standby condition. The rising edge of the Reset pulse will cause the output to go low. This in turn causes Osc-Inh to go low. However, while Reset is high, the oscillator is still disabled (i.e.: standby condition). After Reset goes low, the output remains low for $2^{N/2}$ of the oscillator's period. After the part times out, the output again goes high.

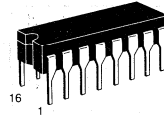


MC14538B

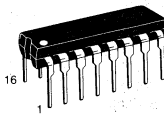
DUAL PRECISION RETRIGGERABLE/RESETTABLE MONOSTABLE MULTIVIBRATOR

The MC14538B is a dual, retriggerable, resettable monostable multivibrator. It may be triggered from either edge of an input pulse, and produces an accurate output pulse over a wide range of widths, the duration and accuracy of which are determined by the external timing components, C_X and R_X .

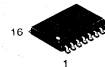
- Unlimited Rise and Fall Time Allowed on the A Trigger Input
- Pulse Width Range = 10 μ s to 10 s
- Latched Trigger Inputs
- Separate Latched Reset Inputs
- 3.0 Vdc to 18 Vdc Operational Limits
- Triggerable from Positive (A Input) or Negative-Going Edge (B-Input)
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range
- Pin-for-pin Compatible with MC14528B and CD4528B (CD4098)
- Use the MC54/74HC4538A for Pulse Widths Less Than 10 μ s with Supplies Up to 6 V.



L SUFFIX
CERAMIC
CASE 620



P SUFFIX
PLASTIC
CASE 648



DW SUFFIX
SOIC
CASE 751G

ORDERING INFORMATION

- MC14XXXBCP Plastic
- MC14XXXBCL Ceramic
- *MC14XXXBDW SOIC

$T_A = -55^\circ$ to 125°C for all packages.

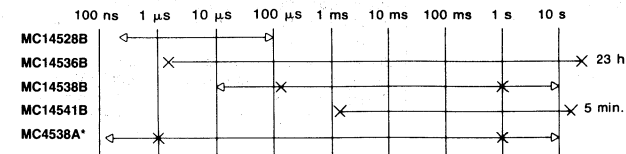
MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	-0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	-0.5 to $V_{DD} + 0.5$	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	± 10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	-65 to +150	$^\circ\text{C}$
T_L	Lead Temperature (8-Second Soldering)	260	$^\circ\text{C}$

*Maximum Ratings are those values beyond which damage to the device may occur.

†Temperature Derating: Plastic "P and D/DW" Packages: -7.0 mW/ $^\circ\text{C}$ From 65°C To 125°C
Ceramic "L" Packages: -12 mW/ $^\circ\text{C}$ From 100°C To 125°C

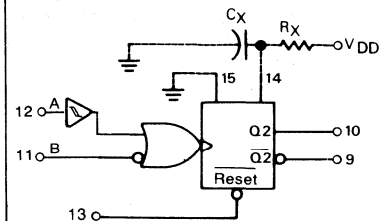
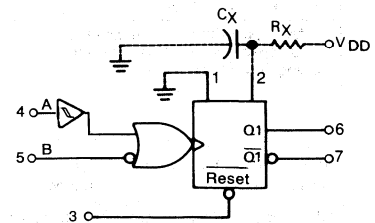
ONE-SHOT SELECTION GUIDE



*LIMITED OPERATING VOLTAGE (2-6V)

Total Output Pulse Width Range $\leftarrow \rightarrow$
Recommended Pulse Width Range $\times \times$

BLOCK DIAGRAM



R_X and C_X are external components.

V_{DD} = Pin 16

V_{SS} = Pin 8, Pin 1, Pin 15

*Consult factory for possible "D" suffix SOIC Case 751B.

MC14538B

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V _{DD} V _{dC}	-55°C		25°C			125°C		Unit
			Min	Max	Min	Typ #	Max	Min	Max	
Output Voltage V _{in} = V _{DD} or 0	V _{OL}	5.0	—	0.05	—	0	0.05	—	0.05	V _{dC}
		10	—	0.05	—	0	0.05	—	0.05	
V _{in} = 0 or V _{DD}	V _{OH}	5.0	4.95	—	4.95	5.0	—	4.95	—	V _{dC}
		10	9.95	—	9.95	10	—	9.95	—	
Input Voltage (V _O = 4.5 or 0.5 V _{dC}) (V _O = 9.0 or 1.0 V _{dC}) (V _O = 13.5 or 1.5 V _{dC})	V _{IL}	5.0	—	1.5	—	2.25	1.5	—	1.5	V _{dC}
		10	—	3.0	—	4.50	3.0	—	3.0	
(V _O = 0.5 or 4.5 V _{dC}) (V _O = 1.0 or 9.0 V _{dC}) (V _O = 1.5 or 13.5 V _{dC})	V _{IH}	5.0	3.5	—	3.5	2.75	—	3.5	—	V _{dC}
		10	7.0	—	7.0	5.50	—	7.0	—	
Output Drive Current (V _{OH} = 2.5 V _{dC}) (V _{OH} = 4.6 V _{dC}) (V _{OH} = 9.5 V _{dC}) (V _{OH} = 13.5 V _{dC})	Source	I _{OH}	5.0	-3.0	—	-2.4	-4.2	—	-1.7	mAdc
	Sink		5.0	-0.64	—	-0.51	-0.88	—	-0.36	
(V _{OL} = 0.4 V _{dC}) (V _{OL} = 0.5 V _{dC}) (V _{OL} = 1.5 V _{dC})		I _{OL}	10	-1.6	—	-1.3	-2.25	—	-0.9	mAdc
	15		-4.2	—	-3.4	-8.8	—	-2.4		
Input Current, Pin 2 or 14	I _{in}	15	—	±0.05	—	±0.00001	±0.05	—	±0.5	μAdc
Input Current, Other Inputs	I _{in}	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	μAdc
Input Capacitance, Pin 2 or 14	C _{in}	—	—	—	—	25	—	—	—	pF
Input Capacitance, Other Inputs (V _{in} = 0)	C _{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package) Q = Low, Q̄ = High	I _{DD}	5.0	—	5.0	—	0.005	5.0	—	150	μAdc
		10	—	10	—	0.010	10	—	300	
		15	—	20	—	0.015	20	—	600	
Quiescent Current, Active State (Both) (Per Package) Q = High, Q̄ = Low	I _{DD}	5.0	—	2.0	—	0.04	0.20	—	2.0	mAdc
		10	—	2.0	—	0.08	0.45	—	2.0	
		15	—	2.0	—	0.13	0.70	—	2.0	
**Total Supply Current at an external load capacitance (C _L) and at external timing network (R _X , C _X)	I _T	5.0 10	$I_T = (3.5 \times 10^{-2}) R_X C_X f + 4 C_X f + 1 \times 10^{-5} C_L f$ $I_T = (8.0 \times 10^{-2}) R_X C_X f + 9 C_X f + 2 \times 10^{-5} C_L f$ $I_T = (1.25 \times 10^{-1}) R_X C_X f + 12 C_X f + 3 \times 10^{-5} C_L f$ where: I _T in μA (one monostable switching only), C _X in μF, C _L in pF, R _X in k ohms, and f in Hz is the input frequency.							

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range V_{SS} ≤ (V_{in} or V_{out}) ≤ V_{DD}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

MC14538B

SWITCHING CHARACTERISTICS* ($C_L = 50 \text{ pF}$, $T_A = 25^\circ\text{C}$)

Characteristic	Symbol	V _{DD} V _{dc}	All Types			Unit
			Min	Typ #	Max	
Output Rise Time $t_{TLH} = (1.35 \text{ ns/pF}) C_L + 33 \text{ ns}$ $t_{TLH} = (0.60 \text{ ns/pF}) C_L + 20 \text{ ns}$ $t_{TLH} = (0.40 \text{ ns/pF}) C_L + 20 \text{ ns}$	t_{TLH}	5.0 10 15	— — —	100 50 40	200 100 80	ns
Output Fall Time $t_{THL} = (1.35 \text{ ns/pF}) C_L + 33 \text{ ns}$ $t_{THL} = (0.60 \text{ ns/pF}) C_L + 20 \text{ ns}$ $t_{THL} = (0.40 \text{ ns/pF}) C_L + 20 \text{ ns}$	t_{THL}	5.0 10 15	— — —	100 50 40	200 100 80	ns
Propagation Delay Time A or B to Q or \bar{Q} $t_{PLH}, t_{PHL} = (0.90 \text{ ns/pF}) C_L + 255 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.36 \text{ ns/pF}) C_L + 132 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.26 \text{ ns/pF}) C_L + 87 \text{ ns}$ Reset to Q or \bar{Q} $t_{PLH}, t_{PHL} = (0.90 \text{ ns/pF}) C_L + 205 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.36 \text{ ns/pF}) C_L + 107 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.26 \text{ ns/pF}) C_L + 82 \text{ ns}$	$t_{PLH},$ t_{PHL}	5.0 10 15	— — —	300 150 100	600 300 220	ns
Input Rise and Fall Times Reset	t_r, t_f	5 10 15	— — —	— — —	15 5 4	μs
B Input		5 10 15	— — —	300 1.2 0.4	1.0 0.1 0.05	ms
A Input		5 10 15	No Limit			—
Input Pulse Width A, B, or Reset	$t_{WH},$ t_{WL}	5.0 10 15	170 90 80	85 45 40	— — —	ns
Retrigger Time	t_{rr}	5.0 10 15	0 0 0	— — —	— — —	ns
Output Pulse Width — Q or \bar{Q} Refer to Figures 8 and 9 $C_X = 0.002 \mu\text{F}, R_X = 100 \text{ k}\Omega$	T	5.0 10 15	198 200 202	210 212 214	230 232 234	μs
$C_X = 0.1 \mu\text{F}, R_X = 100 \text{ k}\Omega$		5.0 10 15	9.3 9.4 9.5	9.86 10 10.14	10.5 10.6 10.7	ms
$C_X = 10 \mu\text{F}, R_X = 100 \text{ k}\Omega$		5.0 10 15	0.91 0.92 0.93	0.965 0.98 0.99	1.03 1.04 1.06	s
Pulse Width Match between circuits in the same package. $C_X = 0.1 \mu\text{F}, R_X = 100 \text{ k}\Omega$	$100 \frac{(T_1 - T_2)}{T_1}$	5.0 10 15	— — —	± 1.0 ± 1.0 ± 1.0	± 5.0 ± 5.0 ± 5.0	%

*The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

OPERATING CONDITIONS

External Timing Resistance	R_X	—	5.0	—	*	$\text{k}\Omega$
External Timing Capacitance	C_X	—	0	—	No Limit †	μF

* The maximum usable resistance R_X is a function of the leakage of the capacitor C_X , leakage of the MC14538B, and leakage due to board layout and surface resistance. Susceptibility to externally induced noise signals may occur for $R_X \geq 1 \text{ M}\Omega$.

† If $C_X \geq 15 \mu\text{F}$, use discharge protection diode per Fig. 11.

6

MC14538B

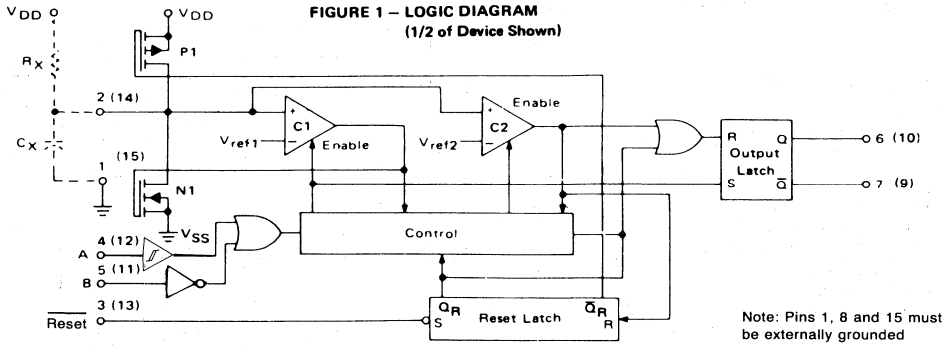


FIGURE 2 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORMS

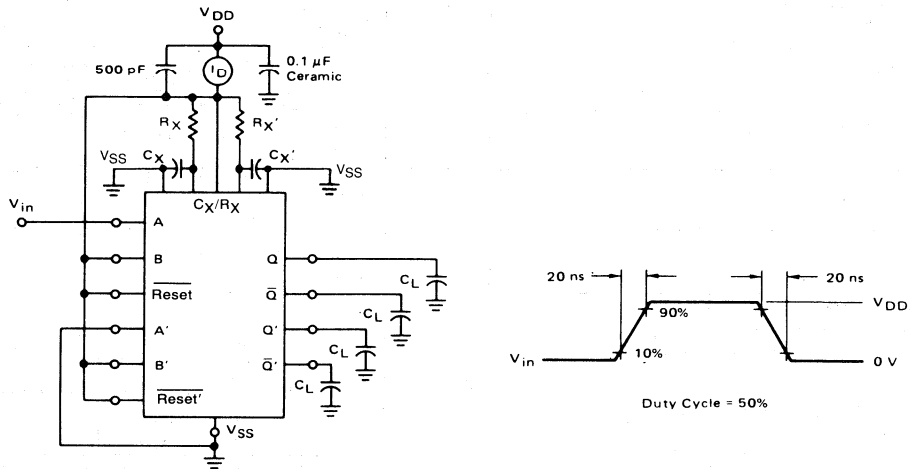
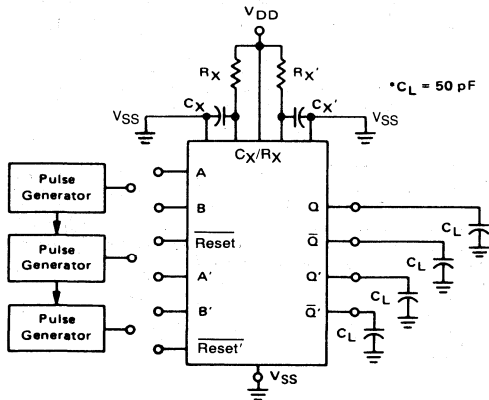


FIGURE 3 – SWITCHING TEST CIRCUIT

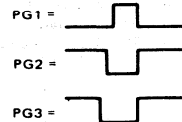


INPUT CONNECTIONS

CHARACTERISTICS	Reset	A	B
t_{PLH} , t_{PHL} , t_{TLH} , t_{THL} , T , t_{WH} , t_{WL}	VDD	PG1	VDD
t_{PLH} , t_{PHL} , t_{TLH} , t_{THL} , T , t_{WH} , t_{WL}	VDD	VSS	PG2
$t_{PLH(R)}$, $t_{PHL(R)}$, T , t_{WH} , t_{WL}	PG3	PG1	PG2

*Includes capacitance of probes, wiring, and fixture parasitic.

NOTE: Switching test waveforms for PG1, PG2, PG3 are shown in Figure 4.



6

MC14538B

FIGURE 4 – SWITCHING TEST WAVEFORMS

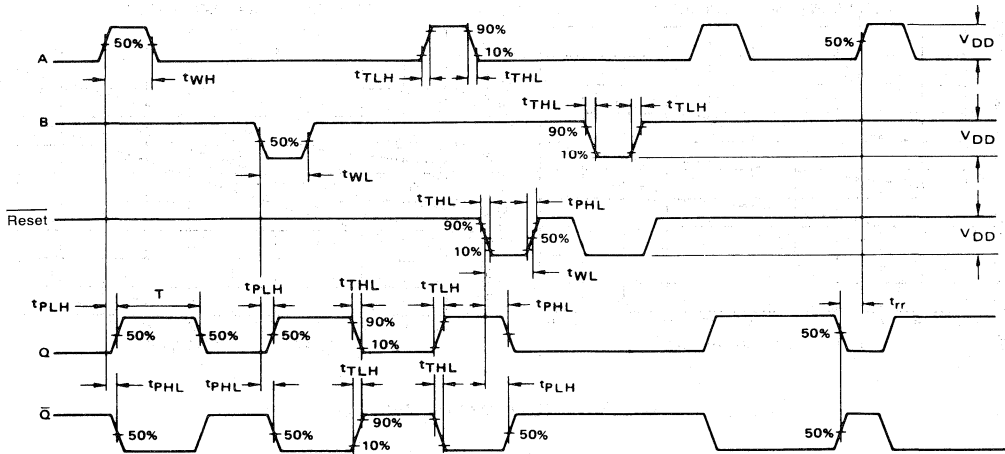


FIGURE 5 – TYPICAL NORMALIZED DISTRIBUTION OF UNITS FOR OUTPUT PULSE WIDTH

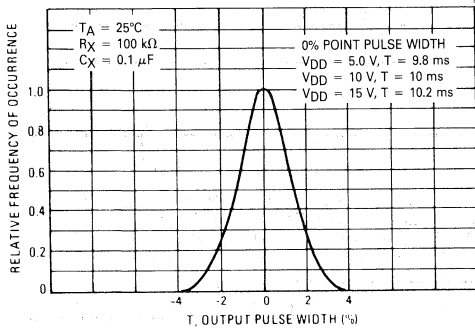


FIGURE 6 – TYPICAL PULSE WIDTH VARIATION AS A FUNCTION OF SUPPLY VOLTAGE V_{DD}

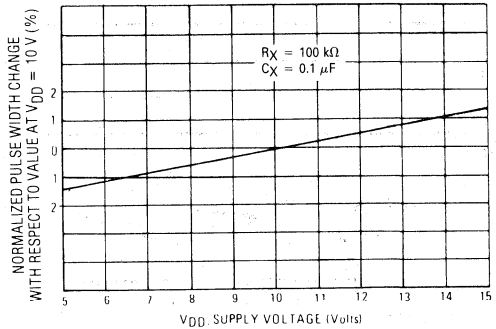
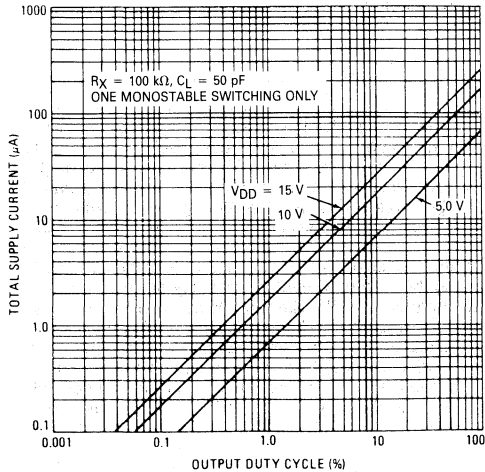


FIGURE 7 – TYPICAL TOTAL SUPPLY CURRENT versus OUTPUT DUTY CYCLE



FUNCTION TABLE

Inputs		Outputs	
Reset	A	B	Q \bar{Q}
H		H	
H	L		
H		L	Not Triggered
H	H		Not Triggered
H	L, H,	H	Not Triggered
H	L	L, H,	Not Triggered
L	X	X	L H
	X	X	Not Triggered

MC14538B

FIGURE 8 — TYPICAL ERROR OF PULSE WIDTH EQUATION versus TEMPERATURE

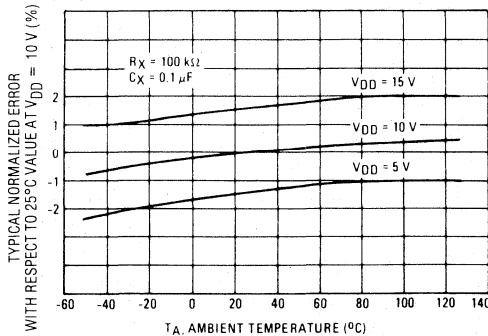
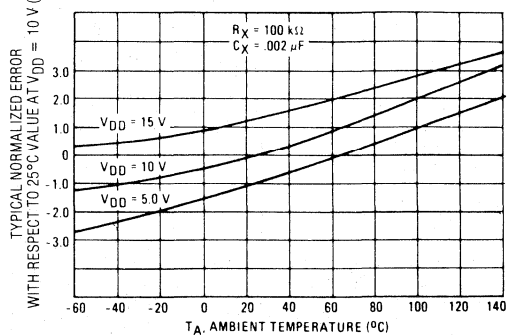
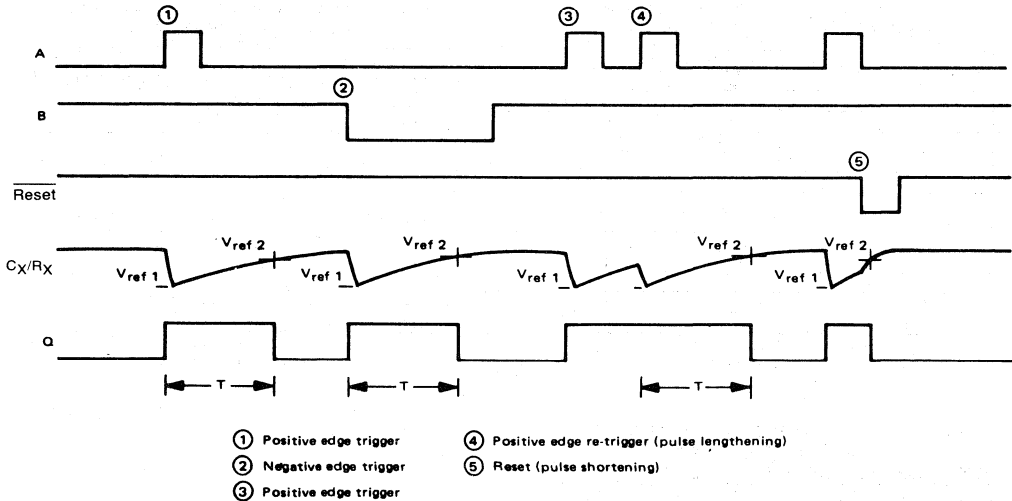


FIGURE 9 — TYPICAL ERROR OF PULSE WIDTH EQUATION versus TEMPERATURE



THEORY OF OPERATION

FIGURE 10 — Timing Operation



TRIGGER OPERATION

The block diagram of the MC14538B is shown in Figure 1, with circuit operation following.

As shown in Figure 1 and 10, before an input trigger occurs, the monostable is in the quiescent state with the Q output low, and the timing capacitor C_X completely charged to V_{DD} . When the trigger input A goes from V_{SS} to V_{DD} (while inputs B and Reset are held to V_{DD}) a valid trigger is recognized, which turns on comparator C1 and N-channel transistor N1 (1). At the same time the output latch is set. With transistor N1 on, the capacitor C_X rapidly discharges toward V_{SS} until V_{ref1} is reached. At this point the output of comparator C1 changes state and transistor N1 turns off. Comparator C1 then turns off while at the same time comparator C2 turns on. With transistor N1 off, the capacitor C_X begins

to charge through the timing resistor, R_X , toward V_{DD} . When the voltage across C_X equals V_{ref2} , comparator C2 changes state, causing the output latch to reset (Q goes low) while at the same time disabling comparator C2 (2). This ends at the timing cycle with the monostable in the quiescent state, waiting for the next trigger.

In the quiescent state, C_X is fully charged to V_{DD} causing the current through resistor R_X to be zero. Both comparators are "off" with total device current due only to reverse junction leakages. An added feature of the MC14538B is that the output latch is set via the input trigger without regard to the capacitor voltage. Thus, propagation delay from trigger to Q is independent of the value of C_X , R_X , or the duty cycle of the input waveform.

MC14538B

RETRIGGER OPERATION

The MC14538B is retriggered if a valid trigger occurs ③ followed by another valid trigger ④ before the Q output has returned to the quiescent (zero) state. Any retrigger, after the timing node voltage at pin 2 or 14 has begun to rise from $V_{ref 1}$, but has not yet reached $V_{ref 2}$, will cause an increase in output pulse width T. When a valid retrigger is initiated ④, the voltage at C_X/R_X will again drop to $V_{ref 1}$ before progressing along the RC charging curve toward V_{DD} . The Q output will remain high until time T, after the last valid retrigger.

RESET OPERATION

The MC14538B may be reset during the generation of the output pulse. In the reset mode of operation, an input pulse on Reset sets the reset latch and causes the capacitor to be fast charged to V_{DD} by turning on transistor P1 ⑤. When the voltage on the capacitor reaches $V_{ref 2}$, the reset latch will clear, and will then be ready to accept another pulse. If the Reset input is held low, any trigger inputs that occur will be inhibited and the Q and \bar{Q} outputs of the output latch will not change. Since the Q output is reset when an input low level is

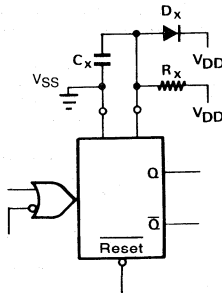
detected on the $\overline{\text{Reset}}$ input, the output pulse T can be made significantly shorter than the minimum pulse width specification.

POWER-DOWN CONSIDERATIONS

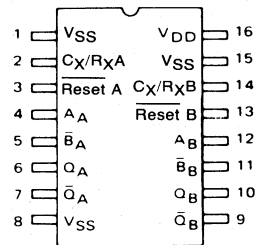
Large capacitance values can cause problems due to the large amount of energy stored. When a system containing the MC14538B is powered down, the capacitor voltage may discharge from V_{DD} through the standard protection diodes at pin 2 or 14. Current through the protection diodes should be limited to 10 mA and therefore the discharge time of the V_{DD} supply must not be faster than $(V_{DD}) \cdot (C_X)/(10 \text{ mA})$. For example, if $V_{DD} = 10 \text{ V}$ and $C_X = 10 \mu\text{F}$, the V_{DD} supply should discharge no faster than $(10 \text{ V}) \times (10 \mu\text{F})/(10 \text{ mA}) = 10 \text{ ms}$. This is normally not a problem since power supplies are heavily filtered and cannot discharge at this rate.

When a more rapid decrease of V_{DD} to zero volts occurs, the MC14538B can sustain damage. To avoid this possibility use an external clamping diode, D_X , connected as shown in Fig. 11.

FIGURE 11 — USE OF A DIODE TO LIMIT POWER DOWN CURRENT SURGE



PIN ASSIGNMENT



MC14538B

TYPICAL APPLICATIONS

FIGURE 12 — RETRIGGERABLE MONOSTABLES CIRCUITRY

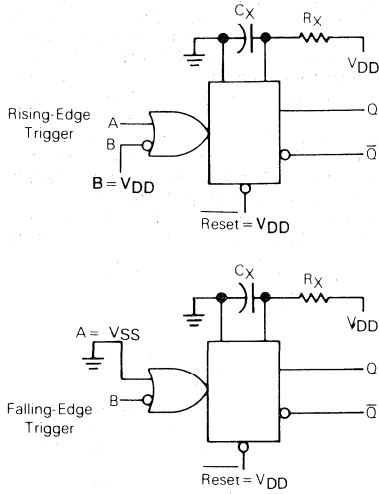


FIGURE 13 — NON-RETRIGGERABLE MONOSTABLES CIRCUITRY

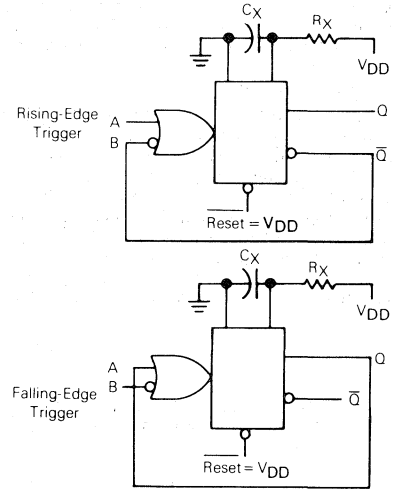
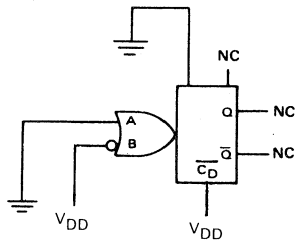


FIGURE 14 — CONNECTION OF UNUSED SECTIONS





MOTOROLA

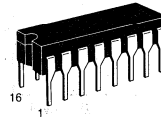
MC14539B

DUAL 4-CHANNEL DATA SELECTOR/MULTIPLEXER

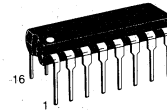
The MC14539B data selector/multiplexer is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. The circuit consists of two sections of four inputs each. One input from each section is selected by the address inputs A and B. A "high" on the Strobe input will cause the output to remain "low".

This device finds primary application in signal multiplexing functions. It permits multiplexing from N-lines to I-line, and can also perform parallel-to-serial conversion. The Strobe input allows cascading of n-lines to n-lines.

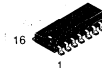
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-Power TTL Loads or One Low-Power Schottky TTL Load Over the Rated Temperature Range



**L SUFFIX
CERAMIC
CASE 620**



**P SUFFIX
PLASTIC
CASE 648**



**D SUFFIX
SOIC
CASE 751B**

ORDERING INFORMATION

- MC14XXXBCP Plastic
- MC14XXXBCL Ceramic
- MC14XXXBD SOIC

T_A = -55° to 125°C for all packages.

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V _{DD}	DC Supply Voltage	-0.5 to +18.0	V
V _{in} , V _{out}	Input or Output Voltage (DC or Transient)	-0.5 to V _{DD} + 0.5	V
I _{in} , I _{out}	Input or Output Current (DC or Transient), per Pin	± 10	mA
P _D	Power Dissipation, per Package†	500	mW
T _{stg}	Storage Temperature	-65 to +150	°C
T _L	Lead Temperature (8-Second Soldering)	260	°C

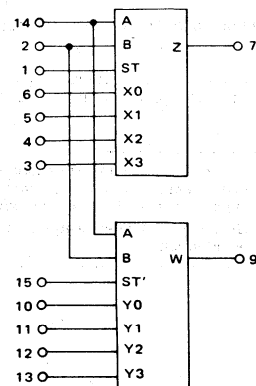
*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P and D/DW" Packages: -7.0 mW/°C From 65°C To 125°C
Ceramic "L" Packages: -12 mW/°C From 100°C To 125°C

TRUTH TABLE

ADDRESS INPUTS		DATA INPUTS				ST, ST'	OUTPUTS Z, W
B	A	X3	X2	X1	X0		
X	X	X	X	X	X	1	0
0	0	X	X	X	0	0	0
0	0	X	X	X	1	0	1
0	1	X	X	0	X	0	0
0	1	X	X	1	X	0	1
1	0	X	0	X	X	0	0
1	0	X	1	X	X	0	1
1	1	0	X	X	X	0	0
1	1	1	X	X	X	0	1

X = Don't Care

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

MC14539B

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V _{DD} Vdc	-55°C		25°C			125°C		Unit
			Min	Max	Min	Typ #	Max	Min	Max	
Output Voltage V _{in} = V _{DD} or 0 V _{in} = 0 or V _{DD}	V _{OL}	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
		10	—	0.05	—	0	0.05	—	0.05	
15		—	0.05	—	0	0.05	—	0.05		
"1" Level	V _{OH}	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc
		10	9.95	—	9.95	10	—	9.95	—	
		15	14.95	—	14.95	15	—	14.95	—	
Input Voltage (V _O = 4.5 or 0.5 Vdc) (V _O = 9.0 or 1.0 Vdc) (V _O = 13.5 or 1.5 Vdc)	V _{IL}	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc
		10	—	3.0	—	4.50	3.0	—	3.0	
15		—	4.0	—	6.75	4.0	—	4.0		
"1" Level (V _O = 0.5 or 4.5 Vdc) (V _O = 1.0 or 9.0 Vdc) (V _O = 1.5 or 13.5 Vdc)	V _{IH}	5.0	3.5	—	3.5	2.75	—	3.5	—	Vdc
		10	7.0	—	7.0	5.50	—	7.0	—	
		15	11	—	11	8.25	—	11	—	
Output Drive Current (V _{OH} = 2.5 Vdc) (V _{OH} = 4.6 Vdc) (V _{OH} = 9.5 Vdc) (V _{OH} = 13.5 Vdc) (V _{OL} = 0.4 Vdc) (V _{OL} = 0.5 Vdc) (V _{OL} = 1.5 Vdc)	Source	I _{OH}	5.0	-3.0	—	-2.4	-4.2	—	-1.7	mAdc
		5.0	-0.64	—	-0.51	-0.88	—	-0.36	—	
10		-1.6	—	-1.3	-2.25	—	-0.9	—		
Sink	I _{OL}	5.0	0.64	—	0.51	0.88	—	0.36	—	mAdc
		10	1.6	—	1.3	2.25	—	0.9	—	
		15	4.2	—	3.4	8.8	—	2.4	—	
Input Current	I _{in}	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	μAdc
Input Capacitance (V _{in} = 0)	C _{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)	I _{DD}	5.0	—	5.0	—	0.005	5.0	—	150	μAdc
		10	—	10	—	0.010	10	—	300	
		15	—	20	—	0.015	20	—	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C _L = 50 pF on all outputs, all buffers switching)	I _T	5.0	I _T = (0.85 μA/kHz) f + I _{DD}							μAdc
10	I _T = (1.70 μA/kHz) f + I _{DD}									
15	I _T = (2.60 μA/kHz) f + I _{DD}									

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) Vfk$$

where: I_T is in μA (per package), C_L in pF, V = (V_{DD} - V_{SS}) in volts, f in kHz is input frequency, and k = 0.002.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range V_{SS} ≤ (V_{in} or V_{out}) ≤ V_{DD}. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

MC14539B

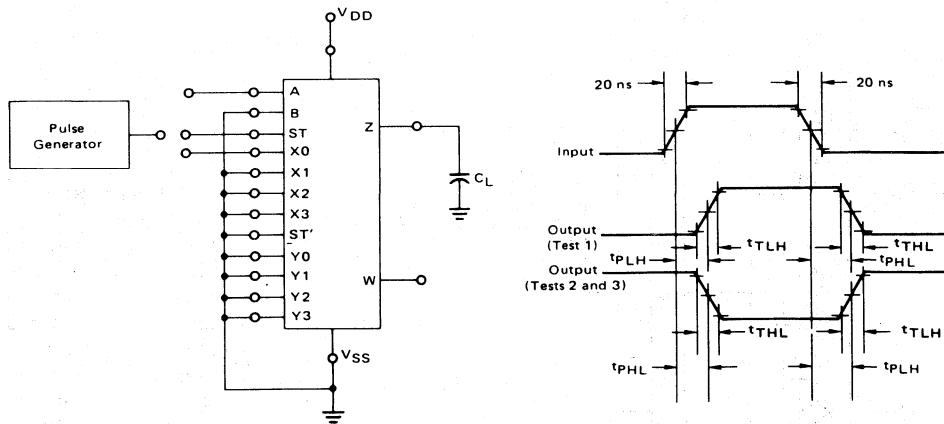
SWITCHING CHARACTERISTICS* ($C_L = 50 \text{ pF}$, $T_A = 25^\circ\text{C}$)

Characteristic	Symbol	V _{DD}	Min	Typ #	Max	Unit	
Output Rise and Fall Time $t_{TLH}, t_{THL} = (1.5 \text{ ns/pF}) C_L + 25 \text{ ns}$ $t_{TLH}, t_{THL} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$ $t_{TLH}, t_{THL} = (0.55 \text{ ns/pF}) C_L + 9.5 \text{ ns}$	t_{TLH}, t_{THL}	5.0	—	100	200	ns	
		10	—	50	100		
		15	—	40	80		
Propagation Delay Time X, Y Input to Output $t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 125 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 57 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.55 \text{ ns/pF}) C_L + 45 \text{ ns}$ A Input to Output $t_{PLH} = (1.7 \text{ ns/pF}) C_L + 140 \text{ ns}$ $t_{PLH} = (0.66 \text{ ns/pF}) C_L + 77 \text{ ns}$ $t_{PLH} = (0.5 \text{ ns/pF}) C_L + 60 \text{ ns}$ $t_{PHL} = (1.7 \text{ ns/pF}) C_L + 160 \text{ ns}$ $t_{PHL} = (0.66 \text{ ns/pF}) C_L + 82 \text{ ns}$ $t_{PHL} = (0.5 \text{ ns/pF}) C_L + 65 \text{ ns}$ Strobe Input to Output $t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 60 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 35 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 35 \text{ ns}$	t_{PLH}, t_{PHL}	5.0	—	210	420	ns	
		10	—	90	180		
		15	—	70	140		
		t_{PLH}	5.0	—	225	450	ns
			10	—	110	220	
			15	—	85	170	
		t_{PHL}	5.0	—	245	490	ns
			10	—	115	230	
			15	—	90	180	
		t_{PLH}, t_{PHL}	5.0	—	145	290	ns
			10	—	75	150	
			15	—	60	120	

*The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

FIGURE 1 – AC TEST CIRCUIT AND WAVEFORMS

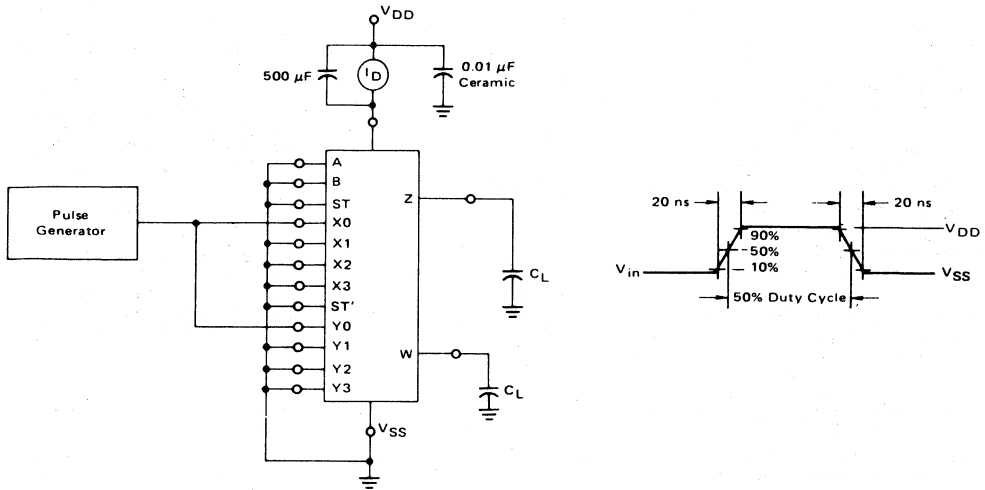


Input Connections for $t_{TLH}, t_{THL}, t_{PHL}, t_{PLH}$

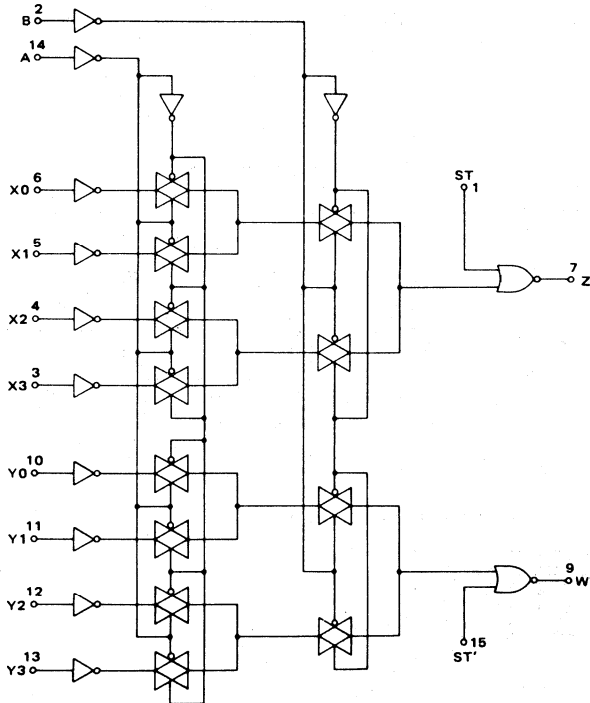
TEST	STROBE	A	X0
1	Gnd	Gnd	P. G
2	P. G.	Gnd	V _{DD}
3	Gnd	P. G.	V _{DD}

MC14539B

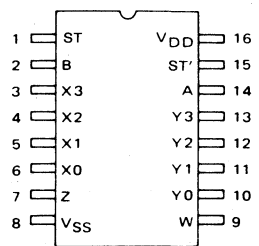
FIGURE 2 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM



LOGIC DIAGRAM



PIN ASSIGNMENT



6



MOTOROLA

MC14541B

PROGRAMMABLE TIMER

The MC14541B programmable timer consists of a 16-stage binary counter, an integrated oscillator for use with an external capacitor and two resistors, an automatic power-on reset circuit, and output control logic.

Timing is initialized by turning on power, whereupon the power-on reset is enabled and initializes the counter, within the specified V_{DD} range. With the power already on, an external reset pulse can be applied. Upon release of the initial reset command, the oscillator will oscillate with a frequency determined by the external RC network. The 16-stage counter divides the oscillator frequency (f_{osc}) with the n^{th} stage frequency being $f_{osc}/2^n$.

- Available Outputs 2^8 , 2^{10} , 2^{13} or 2^{16}
- Increments on Positive Edge Clock Transitions
- Built-in Low Power RC Oscillator
($\pm 2\%$ accuracy over temperature range and $\pm 20\%$ supply and $\pm 3\%$ over processing at < 10 kHz)
- Oscillator May Be Bypassed if External Clock Is Available (Apply external clock to Pin 3)
- External Master Reset Totally Independent of Automatic Reset Operation
- Operates as 2^n Frequency Divider or Single Transition Timer
- Q/\bar{Q} Select Provides Output Logic Level Flexibility
- Reset (auto or master) Disables Oscillator During Resetting to Provide No Active Power Dissipation
- Clock Conditioning Circuit Permits Operation with Very Slow Clock Rise and Fall Times
- Automatic Reset Initializes All Counters On Power Up
- Supply Voltage Range = 3.0 Vdc to 18 Vdc with Auto Reset Disabled (Pin 5 = V_{DD})
= 8.5 Vdc to 18 Vdc with Auto Reset Enabled (Pin 5 = V_{SS})

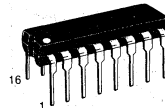
MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	-0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	-0.5 to $V_{DD} + 0.5$	V
I_{in}	Input Current (DC or Transient), per Pin	± 10	mA
I_{out}	Output Current (DC or Transient), per Pin	± 45	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

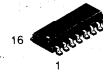
*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P and D/DW" Packages: -7.0 mW/°C From 65°C To 125°C
Ceramic "L" Packages: -12 mW/°C From 100°C To 125°C



L SUFFIX
CERAMIC
CASE 620



P SUFFIX
PLASTIC
CASE 648



D SUFFIX
SOIC
CASE 751B

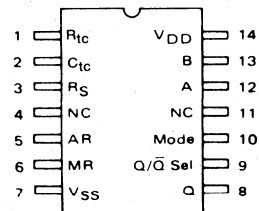
ORDERING INFORMATION

MC14XXXBCP Plastic
MC14XXXBCL Ceramic
MC14XXXBD SOIC

$T_A = -55^\circ$ to 125°C for all packages.

6

PIN ASSIGNMENT



NC = No Connection

MC14541B

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V _{DD} Vdc	-55°C		25°C			125°C		Unit
			Min	Max	Min	Typ #	Max	Min	Max	
Output Voltage V _{in} = V _{DD} or 0	V _{OL}	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
		10	—	0.05	—	0	0.05	—	0.05	
V _{in} = 0 or V _{DD}	V _{OH}	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc
		10	9.95	—	9.95	10	—	9.95	—	
Input Voltage (V _O = 4.5 or 0.5 Vdc) (V _O = 9.0 or 1.0 Vdc) (V _O = 13.5 or 1.5 Vdc)	V _{IL}	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc
		10	—	3.0	—	4.50	3.0	—	3.0	
(V _O = 0.5 or 4.5 Vdc) (V _O = 1.0 or 9.0 Vdc) (V _O = 1.5 or 13.5 Vdc)	V _{IH}	5.0	3.5	—	3.5	2.75	—	3.5	—	Vdc
		10	7.0	—	7.0	5.50	—	7.0	—	
Output Drive Current (V _{OH} = 2.5 Vdc) (V _{OH} = 9.5 Vdc) (V _{OH} = 13.5 Vdc)	Source I _{OH}	5.0	-7.96	—	-6.42	-12.83	—	-4.49	—	mAdc
		10	-4.19	—	-3.38	-6.75	—	-2.37	—	
(V _{OL} = 0.4 Vdc) (V _{OL} = 0.5 Vdc) (V _{OL} = 1.5 Vdc)	Sink I _{OL}	5.0	1.93	—	1.56	3.12	—	1.09	—	mAdc
		10	4.96	—	4.0	8.0	—	2.8	—	
15	19.3	—	15.6	31.2	—	10.9	—	—		
Input Current	I _{in}	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	μAdc
Input Capacitance (V _{in} = 0)	C _{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Pin 5 is High) Auto Reset Disabled	I _{DD}	5.0	—	5.0	—	0.005	5.0	—	150	μAdc
		10	—	10	—	0.010	10	—	300	
		15	—	20	—	0.015	20	—	600	
Auto Reset Quiescent Current (Pin 5 is low)	I _{DDR}	10	—	250	—	30	250	—	1500	μAdc
		15	—	500	—	82	500	—	2000	
Supply Current**† (Dynamic plus Quiescent)	I _D	5.0	I _D = (0.4 μA/kHz) f + I _{DD}							μAdc
		10	I _D = (0.8 μA/kHz) f + I _{DD}							
		15	I _D = (1.2 μA/kHz) f + I _{DD}							

#Data labeled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C.

†When using the on chip oscillator the total supply current (in μAdc) becomes: $I_T = I_D + 2 C_{IC} V_{DD} f \times 10^{-3}$ where I_D is in μA, C_{IC} is in pF, V_{DD} in Volts DC, and f in kHz. (see Fig. 3)
Dissipation during power-on with automatic reset enabled is typically 50 μA @ V_{DD} = 10 Vdc.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range V_{SS} ≤ (V_{in} or V_{out}) ≤ V_{DD}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

MC14541B

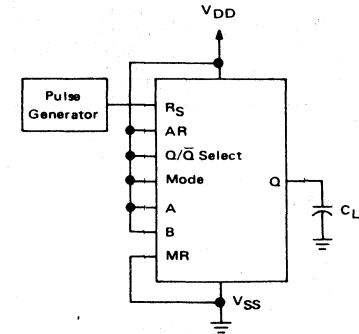
SWITCHING CHARACTERISTICS* ($C_L = 50 \text{ pF}$, $T_A = 25^\circ\text{C}$)

Characteristic	Symbol	V _{DD}	Min	Typ #	Max	Unit
Output Rise and Fall Time $t_{TLH}, t_{THL} = (1.5 \text{ ns/pF}) C_L + 25 \text{ ns}$ $t_{TLH}, t_{THL} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$ $t_{TLH}, t_{THL} = (0.55 \text{ ns/pF}) C_L + 9.5 \text{ ns}$	t_{TLH}	5.0	—	100	200	ns
	t_{THL}	10	—	50	100	
		15	—	40	80	
Propagation Delay, Clock to Q (2^8 Output) $t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 3415 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 1217 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 875 \text{ ns}$	t_{PLH}	5.0	—	3.5	10.5	μs
	t_{PHL}	10	—	1.25	3.8	
		15	—	0.9	2.9	
Propagation Delay, Clock to Q (2^{16} Output) $t_{PHL}, t_{PLH} = (1.7 \text{ ns/pF}) C_L + 5915 \text{ ns}$ $t_{PHL}, t_{PLH} = (0.66 \text{ ns/pF}) C_L + 3467 \text{ ns}$ $t_{PHL}, t_{PLH} = (0.5 \text{ ns/pF}) C_L + 2475 \text{ ns}$	t_{PHL}	5.0	—	6.0	18	μs
	t_{PLH}	10	—	3.5	10	
		15	—	2.5	7.5	
Clock Pulse Width	$t_{WH}(cl)$	5.0	900	300	—	ns
		10	300	100	—	
		15	225	85	—	
Clock Pulse Frequency (50% Duty Cycle)	f_{cl}	5.0	—	1.5	0.75	MHz
		10	—	4.0	2.0	
		15	—	6.0	3.0	
MR Pulse Width	$t_{WH}(R)$	5.0	900	300	—	ns
		10	300	100	—	
		15	225	85	—	
Master Reset Removal Time	t_{rem}	5.0	420	210	—	ns
		10	200	100	—	
		15	200	100	—	

*The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

FIGURE 1 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM



(R_{TC} and C_{TC} outputs are left open)

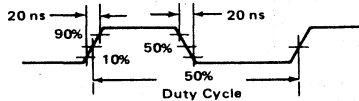
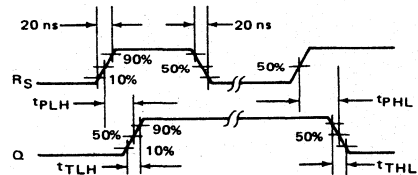
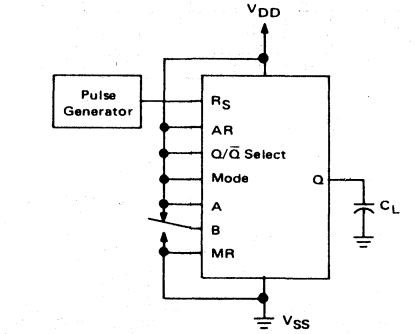
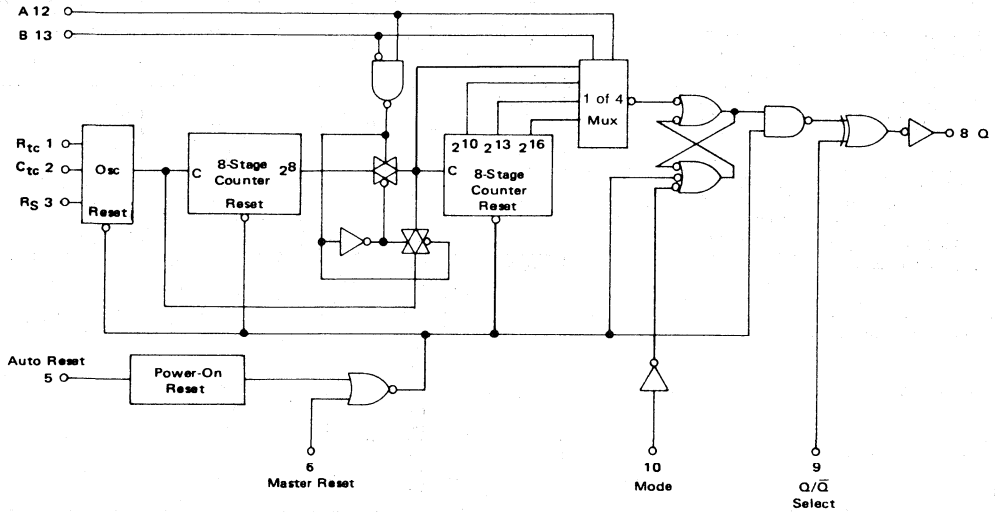


FIGURE 2 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



MC14541B

EXPANDED BLOCK DIAGRAM



V_{DD} = Pin 14
 V_{SS} = Pin 7

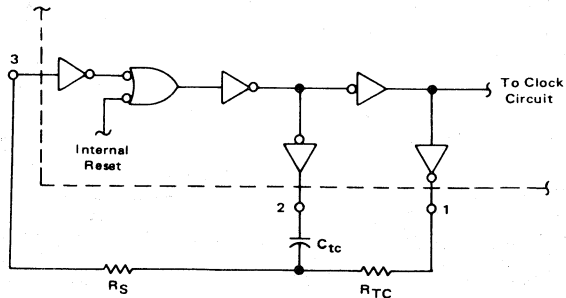
FREQUENCY SELECTION TABLE

A	B	Number of Counter Stages n	Count 2^n
0	0	13	8192
0	1	10	1024
1	0	8	256
1	1	16	65536

TRUTH TABLE

Pin	State	
	0	1
Auto Reset, 5	Auto Reset Operating	Auto Reset Disabled
Master Reset, 6	Timer Operational	Master Reset On
Q/\bar{Q} , 9	Output Initially Low After Reset	Output Initially High After Reset
Mode, 10	Single Cycle Mode	Recycle Mode

FIGURE 3 – OSCILLATOR CIRCUIT USING RC CONFIGURATION



MC14541B

TYPICAL RC OSCILLATOR CHARACTERISTICS

FIGURE 4 – RC OSCILLATOR STABILITY

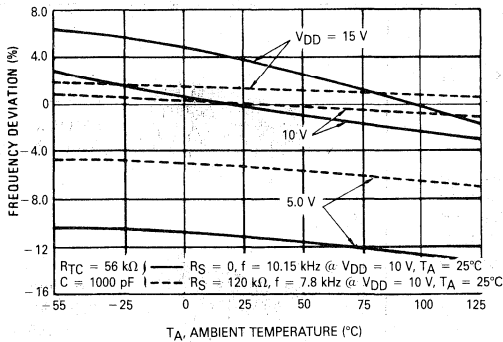
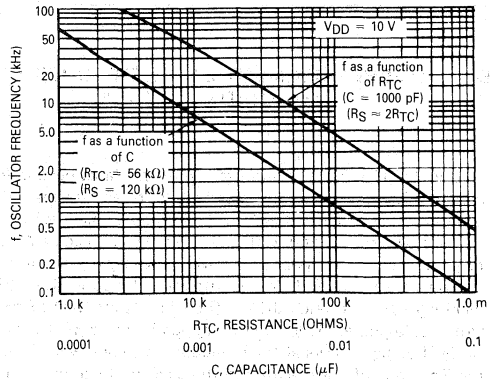


FIGURE 5 – RC OSCILLATOR FREQUENCY AS A FUNCTION OF R_{TC} AND C_{TC}



OPERATING CHARACTERISTICS

With Auto Reset pin set to a "0" the counter circuit is initialized by turning on power. Or with power already on, the counter circuit is reset when the Master Reset pin is set to a "1". Both types of reset will result in synchronously resetting all counter stages independent of counter state. Auto Reset pin when set to a "1" provides a low power operation.

The RC oscillator as shown in Figure 3 will oscillate with a frequency determined by the external RC network i.e.,

$$f = \frac{1}{2.3 R_{TC} C_{TC}} \quad \text{if } (1 \text{ kHz} \leq f \leq 100 \text{ kHz})$$

and $R_S \approx 2 R_{TC}$ where $R_S \geq 10 \text{ k}\Omega$

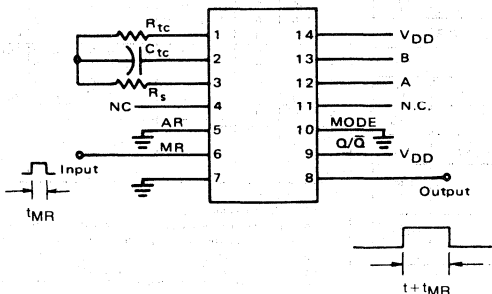
The time select inputs (A and B) provide a two-bit address to output any one of four counter stages (2⁸, 2¹⁰, 2¹³ and 2¹⁶). The 2ⁿ counts as shown in the Frequency Selection Table represents the Q output of the Nth stage of the counter. When A is "1", 2¹⁶ is selected for both

states of B. However, when B is "0", normal counting is interrupted and the 9th counter stage receives its clock directly from the oscillator (i.e., effectively outputting 2⁸).

The Q/ \bar{Q} select output control pin provides for a choice of output level. When the counter is in a reset condition and Q/ \bar{Q} select pin is set to a "0" the Q output is a "0", correspondingly when Q/ \bar{Q} select pin is set to a "1" the Q output is a "1".

When the mode control pin is set to a "1", the selected count is continually transmitted to the output. But, with mode pin "0" and after a reset condition the RS flip-flop (see Expanded Block Diagram) resets, counting commences, and after 2ⁿ⁻¹ counts the RS flip-flop sets which causes the output to change state. Hence, after another 2ⁿ⁻¹ counts the output will not change. Thus, a Master Reset pulse must be applied or a change in the mode pin level is required to reset the single cycle operation.

DIGITAL TIMER APPLICATION



When Master Reset (MR) receives a positive pulse, the internal counters and latch are reset. The Q output goes high and remains high until the selected (via A and B) number of clock pulses are counted, the Q output then goes low and remains low until another input pulse is received.

This "one shot" is fully retriggerable and as accurate as the input frequency. An external clock can be used (pin 3 is the clock input, pins 1 and 2 are outputs) if additional accuracy is needed.

Notice that a setup time equal to the desired pulse width output is required immediately following initial power up, during which time Q output will be high.



MOTOROLA

MC14543B

**BCD-TO-SEVEN SEGMENT LATCH/DECODER/DRIVER
for LIQUID CRYSTALS**

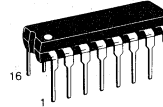
The MC14543B BCD-to-seven segment latch/decoder/driver is designed for use with liquid crystal readouts, and is constructed with complementary MOS (CMOS) enhancement mode devices. The circuit provides the functions of a 4-bit storage latch and an 8421 BCD-to-seven segment decoder and driver. The device has the capability to invert the logic levels of the output combination. The phase (Ph), blanking (BI), and latch disable (LD) inputs are used to reverse the truth table phase, blank the display, and store a BCD code, respectively. For liquid crystal (LC) readouts, a square wave is applied to the Ph input of the circuit and the electrically common backplane of the display. The outputs of the circuit are connected directly to the segments of the LC readout. For other types of readouts, such as light-emitting diode (LED), incandescent, gas discharge, and fluorescent readouts, connection diagrams are given on this data sheet.

Applications include instrument (e.g., counter, DVM etc.) display driver, computer/calculator display driver, cockpit display driver, and various clock, watch, and timer uses.

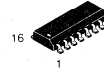
- Latch Storage of Code
- Blanking Input
- Readout Blanking on All Illegal Input Combinations
- Direct LED (Common Anode or Cathode) Driving Capability
- Supply Voltage Range = 3.0 V to 18 V
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range
- Pin-for-Pin Replacement for CD4056A (with Pin 7 Tied to V_{SS}).
- Chip Complexity: 207 FETs or 52 Equivalent Gates



**L SUFFIX
CERAMIC
CASE 620**



**P SUFFIX
PLASTIC
CASE 648**



**D SUFFIX
SOIC
CASE 751B**

ORDERING INFORMATION

- MC14XXXBCP Plastic
- MC14XXXBCL Ceramic
- MC14XXXBD SOIC

T_A = -55° to 125°C for all packages.

6

TRUTH TABLE

INPUTS				OUTPUTS							
LD	BI	Ph*	D C B A	a	b	c	d	e	f	g	Display
X	1	0	X X X X	0	0	0	0	0	0	0	Blank
1	0	0	0 0 0 0	1	1	1	1	1	1	0	0
1	0	0	0 0 0 1	0	1	1	0	0	0	0	1
1	0	0	0 0 1 0	1	1	0	1	1	0	0	2
1	0	0	0 0 1 1	1	1	1	0	0	1	0	3
1	0	0	0 1 0 0	0	1	0	0	1	0	1	4
1	0	0	0 1 0 1	1	0	1	0	1	1	1	5
1	0	0	0 1 1 0	1	0	1	1	1	1	1	6
1	0	0	0 1 1 1	1	1	1	0	0	0	0	7
1	0	0	1 0 0 0	1	1	1	1	1	1	1	8
1	0	0	1 0 0 1	1	1	1	0	1	0	1	9
1	0	0	1 0 1 0	0	0	0	0	0	0	0	Blank
1	0	0	1 0 1 1	0	0	0	0	0	0	0	Blank
1	0	0	1 1 0 0	0	0	0	0	0	0	0	Blank
1	0	0	1 1 0 1	0	0	0	0	0	0	0	Blank
1	0	0	1 1 1 0	0	0	0	0	0	0	0	Blank
1	0	0	1 1 1 1	0	0	0	0	0	0	0	Blank
0	0	0	X X X X	**	**	**	**	**	**	**	**
t	t	t	t	Inverse of Output Combinations Above							Display as above

X = Don't care
 † = Above Combinations
 * = For liquid crystal readouts, apply a square wave to Ph
 For common cathode LED readouts, select Ph = 0
 For common anode LED readouts, select Ph = 1
 ** = Depends upon the BCD code previously applied when LD = 1

MAXIMUM RATINGS* (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V _{DD}	-0.5 to +18	V
Input Voltage, All Inputs	V _{in}	-0.5 to V _{DD} + 0.5	V
DC Input Current per Pin	I _{in}	±10	mA
Operating Temperature Range	T _A	-55 to +125	°C
Power Dissipation, per Package†	P _D	500	mW
Storage Temperature Range	T _{stg}	-65 to +150	°C
Maximum Continuous Output Drive Current (Source or Sink) per Output	I _{OHmax} I _{OLmax}	10	mA
Maximum Continuous Output Power* (Source or Sink) per Output	POHmax POLmax	70	mW

*POHmax = I_{OH} (V_{OH} - V_{DD}) and POLmax = I_{OL} (V_{OL} - V_{SS})

†Maximum Ratings are those values beyond which damage to the device may occur.

‡Temperature Derating: Plastic "P and D/DW" Packages: -7.0 mW/°C From 65°C To 125°C

Ceramic "L" Packages: -12 mW/°C From 100°C To 125°C

MC14543B

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V _{DD} Vdc	-55°C		25°C			125°C		Unit
			Min	Max	Min	Typ #	Max	Min	Max	
Output Voltage V _{in} = V _{DD} or 0	"0" Level V _{OL}	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
		10	—	0.05	—	0	0.05	—	0.05	
		15	—	0.05	—	0	0.05	—	0.05	
	"1" Level V _{OH}	5.0	4.95	—	4.95	5.0	—	4.95	—	
		10	9.95	—	9.95	10	—	9.95	—	
		15	14.95	—	14.95	15	—	14.95	—	
Input Voltage (V _O = 4.5 or 0.5 Vdc) (V _O = 9.0 or 1.0 Vdc) (V _O = 13.5 or 1.5 Vdc)	"0" Level V _{IL}	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc
		10	—	3.0	—	4.50	3.0	—	3.0	
		15	—	4.0	—	6.75	4.0	—	4.0	
	"1" Level V _{IH}	5.0	3.5	—	3.5	2.75	—	3.5	—	
		10	7.0	—	7.0	5.50	—	7.0	—	
		15	11	—	11	8.25	—	11	—	
Output Drive Current (V _{OH} = 2.5 Vdc) (V _{OH} = 4.6 Vdc) (V _{OH} = 0.5 Vdc) (V _{OH} = 9.5 Vdc) (V _{OH} = 13.5 Vdc)	Source I _{OH}	5.0	-3.0	—	-2.4	-4.2	—	-1.7	—	mAdc
		5.0	-0.64	—	-0.51	-0.88	—	-0.36	—	
		10	—	—	—	-10.1	—	—	—	
		10	-1.6	—	-1.3	-2.25	—	-0.9	—	
		15	-4.2	—	-3.4	-8.8	—	-2.4	—	
		15	—	—	—	—	—	—	—	
	Sink I _{OL}	5.0	0.64	—	0.51	0.88	—	0.36	—	mAdc
		10	1.6	—	1.3	2.25	—	0.9	—	
		10	—	—	—	10.1	—	—	—	
		15	4.2	—	3.4	8.8	—	2.4	—	
		15	—	—	—	—	—	—	—	
		15	—	—	—	—	—	—	—	
Input Current	I _{in}	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	μAdc
Input Capacitance	C _{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package) V _{in} = 0 or V _{DD} , I _{out} = 0 μA	I _{DD}	5.0	—	5.0	—	0.005	5.0	—	150	μAdc
		10	—	10	—	0.010	10	—	300	
		15	—	20	—	0.015	20	—	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C _L = 50 pF on all outputs, all buffers switching)	I _T	5.0	I _T = (1.6 μA/kHz) f + I _{DD}							μAdc
		10	I _T = (3.1 μA/kHz) f + I _{DD}							
		15	I _T = (4.7 μA/kHz) f + I _{DD}							

#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 V min (α V_{DD} = 5.0 V)
2.0 V min (α V_{DD} = 10 V)
2.5 V min (α V_{DD} = 15 V)

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + 3.5 \times 10^{-3} (C_L - 50) V_{DD} f$$

where: I_T is in μA (per package), C_L in pF, V_{DD} in V, and f in kHz is input frequency.

**The formulas given are for the typical characteristics only at 25°C.

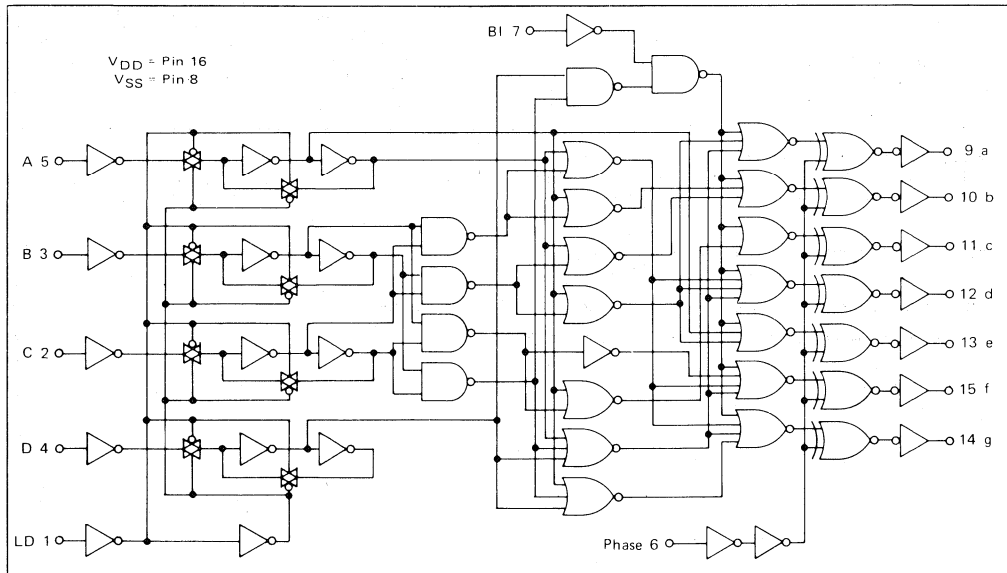
MC14543B

SWITCHING CHARACTERISTICS* ($C_L = 50 \text{ pF}$, $T_A = 25^\circ\text{C}$)

Characteristic	Symbol	V _{DD}	Min	Typ	Max	Unit
Output Rise Time $t_{TLH} = (3.0 \text{ ns/pF}) C_L + 30 \text{ ns}$ $t_{TLH} = (1.5 \text{ ns/pF}) C_L + 15 \text{ ns}$ $t_{TLH} = (1.1 \text{ ns/pF}) C_L + 10 \text{ ns}$	t_{TLH}	5.0 10 15	— — —	100 50 40	200 100 80	ns
Output Fall Time $t_{THL} = (1.5 \text{ ns/pF}) C_L + 25 \text{ ns}$ $t_{THL} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$ $t_{THL} = (0.55 \text{ ns/pF}) C_L + 12.5 \text{ ns}$	t_{THL}	5.0 10 15	— — —	100 50 40	200 100 80	ns
Turn-Off Delay Time $t_{PLH} = (1.7 \text{ ns/pF}) C_L + 520 \text{ ns}$ $t_{PLH} = (0.66 \text{ ns/pF}) C_L + 217 \text{ ns}$ $t_{PLH} = (0.5 \text{ ns/pF}) C_L + 160 \text{ ns}$	t_{PLH}	5.0 10 15	— — —	605 250 185	1210 500 370	ns
Turn-On Delay Time $t_{PHL} = (1.7 \text{ ns/pF}) C_L + 420 \text{ ns}$ $t_{PHL} = (0.66 \text{ ns/pF}) C_L + 172 \text{ ns}$ $t_{PHL} = (0.5 \text{ ns/pF}) C_L + 130 \text{ ns}$	t_{PHL}	5.0 10 15	— — —	505 205 155	1650 660 495	ns
Setup Time	t_{su}	5.0 10 15	350 450 500		— — —	ns
Hold Time	t_h	5.0 10 15	40 30 20		— — —	ns
Latch Disable Pulse Width (Strobing Data)	t_{WH}	5.0 10 15	250 100 80	125 50 40	— — —	ns

*The formulas given are for the typical characteristics only.

LOGIC DIAGRAM



MC14543B

FIGURE 1 – TYPICAL OUTPUT SOURCE CHARACTERISTICS

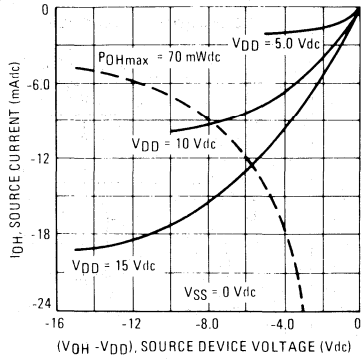


FIGURE 2 – TYPICAL OUTPUT SINK CHARACTERISTICS

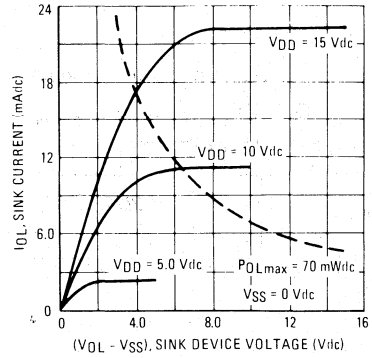


FIGURE 3 – DYNAMIC POWER DISSIPATION SIGNAL WAVEFORMS

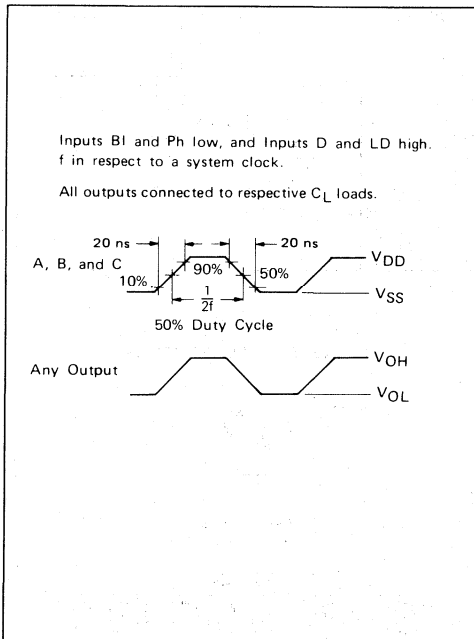
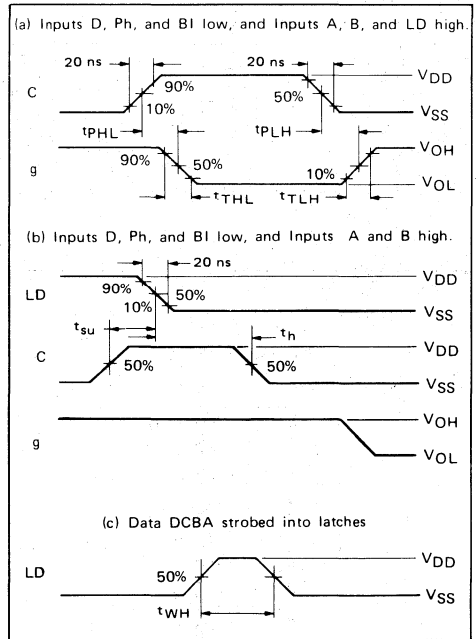
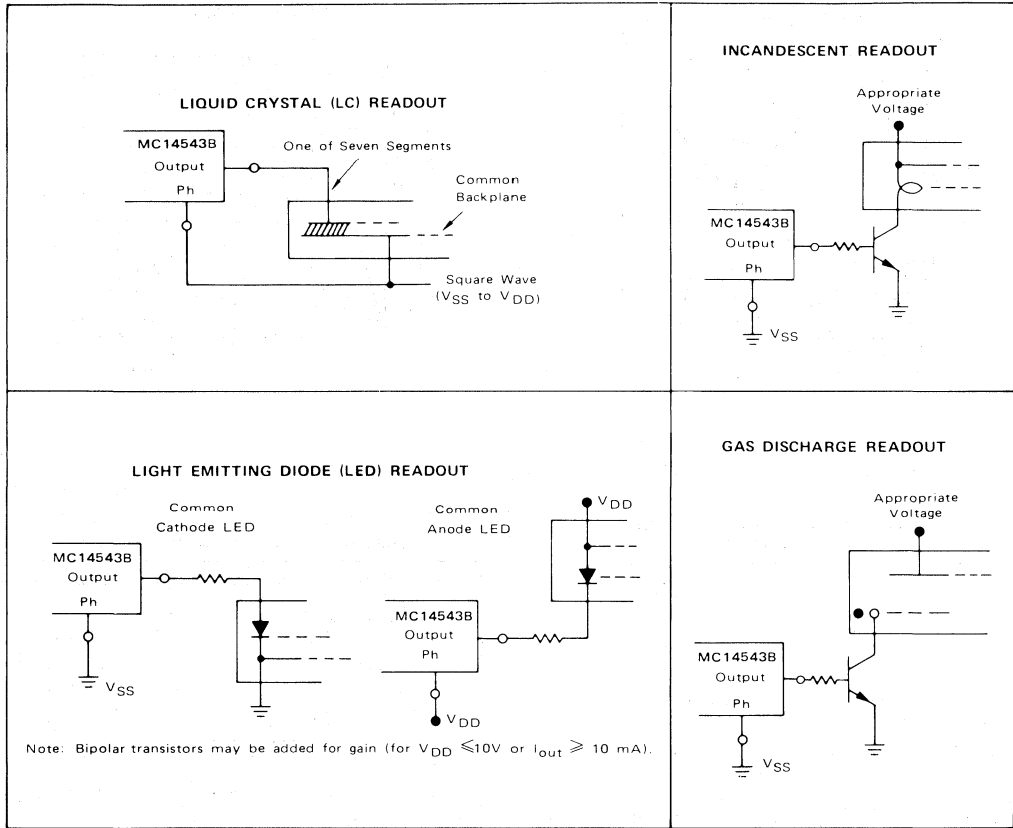


FIGURE 4 – DYNAMIC SIGNAL WAVEFORMS



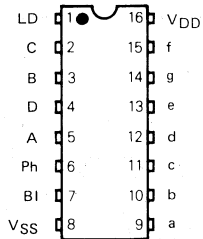
MC14543B

CONNECTIONS TO VARIOUS DISPLAY READOUTS



6

PIN ASSIGNMENT

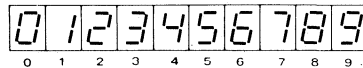


CONNECTIONS TO SEGMENTS



V_{DD} = Pin 16
 V_{SS} = Pin 8

DISPLAY





MC14544B

BCD-TO-SEVEN SEGMENT LATCH/DECODER/DRIVER FOR LIQUID CRYSTALS

The MC14544B BCD-to-seven segment latch/decoder/driver is designed for use with liquid crystal readouts, and is constructed with complementary MOS (CMOS) enhancement mode devices. The circuit provides the functions of a 4-bit storage latch and an 8421 BCD-to-seven segment decoder and driver. The device has the capability to invert the logic levels of the output combination. The phase (Ph), blanking (BI), and latch disable (LD) inputs are used to reverse the truth table phase, blank the display, and store a BCD code, respectively. For liquid crystal (LC) readouts, a square wave is applied to the Ph input of the circuit and the electrically common backplane of the display. The outputs of the circuit are connected directly to the segments of the LC readout. The Ripple Blanking Input (RBI) and the Ripple Blanking Output (RBO) can be used to suppress either leading or trailing zeroes.

For other types of readouts, such as light-emitting diode (LED), incandescent, gas discharge, and fluorescent readouts, connection diagrams are given on this data sheet.

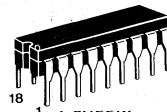
Applications include instrument (e.g., counter, DVM etc.) display driver, computer/calculator display driver, cockpit display driver, and various clock, watch, and timer uses.

- Latch Storage of Code
- Blanking Input
- Readout Blanking on All Illegal Input Combinations
- Direct LED (Common Anode or Cathode) Driving Capability
- Supply Voltage Range = 3.0 V to 18 V
- Capability for Suppression of Non-significant zero
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

BCD-TO-SEVEN SEGMENT LATCH/DECODER/DRIVER WITH RIPPLE BLANKING



L SUFFIX
CERAMIC PACKAGE
CASE 726



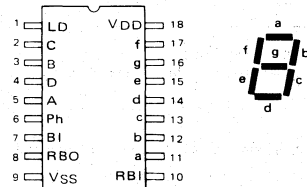
P SUFFIX
PLASTIC PACKAGE
CASE 707

ORDERING INFORMATION

MC14XXXBCP (Plastic Package)
MC14XXXBCL (Ceramic Package)

T_A = -55°C to +125°C for all packages

PIN ASSIGNMENT



MAXIMUM RATINGS* (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V _{DD}	-0.5 to +18	V
Input Voltage, All Inputs	V _{in}	-0.5 to V _{DD} + 0.5	V
DC Input Current per Pin	I _{in}	±10	mAdc
Operating Temperature Range	T _A	-55 to +125	°C
Power Dissipation, per Package†	P _D	500	mW
Storage Temperature Range	T _{stg}	-65 to +150	°C
Maximum Continuous Output Drive Current (Source or Sink) per Output	I _{OHmax} I _{OLmax}	10	mAdc
Maximum Continuous Output Power* (Source or Sink) per Output	P _{OHmax} P _{OLmax}	70	mW

*P_{OHmax} = I_{OH} (V_{OH} - V_{DD}) and P_{OLmax} = I_{OL} (V_{OL} - V_{SS})

†Maximum Ratings are those values beyond which damage to the device may occur.

†Temperature Derating: Plastic "P and D/DW" Packages: -7.0 mW/°C From 65°C To 125°C

Ceramic "L" Packages: -12 mW/°C From 100°C To 125°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range V_{SS} ≤ (V_{in} or V_{out}) ≤ V_{DD}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

MC14544B

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V _{DD} Vdc	-55°C		25°C			125°C		Unit	
			Min	Max	Min	Typ #	Max	Min	Max		
Output Voltage V _{in} = V _{DD} or 0	VOL	5.0	—	0.05	—	0	0.05	—	0.05	Vdc	
		10	—	0.05	—	0	0.05	—	0.05		
		15	—	0.05	—	0	0.05	—	0.05		
	V _{in} = 0 or V _{DD}	VOH	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc
			10	9.95	—	9.95	10	—	9.95	—	
			15	14.95	—	14.95	15	—	14.95	—	
Input Voltage # (V _O = 4.5 or 0.5 Vdc) (V _O = 9.0 or 1.0 Vdc) (V _O = 13.5 or 1.5 Vdc)	V _{IL}	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc	
		10	—	3.0	—	4.50	3.0	—	3.0		
		15	—	4.0	—	6.75	4.0	—	4.0		
	(V _O = 0.5 or 4.5 Vdc) (V _O = 1.0 or 9.0 Vdc) (V _O = 1.5 or 13.5 Vdc)	V _{IH}	5.0	3.5	—	3.5	2.75	—	3.5	—	Vdc
			10	7.0	—	7.0	5.50	—	7.0	—	
			15	11	—	11	8.25	—	11	—	
Output Drive Current (V _{OH} = 2.5 Vdc) (V _{OH} = 4.6 Vdc) (V _{OH} = 0.5 Vdc) (V _{OH} = 9.5 Vdc) (V _{OH} = 13.5 Vdc)	Source	I _{OH}	5.0	-3.0	—	-2.4	-4.2	—	-1.7	—	mAdc
			5.0	-0.64	—	-0.51	-0.88	—	-0.36	—	
			10	—	—	—	—	—	—	—	
			10	-1.6	—	-1.3	-2.25	—	-0.9	—	
			10	-4.2	—	-3.4	-8.8	—	-2.4	—	
			15	—	—	—	—	—	—	—	
	Sink (V _{OL} = 0.4 Vdc) (V _{OL} = 0.5 Vdc) (V _{OL} = 9.5 Vdc) (V _{OL} = 1.5 Vdc)	I _{OL}	5.0	0.64	—	0.51	0.88	—	0.36	—	mAdc
			10	1.6	—	1.3	2.25	—	0.9	—	
			10	—	—	—	10.1	—	—	—	
			10	—	—	—	—	—	—	—	
			10	—	—	—	—	—	—	—	
			15	4.2	—	3.4	8.8	—	2.4	—	
Input Current	I _{in}	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	μAdc	
Input Capacitance	C _{in}	—	—	—	—	5.0	7.5	—	—	pF	
Quiescent Current (Per Package) V _{in} = 0 or V _{DD} , I _{out} = 0 μA	I _{DD}	5.0	—	5.0	—	0.005	5.0	—	150	μAdc	
		10	—	10	—	0.010	10	—	300		
		15	—	20	—	0.015	20	—	600		
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C _L = 50 pF on all outputs, all buffers switching)	I _T	5.0	I _T = (1.6 μA/kHz) f + I _{DD}							μAdc	
		10	I _T = (3.1 μA/kHz) f + I _{DD}								
		15	I _T = (4.7 μA/kHz) f + I _{DD}								

#Noise immunity specified for worst-case input combination.

Noise Margin for both "1" and "0" level = 1.0 V min (α V_{DD} = 5.0 V)
2.0 V min (α V_{DD} = 10 V)
2.5 V min (α V_{DD} = 15 V)

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + 3.5 \times 10^{-3} (C_L - 50) V_{DD} f$$

where: I_T is in μA (per package), C_L in pF, V_{DD} in V, and f in kHz is input frequency.

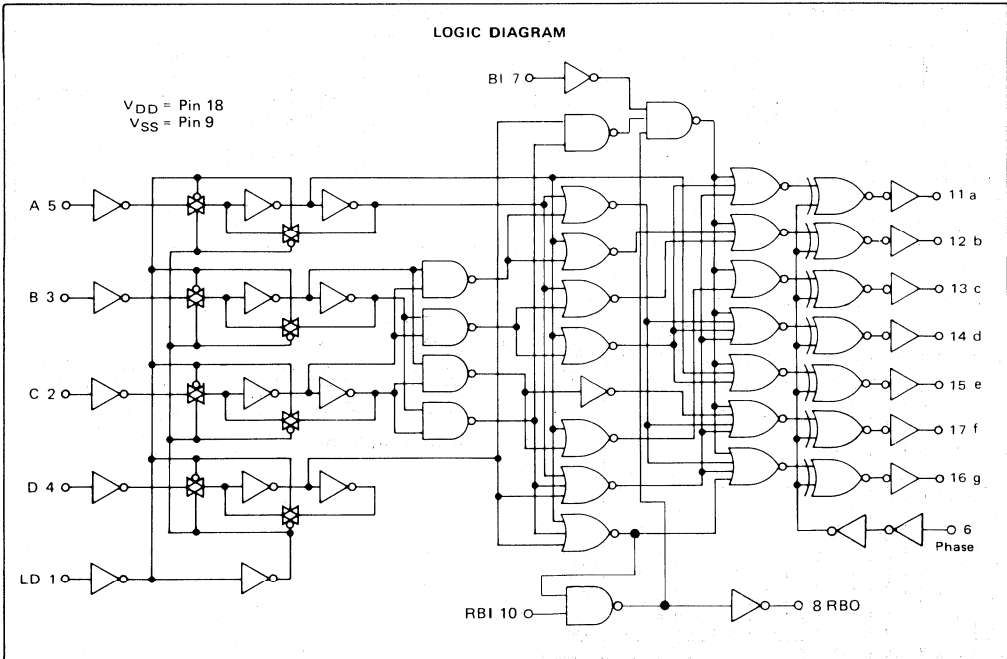
**The formulas given are for the typical characteristics only at 25°C.

MC14544B

SWITCHING CHARACTERISTICS* ($C_L = 50 \text{ pF}$, $T_A = 25^\circ\text{C}$)

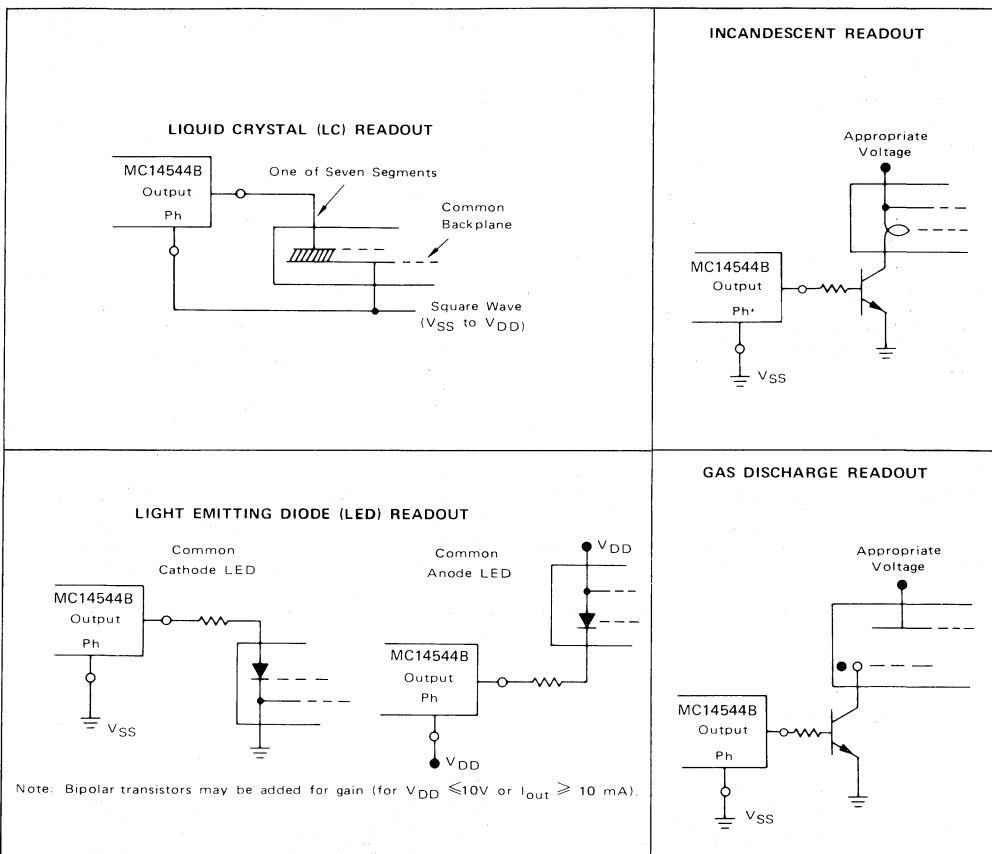
Characteristic	Symbol	V _{DD}	Min	Typ	Max	Unit
Output Rise Time $t_{TLH} = (3.0 \text{ ns/pF}) C_L + 30 \text{ ns}$ $t_{TLH} = (1.5 \text{ ns/pF}) C_L + 15 \text{ ns}$ $t_{TLH} = (1.1 \text{ ns/pF}) C_L + 10 \text{ ns}$	t_{TLH}	5.0 10 15	— — —	100 50 40	200 100 80	ns
Output Fall Time $t_{THL} = (1.5 \text{ ns/pF}) C_L + 25 \text{ ns}$ $t_{THL} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$ $t_{THL} = (0.55 \text{ ns/pF}) C_L + 12.5 \text{ ns}$	t_{THL}	5.0 10 15	— — —	100 50 40	200 100 80	ns
Turn-Off Delay Time $t_{PLH} = (1.7 \text{ ns/pF}) C_L + 520 \text{ ns}$ $t_{PLH} = (0.66 \text{ ns/pF}) C_L + 217 \text{ ns}$ $t_{PLH} = (0.5 \text{ ns/pF}) C_L + 160 \text{ ns}$	t_{PLH}	5.0 10 15	— — —	605 250 185	1210 500 370	ns
Turn-On Delay Time $t_{PHL} = (1.7 \text{ ns/pF}) C_L + 420 \text{ ns}$ $t_{PHL} = (0.66 \text{ ns/pF}) C_L + 172 \text{ ns}$ $t_{PHL} = (0.5 \text{ ns/pF}) C_L + 130 \text{ ns}$	t_{PHL}	5.0 10 15	— — —	505 205 155	1650 660 495	ns
Setup Time	t_{su}	5.0 10 15	0 0 0	-40 -15 -10	— — —	ns
Hold Time	t_h	5.0 10 15	80 30 20	40 15 10	— — —	ns
Latch Disable Pulse Width (Strobing Data)	t_{WH}	5.0 10 15	250 100 80	125 50 40	— — —	ns

*The formulas given are for the typical characteristics only.



MC14544B

CONNECTIONS TO VARIOUS DISPLAY READOUTS



6

TRUTH TABLE

INPUTS						OUTPUTS														
RBI	LD	BI	Ph*	D	C	B	A	RBO	a	b	c	d	e	f	g	DISPLAY				
X	X	1	0	X	X	X	X	≡	0	0	0	0	0	0	0	Blank				
0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	Blank				
0	1	0	0	0	0	0	0	0	0	1	1	1	1	1	0	0				
X	1	0	0	0	0	0	1	0	0	1	1	0	0	0	0	1				
X	1	0	0	0	0	1	0	0	1	1	0	1	1	0	1	2				
X	1	0	0	0	0	1	1	0	1	1	1	0	0	1	0	3				
X	1	0	0	0	1	0	0	0	0	1	1	0	0	1	1	4				
X	1	0	0	0	1	0	1	0	1	0	1	1	0	1	1	5				
X	1	0	0	0	1	1	1	0	0	1	0	1	1	1	1	6				
X	1	0	0	0	0	1	1	1	0	1	1	0	0	0	0	7				
X	1	0	0	1	0	0	0	0	1	1	1	1	1	1	1	8				
X	1	0	0	1	0	0	1	0	1	1	1	0	0	1	1	9				
X	1	0	0	1	1	1	0	0	0	0	0	0	0	0	0	Blank				
X	1	0	0	1	0	1	1	0	0	0	0	0	0	0	0	Blank				
X	1	0	0	1	1	0	0	0	0	0	0	0	0	0	0	Blank				
X	1	0	0	1	1	1	0	0	0	0	0	0	0	0	0	Blank				
X	0	0	0	X	X	X	X	≡								**				
†	†	†	†	†	†	†	†		Inverse of Output						†	†	†	†	†	
									Continuation Above											

- X Don't Care
- † Above Combinations
- * For liquid crystal readouts, apply a square wave to Ph. For common cathode LED readouts, select Ph = 0. For common anode LED readouts, select Ph = 1.
- ** Depends upon the BCD Code previously applied when LD = 1.
- ≡ RBO = RBI • (A \bar{B} C \bar{D})

MC14544B

FIGURE 1 – TYPICAL OUTPUT SOURCE CHARACTERISTICS

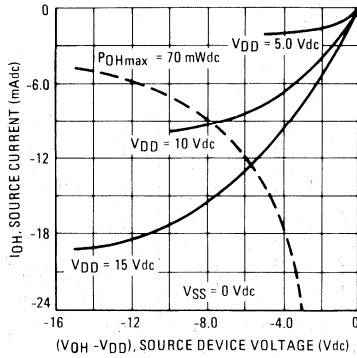


FIGURE 2 – TYPICAL OUTPUT SINK CHARACTERISTICS

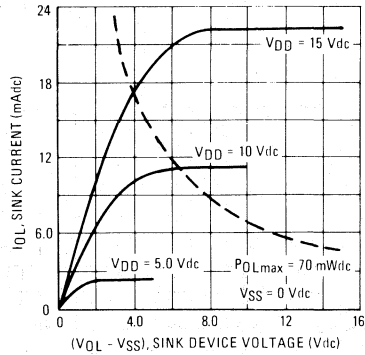


FIGURE 3 – DYNAMIC POWER DISSIPATION SIGNAL WAVEFORMS

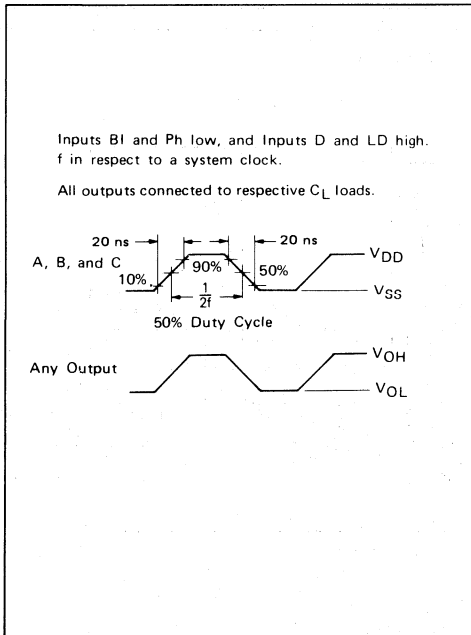
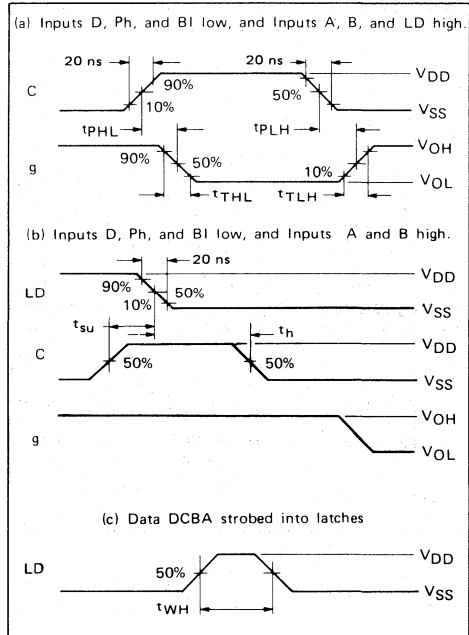
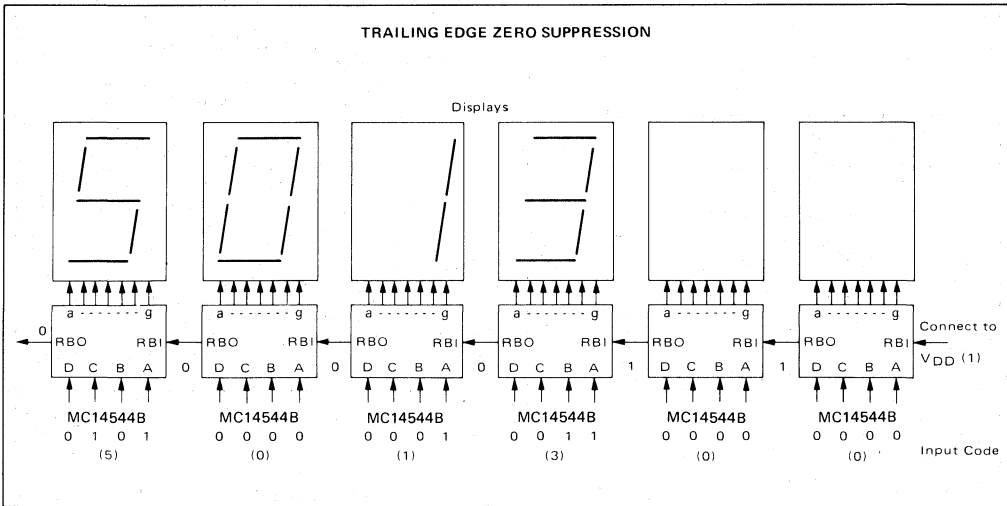
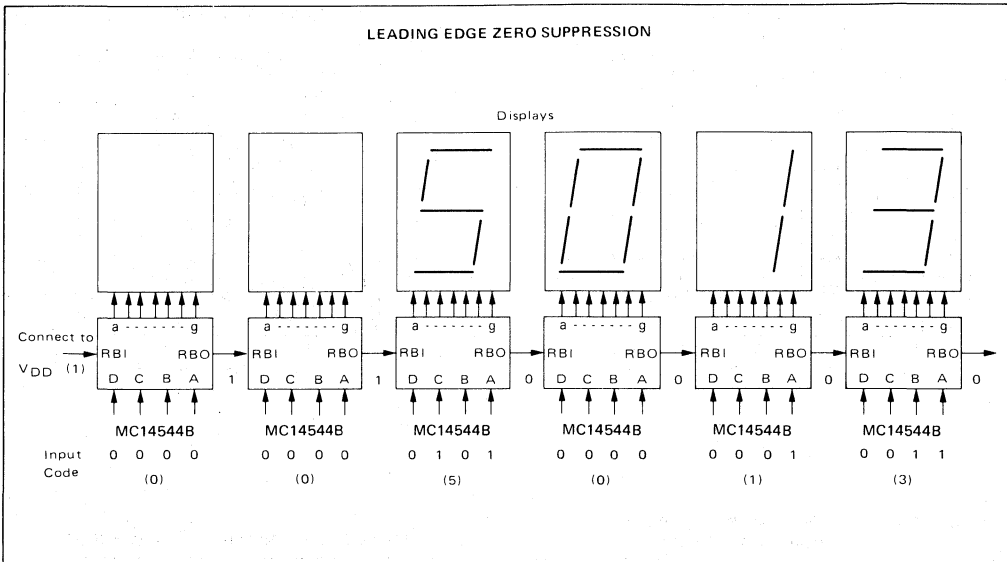


FIGURE 4 – DYNAMIC SIGNAL WAVEFORMS



MC14544B

TYPICAL APPLICATIONS FOR RIPPLE BLANKING





MOTOROLA

**HIGH CURRENT
BCD-TO-SEVEN SEGMENT DECODER/DRIVER**

The MC14547 BCD-to-seven segment decoder/driver is constructed with complementary MOS (CMOS) enhancement mode devices and NPN bipolar output drivers in a single monolithic structure. The circuit provides the functions of an 8421 BCD-to-seven segment decoder with high output drive capability. Blanking (BI), can be used to turn off or pulse modulate the brightness of the display. The MC14547 can drive seven-segment light-emitting diodes (LED), incandescent, fluorescent or gas discharge readouts either directly or indirectly.

Applications include instrument (e.g., counter, DVM, etc.) display driver, computer/calculator display driver, cockpit display driver, and various clock, watch, and timer uses.

- High Current Sourcing Outputs (Up to 65 mA)
- Low Logic Circuit Power Dissipation
- Supply Voltage Range = +3.0 V to +18 V
- Blanking Input
- Readout Blanking on All Illegal Combinations
- Lamp Intensity Modulation Capability
- Multiplexing Capability
- Capable of Driving Two Low-Power TTL Loads, One Low-Power Schottky TTL Load or Two HTL Loads over the Rated Temperature Range
- Use MC14511B for Applications Requiring Data Latches

MAXIMUM RATINGS * (Voltage referenced to V_{SS}, Pin 8)

Rating	Symbol	Value	Unit
DC Supply Voltage	V _{DD}	-0.5 to +18	V
Input Voltage, All Inputs	V _{in}	-0.5 to V _{DD} + 0.5	V
Operating Temperature Range	T _A	-55 to +125	°C
Storage Temperature Range	T _{stg}	-65 to +150	°C
Maximum Continuous Output Drive Current (Source) per Output	I _{OHmax}	65	mA
Maximum Continuous Power Dissipation	P _D	1200*	mW

*Maximum Ratings are those values beyond which damage to the device may occur.

*See Power Derating Curve Figure 1.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. A destructive high current mode may occur if V_{in} and V_{out} is not constrained to the range V_{SS} ≤ (V_{in} or V_{out}) ≤ V_{DD}.

Due to the sourcing capability of this circuit, damage can occur to the device if V_{DD} is applied, and the outputs are shorted to V_{SS} and are at a logical 1 (See Maximum Ratings).

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

MC14547B



**L SUFFIX
CERAMIC
CASE 620**



**P SUFFIX
PLASTIC
CASE 648**

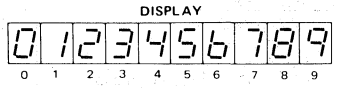
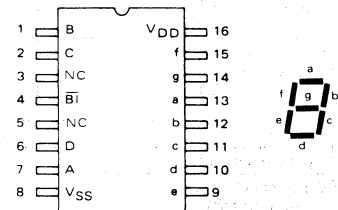


**DW SUFFIX
SOIC
CASE 751G**

ORDERING INFORMATION

MC14XXXBCP Plastic
MC14XXXBCL Ceramic
MC14XXXBDW SOIC

T_A = -55° to 125°C for all packages.



TRUTH TABLE

INPUTS				OUTPUTS							
BI	D	C	B A	a	b	c	d	e	f	g	DISPLAY
0	X	X	X X	0	0	0	0	0	0	0	Blank
1	0	0	0 0	1	1	1	1	1	0	0	0
1	0	0	0 1	0	1	1	0	0	0	0	1
1	0	1	0 0	1	1	0	1	0	1	0	2
1	0	1	0 1	1	1	1	0	0	1	0	3
1	1	0	0 0	0	1	1	0	0	1	1	4
1	1	0	0 1	1	0	1	1	0	1	1	5
1	1	1	0 0	0	0	1	1	1	1	1	6
1	1	1	0 1	1	1	0	0	0	0	0	7
1	1	0	0 0	1	1	1	1	1	1	1	8
1	1	0	0 1	1	1	1	0	0	1	1	9
1	1	1	0 1	0	0	0	0	0	0	0	Blank
1	1	0	1 1	0	0	0	0	0	0	0	Blank
1	1	1	0 0	0	0	0	0	0	0	0	Blank
1	1	1	0 1	0	0	0	0	0	0	0	Blank
1	1	1	1 0	0	0	0	0	0	0	0	Blank
1	1	1	1 1	0	0	0	0	0	0	0	Blank

X = Don't care

MC14547B

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V _{DD} Vdc	-55°C		25°C			125°C		Unit		
			Min	Max	Min	Typ #	Max	Min	Max			
Output Voltage V _{in} = V _{DD} or 0	V _{OL}	5.0	—	0.05	—	0	0.05	—	0.05	Vdc		
		10	—	0.05	—	0	0.05	—	0.05			
V _{in} = 0 or V _{DD}	V _{OH}	5.0	4.1	—	4.4	4.6	—	4.3	—	Vdc		
		10	9.1	—	9.4	9.6	—	9.3	—			
Input Voltage # (V _O = 3.8 or 0.5 Vdc) (V _O = 8.8 or 1.0 Vdc) (V _O = 13.8 or 1.5 Vdc)	V _{IL}	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc		
		10	—	3.0	—	4.50	3.0	—	3.0			
(V _O = 13.8 or 1.5 Vdc)	V _{IH}	5.0	—	4.0	—	6.75	4.0	—	4.0	Vdc		
		10	3.5	—	3.5	2.75	—	3.5	—			
(V _O = 1.0 or 8.8 Vdc) (V _O = 1.5 or 13.8 Vdc)	V _{IH}	10	7.0	—	7.0	5.50	—	7.0	—	Vdc		
		15	11	—	11	8.25	—	11	—			
Output Drive Voltage Source (I _{OH} = 5.0 mA) (I _{OH} = 10 mA) (I _{OH} = 20 mA) (I _{OH} = 40 mA) (I _{OH} = 65 mA)	V _{OH}	5.0	4.0	—	4.2	4.3	—	4.3	—	Vdc		
			—	—	4.1	4.3	—	—	—			
			3.8	—	3.9	4.2	—	4.0	—			
		10	—	—	9.2	9.3	—	9.3	—	9.3	Vdc	
			—	—	9.1	9.3	—	—	—			
			8.8	—	9.0	9.2	—	9.2	—			
		15	—	—	8.9	9.0	—	—	—	—	Vdc	
			—	—	8.9	9.0	—	—	—			
			8.4	—	8.5	8.8	—	8.1	—			
		(I _{OH} = 5.0 mA) (I _{OH} = 10 mA) (I _{OH} = 20 mA) (I _{OH} = 40 mA) (I _{OH} = 65 mA)	V _{OH}	15	14	—	14.2	14.3	—	14.4	—	Vdc
					—	—	14.1	14.3	—	—	—	
					13.8	—	14.0	14.2	—	14.2	—	
(I _{OH} = 5.0 mA) (I _{OH} = 10 mA) (I _{OH} = 20 mA) (I _{OH} = 40 mA) (I _{OH} = 65 mA)	V _{OH}	15	—	—	13.8	14.0	—	—	—	Vdc		
			—	—	13.8	14.0	—	—	—			
			13.5	—	13.5	13.7	—	13.3	—			
Output Drive Current (V _{OL} = 0.4 Vdc) (V _{OL} = 0.5 Vdc) (V _{OL} = 1.5 Vdc)	Sink	I _{OL}	5.0	0.32	—	0.26	0.44	—	0.18	—	mAdc	
10	0.80	—	0.65	1.13	—	0.45	—					
15	2.10	—	1.7	4.4	—	1.2	—					
Input Current	I _{in}	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	—	μAdc	
Input Capacitance	C _{in}	—	—	—	—	5.0	7.5	—	—	—	pF	
Quiescent Current (Per Package) V _{in} = 0 or V _{DD} , I _{out} = 0 μA	I _{DD}	5.0	—	5.0	—	0.005	5.0	—	150	—	μAdc	
		10	—	10	—	0.010	10	—	300	—		
		15	—	20	—	0.015	20	—	600	—		
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C _L = 50 pF on all outputs, all buffers switching)	I _T	5.0				I _T = (1.9 μA/kHz) f + I _{DD}					μAdc	
		10				I _T = (3.8 μA/kHz) f + I _{DD}						
		15				I _T = (5.7 μA/kHz) f + I _{DD}						

#Noise immunity specified for worst-case input combination.

Noise Margin for both "1" and "0" level = 1.0 V min (α V_{DD} = 5.0 V)
2.0 V min (α V_{DD} = 10 V)
2.5 V min (α V_{DD} = 15 V)

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + 3.5 \times 10^{-3} (C_L - 50) V_{DD} f$$

where: I_T is in μA (per package), C_L in pF, V_{DD} in V, and f in kHz is input frequency.

**The formulas given are for the typical characteristics only at 25°C.

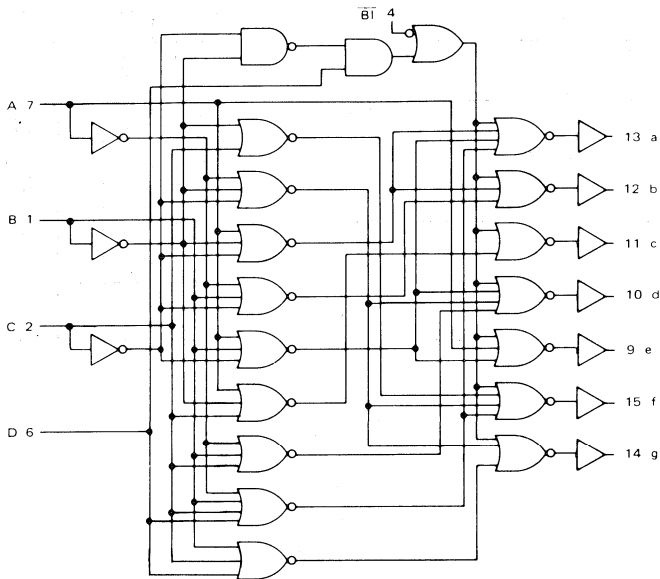
MC14547B

SWITCHING CHARACTERISTICS ($C_L = 50 \text{ pF}$, $T_A = 25^\circ\text{C}$)

Characteristic	Symbol	V _{DD} V _{dC}	Min	Typ	Max	Unit
Output Rise Time	t _{TLH}	5.0	—	40	80	ns
		10	—	40	80	
		15	—	40	80	
Output Fall Time	t _{THL}	5.0	—	125	250	ns
		10	—	75	150	
		15	—	70	140	
Data Propagation Delay Time	t _{PLH}	5.0	—	750	1500	ns
		10	—	300	600	
		15	—	200	400	
	t _{PHL}	5.0	—	750	1500	
		10	—	300	600	
		15	—	200	400	
Blank Propagation Delay Time	t _{PLH}	5.0	—	750	1500	ns
		10	—	300	600	
		15	—	200	400	
	t _{PHL}	5.0	—	500	1000	
		10	—	250	500	
		15	—	170	340	

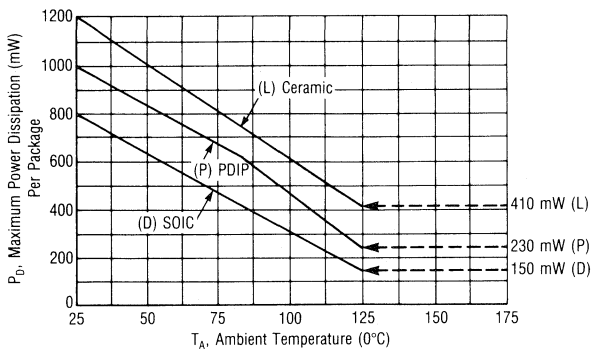
MC14547B

LOGIC DIAGRAM



6

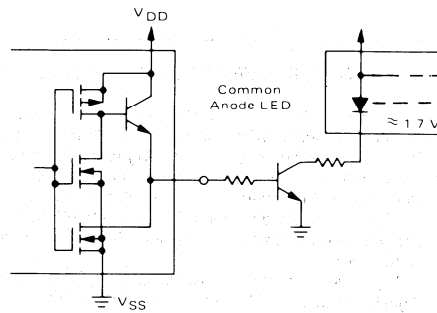
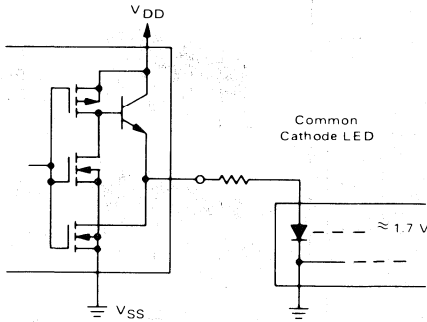
FIGURE 1 — AMBIENT TEMPERATURE POWER DERATING



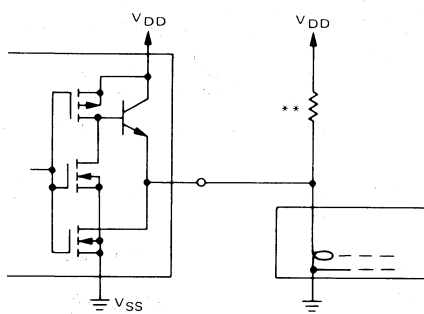
MC14547B

CONNECTIONS TO VARIOUS DISPLAY READOUTS

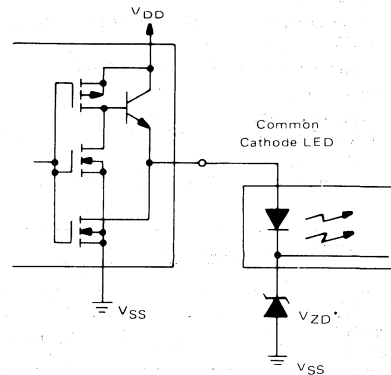
LIGHT EMITTING DIODE (LED) READOUT



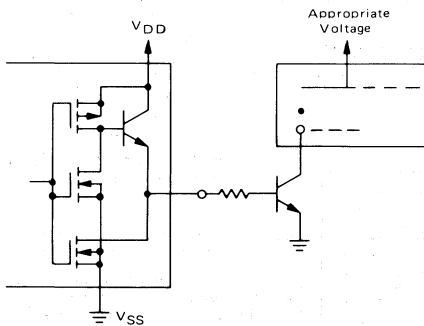
INCANDESCENT READOUT



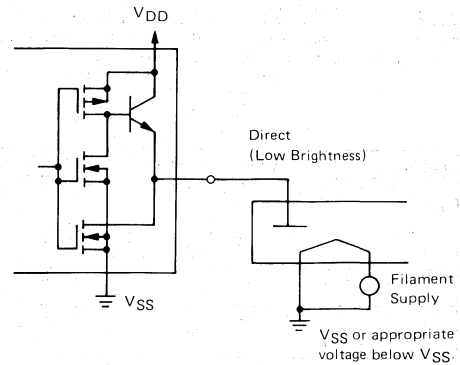
LIGHT-EMITTING DIODE (LED) READOUT USING A ZENER DIODE TO REPLACE DROPPING RESISTORS



GAS DISCHARGE READOUT



FLUORESCENT READOUT



* V_{ZD} should be set at $V_{DD} - 1.3V - V_{LED}$. Wattage of zener diode must be calculated for number of segments and worst-case conditions.

** A filament pre-warm resistor is recommended to reduce filament thermal shock and increase the effective cold resistance of the filament.

V_{SS} or appropriate voltage below V_{SS} .
(Caution: Absolute maximum working voltage = 18.0 V)



MOTOROLA

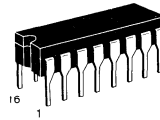
**MC14549B
MC14559B**

SUCCESSIVE APPROXIMATION REGISTERS

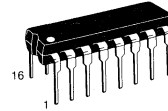
The MC14549B and MC14559B successive approximation registers are 8-bit registers providing all the digital control and storage necessary for successive approximation analog-to-digital conversion systems. These parts differ in only one control input. The Master Reset (MR) on the MC14549B is required in the cascaded mode when more than 8 bits are desired. The Feed Forward (FF) of the MC14559B is used for register shortening where End-of-Conversion (EOC) is required after less than eight cycles.

Applications for the MC14549B and MC14559B include analog-to-digital conversion, with serial and parallel outputs.

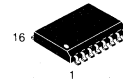
- Totally Synchronous Operation
- All Outputs Buffered
- Single Supply Operation
- Serial Output
- Retriggerable
- Compatible with a Variety of Digital and Analog Systems such as the MC1408 8-Bit D/A Converter
- All Control Inputs Positive-Edge Triggered
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-Power TTL Loads, One Low-Power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range
- Chip Complexity: 488 FETs or 122 Equivalent Gates



**L SUFFIX
CERAMIC
CASE 620**



**P SUFFIX
PLASTIC
CASE 648**



**DW SUFFIX
SOIC
CASE 751G**

ORDERING INFORMATION

MC14XXXBCP Plastic
MC14XXXBCL Ceramic
MC14XXXBDW SOIC

T_A = -55° to 125°C for all packages.

MAXIMUM RATINGS* (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V _{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V _{in}	-0.5 to V _{DD} +0.5	Vdc
DC Input Current, per Pin	I _{in}	± 10	mAdc
Power Dissipation, per Package†	P _D	500	mW
Operating Temperature Range	T _A	-55 to +125	°C
Storage Temperature Range	T _{stg}	-65 to +150	°C

*Maximum Ratings are those values beyond which damage to the device may occur.

†Temperature Derating: Plastic "P and D/DW" Packages: -7.0 mW/°C From 65°C To 125°C
Ceramic "L" Packages: -12 mW/°C From 100°C To 125°C

TRUTH TABLES

MC14549B

SC	SC _(t-1)	MR	MR _(t-1)	Clock	Action
X	X	X	X		None
X	X	1	X		Reset
1	0	0	0		Start Conversion
1	X	0	1		Start Conversion
1	1	0	0		Continue Conversion
0	X	0	X		Continue Previous Operation

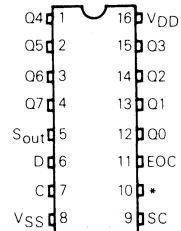
X = Don't Care

t-1 = State at Previous Clock

MC14559B

SC	SC _(t-1)	EOC	Clock	Action
X	X	X		None
1	0	0		Start Conversion
X	1	0		Continue Conversion
0	0	0		Continue Conversion
0	X	1		Retain Conversion Result
1	X	1		Start Conversion

PIN ASSIGNMENT



* For MC14549B Pin 10 is MR input
For MC14559B Pin 10 is FF input

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range V_{SS} ≤ (V_{in} or V_{out}) ≤ V_{DD}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

MC14549B, MC14559B

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V _{DD} V _{dC}	-55°C		25°C			125°C		Unit		
			Min	Max	Min	Typ #	Max	Min	Max			
Output Voltage V _{in} = V _{DD} or 0	"0" Level V _{OL}	5.0	—	0.05	—	0	0.05	—	0.05	V _{dC}		
		10	—	0.05	—	0	0.05	—	0.05			
		15	—	0.05	—	0	0.05	—	0.05			
	"1" Level V _{OH}	5.0	4.95	—	4.95	5.0	—	4.95	—			
		10	9.95	—	9.95	10	—	9.95	—			
		15	14.95	—	14.95	15	—	14.95	—			
Input Voltage # (V _O = 4.5 or 0.5 V _{dC}) (V _O = 9.0 or 1.0 V _{dC}) (V _O = 13.5 or 1.5 V _{dC})	"0" Level V _{IL}	5.0	—	1.5	—	2.25	1.5	—	1.5	V _{dC}		
		10	—	3.0	—	4.50	3.0	—	3.0			
		15	—	4.0	—	6.75	4.0	—	4.0			
	"1" Level (V _O = 0.5 or 4.5 V _{dC}) (V _O = 1.0 or 9.0 V _{dC}) (V _O = 1.5 or 13.5 V _{dC})	V _{IH}	5.0	3.5	—	3.5	2.75	—	3.5		—	
			10	7.0	—	7.0	5.50	—	7.0		—	
			15	11	—	11	8.25	—	11		—	
Output Drive Current (V _{OH} = 2.5 V _{dC}) (V _{OH} = 4.6 V _{dC}) (V _{OH} = 9.5 V _{dC}) (V _{OH} = 13.5 V _{dC})	Source I _{OH}	5.0	-1.2	—	-1.0	-1.7	—	-0.7	—	m _{AdC}		
		5.0	-0.25	—	-0.2	-0.36	—	-0.14	—			
		10	-0.62	—	-0.5	-0.9	—	-0.35	—			
	Sink Q Outputs I _{OL}	5.0	1.28	—	1.02	1.76	—	0.72	—			
		10	3.2	—	2.6	4.5	—	1.8	—			
		15	8.4	—	6.8	17.6	—	4.8	—			
	Sink Pin 5, 11 only I _{OL}	5.0	0.64	—	0.51	0.88	—	0.36	—			
		10	1.6	—	1.3	2.25	—	0.9	—			
		15	4.2	—	3.4	8.8	—	2.4	—			
	Input Current	I _{in}	15	—	±0.1	—	±0.00001	±0.1	—		±1.0	μ _{AdC}
	Input Capacitance	C _{in}	—	—	—	—	5.0	7.5	—		—	pF
	Quiescent Current (Per Package) (Clock = 0 V, Other Inputs = V _{DD} or 0 V, I _{out} = 0 μA)	I _{DD}	5.0	—	5.0	—	0.005	5.0	—		150	μ _{AdC}
10			—	10	—	0.010	10	—	300			
15			—	20	—	0.015	20	—	600			
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C _L = 50 pF on all outputs, all buffers switching)	I _T	5.0	I _T = (0.8 μA/kHz) f + I _{DD}						μ _{AdC}			
		10	I _T = (1.6 μA/kHz) f + I _{DD}									
		15	I _T = (2.4 μA/kHz) f + I _{DD}									

#Noise immunity specified for worst-case input combination.

Noise Margin for both "1" and "0" level = 1.0 V min @ V_{DD} = 5.0 V
 2.0 V min @ V_{DD} = 10 V
 2.5 V min @ V_{DD} = 15 V

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + 3.5 \times 10^{-3} (C_L - 50) V_{DD} f$$

where: I_T is in μA (per package), C_L in pF, V_{DD} in V, and f in kHz is input frequency.

**The formulas given are for the typical characteristics only at 25°C.

MC14549B, MC14559B

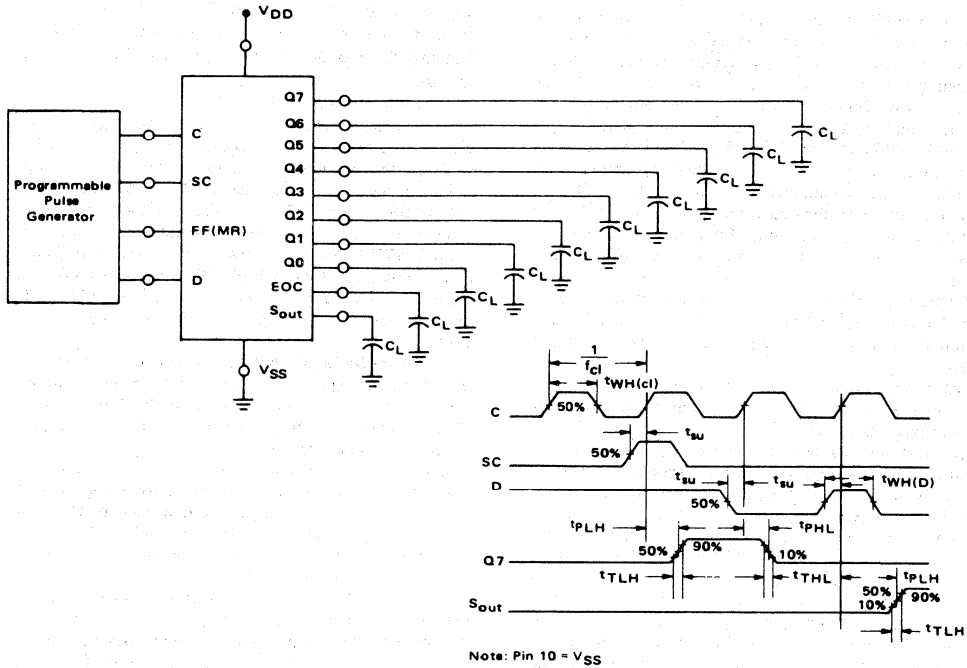
SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V _{DD}	Min	Typ	Max	Unit
Output Rise Time t _{TLH} = (3.0 ns/pF) C _L + 30 ns t _{TLH} = (1.5 ns/pF) C _L + 15 ns t _{TLH} = (1.1 ns/pF) C _L + 10 ns	t _{TLH}	5.0 10 15	— — —	180 90 65	360 180 130	ns
Output Fall Time t _{THL} = (1.5 ns/pF) C _L + 25 ns t _{THL} = (0.75 ns/pF) C _L + 12.5 ns t _{THL} = (0.55 ns/pF) C _L + 9.5 ns	t _{THL}	5.0 10 15	— — —	100 50 40	200 100 80	ns
Propagation Delay Time Clock to Q t _{PLH} , t _{PHL} = (1.7 ns/pF) C _L + 415 ns t _{PLH} , t _{PHL} = (0.66 ns/pF) C _L + 177 ns t _{PLH} , t _{PHL} = (0.5 ns/pF) C _L + 130 ns Clock to S _{out} t _{PLH} , t _{PHL} = (1.7 ns/pF) C _L + 665 ns t _{PLH} , t _{PHL} = (0.66 ns/pF) C _L + 277 ns t _{PLH} , t _{PHL} = (0.5 ns/pF) C _L + 195 ns Clock to EOC t _{PLH} , t _{PHL} = (1.7 ns/pF) C _L + 215 ns t _{PLH} , t _{PHL} = (0.66 ns/pF) C _L + 97 ns t _{PLH} , t _{PHL} = (0.5 ns/pF) C _L + 75 ns	t _{PLH} , t _{PHL}	5.0 10 15 5.0 10 15 5.0 10 15	— — — — — — — — —	500 210 155 750 310 220 300 130 100	1000 420 310 1500 620 440 600 260 200	ns
SC, D, FF or MR Setup Time	t _{su}	5.0 10 15	250 100 80	125 50 40	— — —	ns
Clock Pulse Width	t _{WH(c)}	5.0 10 15	700 270 200	350 135 100	— — —	ns
Pulse Width — D, SC, FF or MR	t _{WH}	5.0 10 15	500 200 160	250 100 80	— — —	ns
Clock Rise and Fall Time	t _{TLH} , t _{THL}	5.0 10 15	— — —	— — —	15 1.0 0.5	μs
Clock Pulse Frequency	f _{cl}	5.0 10 15	— — —	1.5 3.0 4.0	0.8 1.5 2.0	MHz

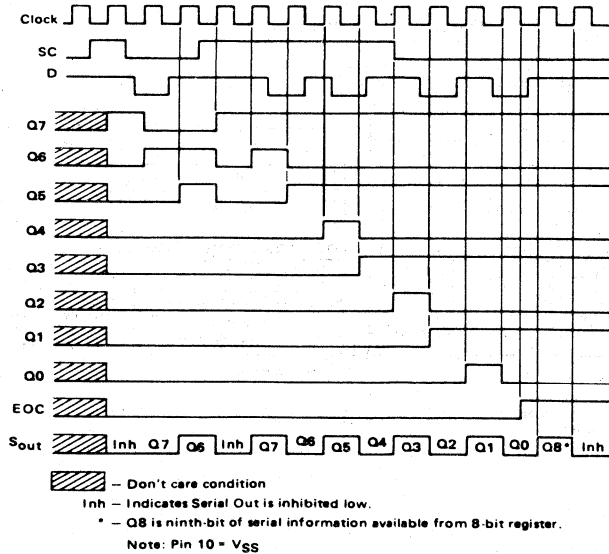
* The formulae given are for the typical characteristics only.

MC14549B, MC14559B

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



TIMING DIAGRAM



MC14549B, MC14559B

OPERATING CHARACTERISTICS

Both the MC14549B and MC14559B can be operated in either the "free run" or "strobed operation" mode for conversion schemes with any number of bits. Reliable cascading and/or recirculating operation can be achieved if the End of Convert (EOC) output is used as the controlling function, since with $EOC = 0$ (and with $SC = 1$ for MC14549B but either 1 or 0 for MC14559B) no stable state exists under continual clocked operation. The MC14559B will automatically recirculate after $EOC = 1$ during externally strobed operation, provided $SC = 1$.

All data and control inputs for these devices are triggered into the circuit on the positive edge of the clock pulse.

Operation of the various terminals is as follows:

C = Clock — A positive-going transition of the Clock is required for data on any input to be strobed into the circuit.

SC = Start Convert — A conversion sequence is initiated on the positive-going transition of the SC input on succeeding clock cycles.

D = Data In — Data on this input (usually from a comparator in A/D applications) is also entered into the circuit on a positive-going transition of the clock. This input is Schmitt triggered and synchronized to allow fast response and guaranteed quality of serial and parallel data.

MR = Master Reset (MC14549B only) — Resets all output to 0 on positive-going transitions of the clock. If removed while $SC = 0$, the circuit will remain reset until $SC = 1$. This allows easy cascading of circuits.

FF = Feed Forward (MC14559B only) — Provides register shortening by removing unwanted bits from a system.

For operation with less than 8 bits, tie the output following the least significant bit of the circuit to EOC.

E.g., for a 6-bit conversion, tie Q1 to FF; the part will respond as shown in the timing diagram less two bit times. Note that Q1 and Q0 will still operate and must be disregarded.

For 8-bit operation, FF is tied to VSS.

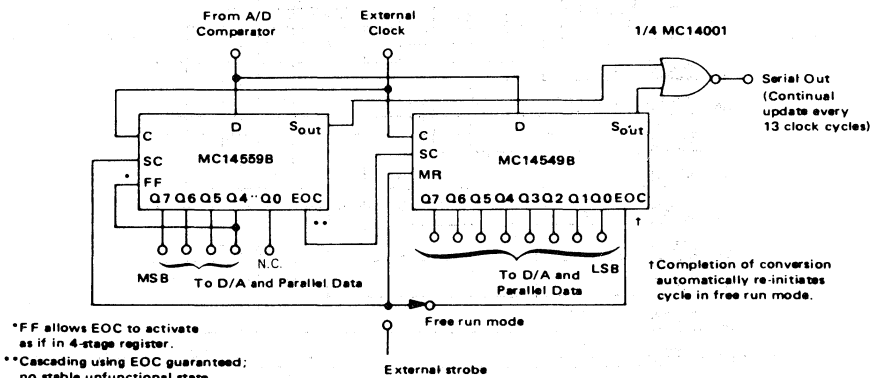
For applications with more than 8 but less than 16 bits, use the basic connections shown in Figure 1. The FF input of the MC14559B is used to shorten the setup. Tying FF directly to the least significant bit used in the MC14559B allows EOC to provide the cascading signal, and results in smooth transition of serial information from the MC14559B to the MC14549B. The Serial Out (S_{out}) inhibit structure of the MC14559B remains inactive one cycle after EOC goes high, while S_{out} of the MC14549B remains inhibited until the second clock cycle of its operation.

Q_n = Data Outputs — After a conversion is initiated the Q 's on succeeding cycles go high and are then conditionally reset dependent upon the state of the D input. Once conditionally reset they remain in the proper state until the circuit is either reset or reinitiated.

EOC = End of Convert — This output goes high on the negative-going transition of the clock following $FF = 1$ (for the MC14559B) or the conditional reset of Q0. This allows settling of the digital circuitry prior to the End of Conversion indication. Therefore either level or edge triggering can indicate complete conversion.

S_{out} = Serial Out — Transmits conversion in serial fashion. Serial data occurs during the clock period when the corresponding parallel data bit is conditionally reset. Serial Out is inhibited on the initial period of a cycle, when the circuit is reset, and on the second cycle after EOC goes high. This provides efficient operation when cascaded.

FIGURE 1 — 12-BIT CONVERSION SCHEME



MC14549B, MC14559B

TYPICAL APPLICATIONS

Externally Controlled 6-Bit ADC (Figure 2)

Several features are shown in this application:

- Shortening of the register to six bits by feeding the seventh output bit into the FF input.
- Continuous conversion, if a continuous signal is applied to SC.
- Externally controlled updating (the start pulse must be shorter than the conversion cycle).
- The EOC output indicating that the parallel data are valid and that the serial output is complete.

Continuously Cycling 8-Bit ADC (Figure 3)

This ADC is running continuously because the EOC signal is fed back to the SC input, immediately initiating a new cycle on the next clock pulse.

Continuously Cycling 12-Bit ADC (Figure 4)

Because each successive approximation register (SAR) has a capability of handling only an eight-bit word, two must be cascaded to make an ADC with more than eight bits.

When it is necessary to cascade two SAR's, the second SAR must have a stable resettable state to remain in while awaiting a subsequent start signal. However, the first stage must not have a stable resettable state while recycling, because during switch-on or due to outside influences, the first stage has entered a reset state, the entire ADC will remain in a stable non-functional condition.

This 12-bit ADC is continuously recycling. The serial as well as the parallel outputs are updated every thirteenth clock pulse. The EOC pulse indicates the completion of

FIGURE 2 – EXTERNALLY CONTROLLED 6-BIT ADC

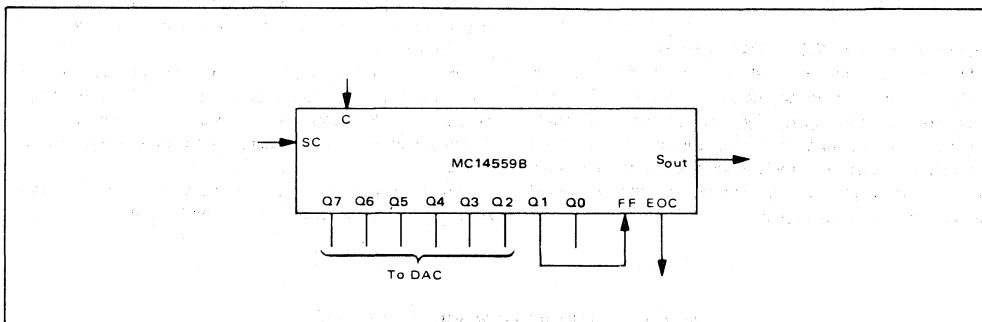
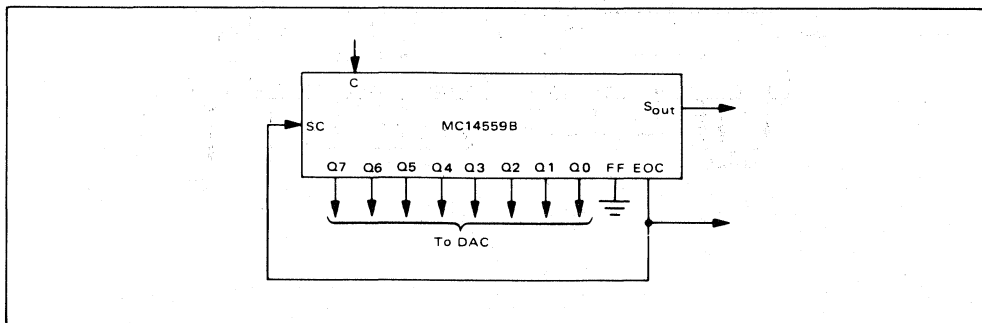
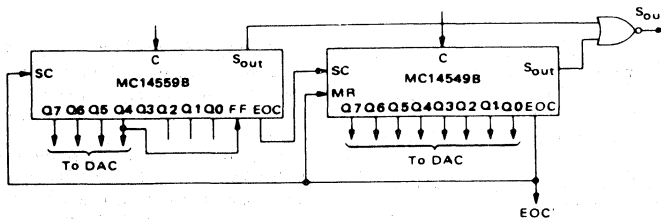


FIGURE 3 – CONTINUOUSLY CYCLING 8-BIT ADC



MC14549B, MC14559B

FIGURE 4 – CONTINUOUSLY CYCLING 12-BIT ADC



the 12-bit conversion cycle, the end of the serial output word, and the validity of the parallel data output.

Externally Controlled 12-Bit ADC (Figure 5)

In this circuit the external pulse starts the first SAR and simultaneously resets the cascaded second SAR. When Q4 of the first SAR goes high, the second SAR starts conversion, and the first one stops conversion. EOC indicates that the parallel data are valid and that the serial output is complete. Updating the output data is started with every external control pulse.

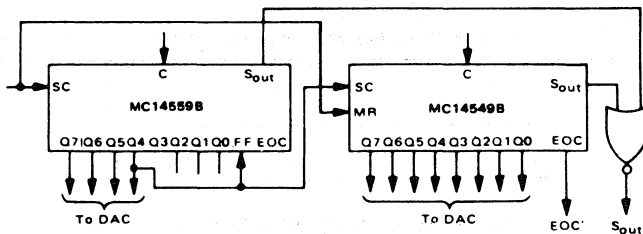
Additional Motorola Parts for Successive Approximation ADC

Monolithic digital-to-analog converters – The MC1408/1508 converter has eight-bit resolution and is available with 6, 7, and 8-bit accuracy. **The amplifier-comparator block** – The MC1407/1507 contains a high speed operational amplifier and a high speed comparator with adjustable window.

With these two linear parts it is possible to construct SA-ADCs with an accuracy of up to eight bits, using as the register one MC14549B or one MC14559B. An additional CMOS block will be necessary to generate the clock frequency.

Additional information on successive approximation ADC is found in Motorola Application Note AN-716.

FIGURE 5 – EXTERNALLY CONTROLLED 12-BIT ADC





MOTOROLA

MC14551B

**QUAD 2-CHANNEL
ANALOG MULTIPLEXER/DEMULTIPLEXER**

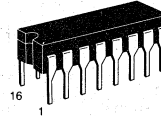
The MC14551B is a digitally-controlled analog switch. This device implements a 4PDT solid state switch with low ON impedance and very low OFF Leakage current. Control of analog signals up to the complete supply voltage range can be achieved.

- Triple Diode Protection on All Control Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Analog Voltage Range ($V_{DD} - V_{EE}$) = 3.0 to 18 V
Note: V_{EE} must be $\leq V_{SS}$
- Linearized Transfer Characteristics
- Low Noise — 12 nV/ $\sqrt{\text{Cycle}}$, $f \geq 1.0$ kHz typical
- For Low R_{ON} , Use The HC4051, HC4052, or HC4053 High-Speed CMOS Devices
- Switch Function is Break Before Make

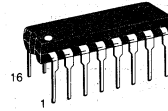
MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage (Referenced to V_{EE} , $V_{SS} \geq V_{EE}$)	- 0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient) (Referenced to V_{SS} for Control Input & V_{EE} for Switch I/O)	- 0.5 to $V_{DD} + 0.5$	V
I_{in}	Input Current (DC or Transient), per Control Pin	± 10	mA
I_{sw}	Switch Through Current	± 25	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	- 65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

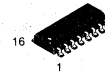
*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P and D/DW" Packages: - 7.0 mW/°C From 65°C To 125°C
Ceramic "L" Packages: - 12 mW/°C From 100°C To 125°C



**L SUFFIX
CERAMIC
CASE 620**



**P SUFFIX
PLASTIC
CASE 648**



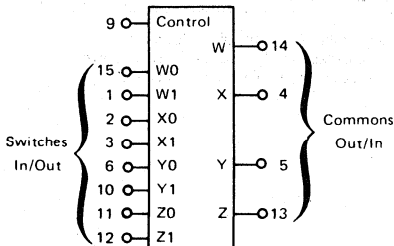
**D SUFFIX
SOIC
CASE 751B**

ORDERING INFORMATION

MC14XXXBCP Plastic
MC14XXXBCL Ceramic
MC14XXXBD SOIC

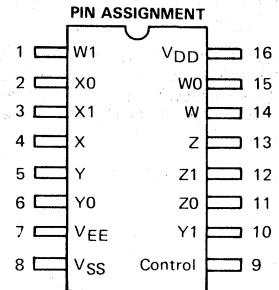
$T_A = -55^\circ$ to 125°C for all packages.

6



Control	ON
0	W0 X0 Y0 Z0
1	W1 X1 Y1 Z1

V_{DD} = Pin 16
 V_{SS} = Pin 8
 V_{EE} = Pin 7



Note: Control Input referenced to V_{SS} . Analog Inputs and Outputs reference to V_{EE} . V_{EE} must be $\leq V_{SS}$.

MC14551B

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V _{DD}	Test Conditions	-55°C		25°C			125°C		Unit
				Min	Max	Min	Typ #	Max	Min	Max	

SUPPLY REQUIREMENTS (Voltages Referenced to V_{EE})

Power Supply Voltage Range	V _{DD}	—	V _{DD} - 3.0 ≥ V _{SS} ≥ V _{EE}	3.0	18	3.0	—	18	3.0	18	V
Quiescent Current Per Package	I _{DD}	5.0	Control Inputs: V _{in} = V _{SS} or V _{DD} .	—	5.0	—	0.005	5.0	—	150	μA
		10	Switch I/O: V _{EE} ≤ V _{I/O} ≤ V _{DD} , and ΔV _{switch} ≤ 500 mV**	—	10	—	0.010	10	—	300	
		15		—	20	—	0.015	20	—	600	
Total Supply Current (Dynamic Plus Quiescent, Per Package)	I _{D(AV)}	5.0 10 15	T _A = 25°C only (The channel component, (V _{in} - V _{out})/R _{on} , is not included.)	Typical			(0.07 μA/kHz)f + I _{DD} (0.20 μA/kHz)f + I _{DD} (0.36 μA/kHz)f + I _{DD}			μA	

CONTROL INPUT (Voltages Referenced to V_{SS})

Low-Level Input Voltage	V _{IL}	5.0	R _{on} = per spec, I _{off} = per spec	—	1.5	—	2.25	1.5	—	1.5	V
		10		—	3.0	—	4.50	3.0	—	3.0	
		15		—	4.0	—	6.75	4.0	—	4.0	
High-Level Input Voltage	V _{IH}	5.0	R _{on} = per spec, I _{off} = per spec	3.5	—	3.5	2.75	—	3.5	—	V
		10		7.0	—	7.0	5.50	—	7.0	—	
		15		11	—	11	8.25	—	11	—	
Input Leakage Current	I _{in}	15	V _{in} = 0 or V _{DD}	—	±0.1	—	±0.00001	±0.1	—	±1.0	μA
Input Capacitance	C _{in}	—		—	—	—	5.0	7.5	—	—	pF

SWITCHES IN/OUT AND COMMONS OUT/IN — W, X, Y, Z (Voltages Referenced to V_{EE})

Recommended Peak-to-Peak Voltage Into or Out of the Switch	V _{I/O}	—	Channel On or Off	0	V _{DD}	0	—	V _{DD}	0	V _{DD}	V _{p-p}
Recommended Static or Dynamic Voltage Across the Switch** (Figure 3)	ΔV _{switch}	—	Channel On	0	600	0	—	600	0	300	mV
Output Offset Voltage	V _{OO}	—	V _{in} = 0 V, No Load	—	—	—	10	—	—	—	μV
ON Resistance	R _{on}	5.0	ΔV _{switch} ≤ 500 mV**, V _{in} = V _{IL} or V _{IH} (Control), and V _{in} = 0 to V _{DD} (Switch)	—	800	—	250	1050	—	1200	Ω
		10		—	400	—	120	500	—	520	
		15		—	220	—	80	280	—	300	
ΔON Resistance Between Any Two Channels in the Same Package	ΔR _{on}	5.0		—	70	—	25	70	—	135	Ω
		10		—	50	—	10	50	—	95	
		15		—	45	—	10	45	—	65	
Off-Channel Leakage Current (Figure 8)	I _{off}	15	V _{in} = V _{IL} or V _{IH} (Control) Channel to Channel or Any One Channel	—	±100	—	±0.05	±100	—	±1000	nA
Capacitance, Switch I/O	C _{I/O}	—	Switch Off	—	—	—	10	—	—	—	pF
Capacitance, Common O/I	C _{O/I}	—		—	—	—	17	—	—	—	pF
Capacitance, Feedthrough (Channel Off)	C _{I/O}	—	Pins Not Adjacent	—	—	—	0.15	—	—	—	pF
		—	Pins Adjacent	—	—	—	0.47	—	—	—	

#Data labeled "Typ" is not to be used for design purposes, but is intended as an indication of the IC's potential performance.

**For voltage drops across the switch (ΔV_{switch}) >600 mV (>300 mV at high temperature), excessive V_{DD} current may be drawn; i.e. the current out of the switch may contain both V_{DD} and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded. (See first page of this data sheet.)

MC14551B

ELECTRICAL CHARACTERISTICS ($C_L = 50$ pF, $T_A = 25^\circ\text{C}$, $V_{EE} \leq V_{SS}$)

Characteristic	Symbol	$V_{DD} - V_{EE}$ Vdc	Min	Typ #	Max	Unit
Propagation Delay Times Switch Input to Switch Output ($R_L = 10$ k Ω) t_{PLH} , $t_{PHL} = (0.17$ ns/pF) $C_L + 26.5$ ns t_{PLH} , $t_{PHL} = (0.08$ ns/pF) $C_L + 11$ ns t_{PLH} , $t_{PHL} = (0.06$ ns/pF) $C_L + 9.0$ ns	t_{PLH} , t_{PHL}	5.0 10 15	— — —	35 15 12	90 40 30	ns
Control Input to Output ($R_L = 10$ k Ω) $V_{EE} = V_{SS}$ (Figure 4)	t_{PLH} , t_{PHL}	5.0 10 15	— — —	350 140 100	875 350 250	ns
Second Harmonic Distortion $R_L = 10$ k Ω , $f = 1$ kHz, $V_{in} = 5$ V _{p-p}	—	10	—	0.07	—	%
Bandwidth (Figure 5) $R_L = 1$ k Ω , $V_{in} = 1/2 (V_{DD} - V_{EE})$ p-p, 20 Log $\frac{V_{out}}{V_{in}} = -3$ dB, $C_L = 50$ pF	BW	10	—	17	—	MHz
Off Channel Feedthrough Attenuation, Figure 5 $R_L = 1$ k Ω , $V_{in} = 1/2 (V_{DD} - V_{EE})$ p-p, $f_{in} = 55$ MHz	—	10	—	-50	—	dB
Channel Separation (Figure 6) $R_L = 1$ k Ω , $V_{in} = 1/2 (V_{DD} - V_{EE})$ p-p, $f_{in} = 3$ MHz	—	10	—	-50	—	dB
Crosstalk, Control Input to Common O/I, Figure 7 $R_1 = 1$ k Ω , $R_L = 10$ k Ω , Control $t_r = t_f = 20$ ns	—	10	—	75	—	mV

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$ for control inputs and $V_{EE} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$ for Switch I/O. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} , V_{EE} , or V_{DD}). Unused outputs must be left open.

MC14551B

FIGURE 1 – SWITCH CIRCUIT SCHEMATIC

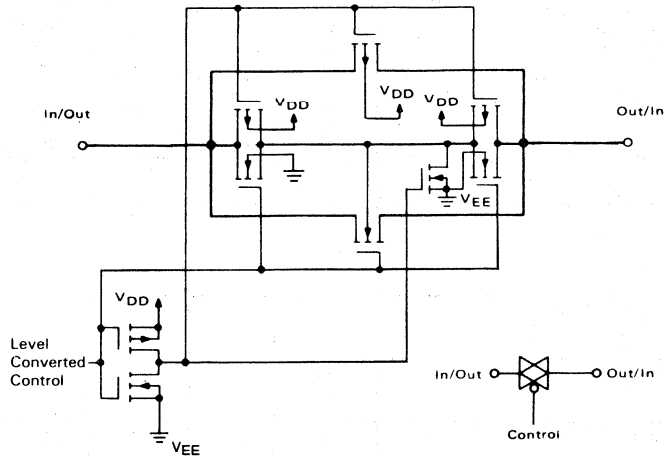
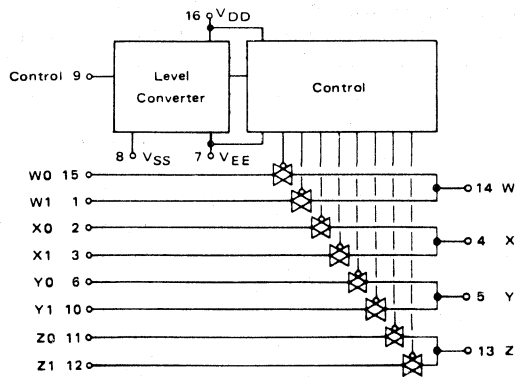


FIGURE 2 – MC14551B FUNCTIONAL DIAGRAM



MC14551B

TEST CIRCUITS

FIGURE 3 — ΔV ACROSS SWITCH

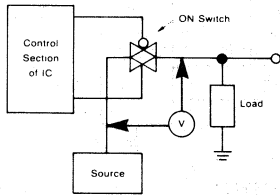


FIGURE 4 — PROPAGATION DELAY TIMES, CONTROL TO OUTPUT

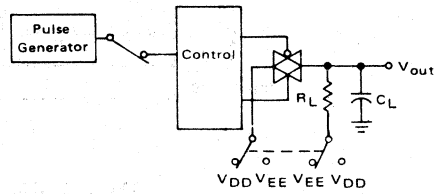


FIGURE 5 — BANDWIDTH AND OFF-CHANNEL FEEDTHROUGH ATTENUATION

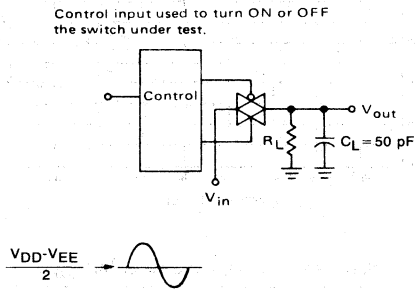


FIGURE 6 — CHANNEL SEPARATION (Adjacent Channels Used for Setup)

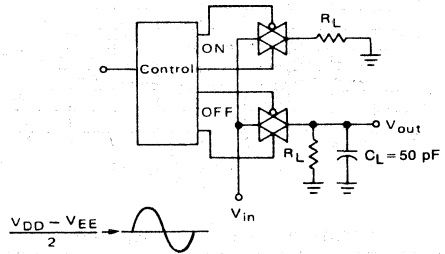


FIGURE 7 — CROSSTALK, CONTROL INPUT TO COMMON O/I

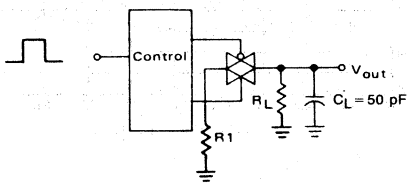
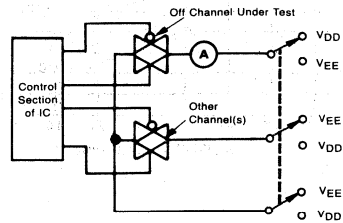
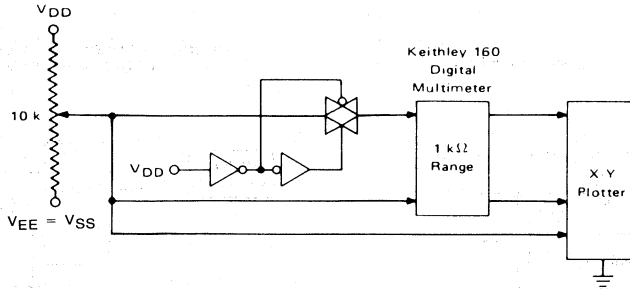


FIGURE 8 — OFF CHANNEL LEAKAGE



MC14551B

FIGURE 9 – CHANNEL RESISTANCE (R_{ON}) TEST CIRCUIT



TYPICAL RESISTANCE CHARACTERISTICS

FIGURE 10 – V_{DD} @ 7.5 V, V_{EE} @ -7.5 V

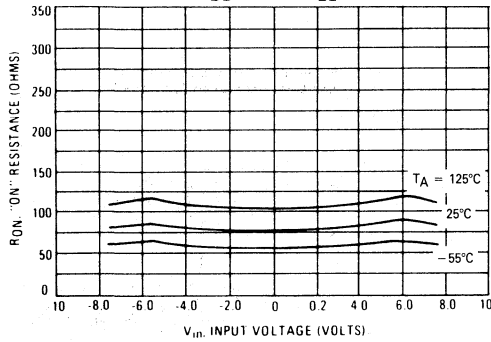


FIGURE 11 – V_{DD} @ 5.0 V, V_{EE} @ -5.0 V

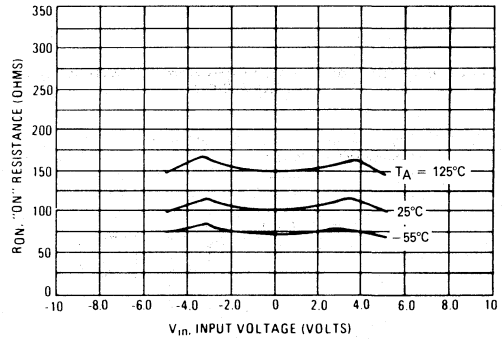


FIGURE 12 – V_{DD} @ 2.5 V, V_{EE} @ -2.5 V

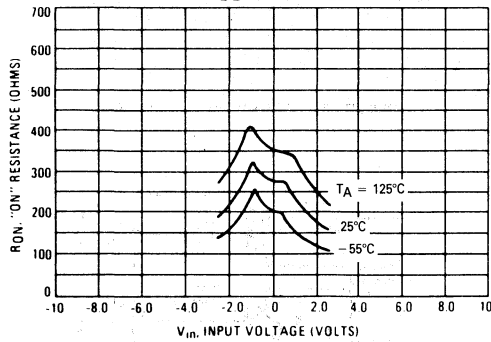
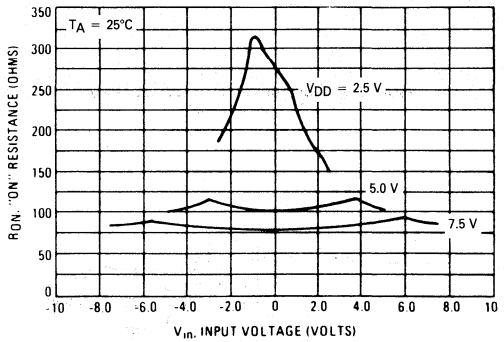


FIGURE 13 – COMPARISON at 25°C, V_{DD} @ $-V_{EE}$



MC14551B

APPLICATIONS INFORMATION

Figure A illustrates use of the on-chip level converter detailed in Figure 2. The 0-to-5 volt Digital Control signal is used to directly control a 9 V_{p-p} analog signal.

The digital control logic levels are determined by V_{DD} and V_{SS}. The V_{DD} voltage is the logic high voltage; the V_{SS} voltage is logic low. For the example, V_{DD} = +5 V = logic high at the control inputs; V_{SS} = GND = 0 V = logic low.

The maximum analog signal level is determined by V_{DD} and V_{VEE}. The V_{DD} voltage determines the maximum recommended peak above V_{SS}. The V_{VEE} voltage determines the maximum swing below V_{SS}. For the example, V_{DD} - V_{SS} = 5 volt maximum swing above V_{SS}; V_{SS} - V_{VEE} = 5 volt maximum swing

below V_{SS}. The example shows a ±4.5 volt signal which allows a 1/2 volt margin at each peak. If voltage transients above V_{DD} and/or below V_{VEE} are anticipated on the analog channels, external diodes (D_x) are recommended as shown in Figure B. These diodes should be small signal types able to absorb the maximum anticipated current surges during clipping.

The *absolute* maximum potential difference between V_{DD} and V_{VEE} is 18.0 volts. Most parameters are specified up to 15 volts which is the *recommended* maximum difference between V_{DD} and V_{VEE}.

Balanced supplies are not required. However, V_{SS} must be greater than or equal to V_{VEE}. For example, V_{DD} = +10 volts, V_{SS} = +5 volts, and V_{VEE} = -3 volts is acceptable. See the table below.

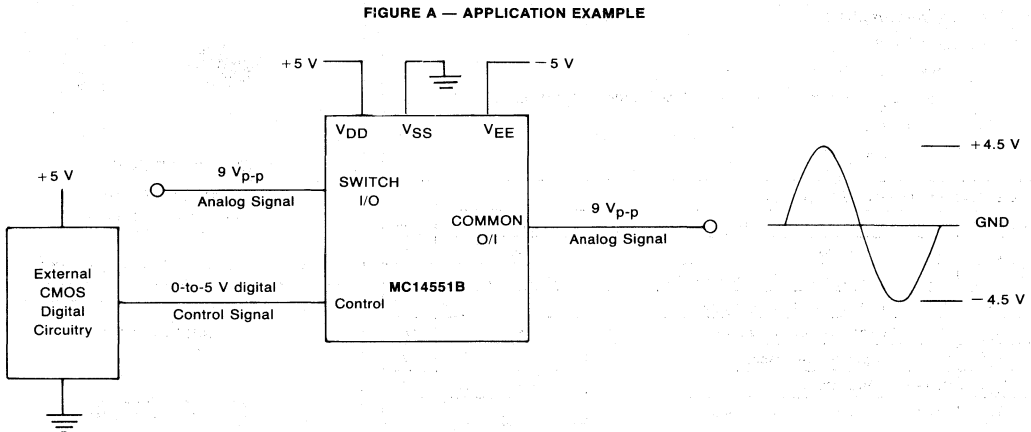
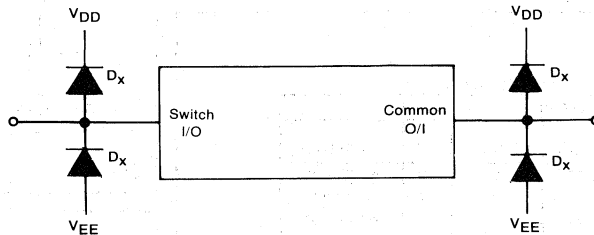


FIGURE B — EXTERNAL SCHOTTKY OR GERMANIUM CLIPPING DIODES



POSSIBLE SUPPLY CONNECTIONS

V _{DD} In Volts	V _{SS} In Volts	V _{VEE} In Volts	Control Inputs Logic High/Logic Low In Volts	Maximum Analog Signal Range In Volts
+8	0	-8	+8/0	+8 to -8 = 16 V _{p-p}
+5	0	-12	+5/0	+5 to -12 = 17 V _{p-p}
+5	0	0	+5/0	+5 to 0 = 5 V _{p-p}
+5	0	-5	+5/0	+5 to -5 = 10 V _{p-p}
+10		-5	+10/+5	+10 to -5 = 15 V _{p-p}



MOTOROLA

MC14553B

3-DIGIT BCD COUNTER

The MC14553B 3-digit BCD counter consists of 3 negative edge triggered BCD counters that are cascaded synchronously. A quad latch at the output of each counter permits storage of any given count. The information is then time division multiplexed, providing one BCD number or digit at a time. Digit select outputs provide display control. All outputs are TTL compatible.

An on-chip oscillator provides the low-frequency scanning clock which drives the multiplexer output selector.

This device is used in instrumentation counters, clock displays, digital panel meters, and as a building block for general logic applications.

- TTL Compatible Outputs
- On-Chip Oscillator
- Cascadable
- Clock Disable Input
- Pulse Shaping Permits Very Slow Rise Times on Input Clock
- Output Latches
- Master Reset

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

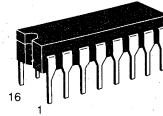
Symbol	Parameter	Value	Unit
V _{DD}	DC Supply Voltage	-0.5 to +18.0	V
V _{in} , V _{out}	Input or Output Voltage (DC or Transient)	-0.5 to V _{DD} + 0.5	V
I _{in}	Input Current (DC or Transient), per Pin	± 10	mA
I _{out}	Output Current (DC or Transient), per Pin	+ 20	mA
P _D	Power Dissipation, per Package†	500	mW
T _{stg}	Storage Temperature	-65 to +150	°C
T _L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
 †Temperature Derating: Plastic "P and D/DW" Packages: -7.0 mW/°C From 65°C To 125°C
 Ceramic "L" Packages: -12 mW/°C From 100°C To 125°C

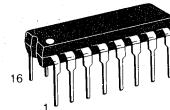
TRUTH TABLE

MASTER RESET	INPUTS			OUTPUTS
	CLOCK	DISABLE	LE	
0		0	0	No Change
0		0	0	Advance
0	X	1	X	No Change
0	1		0	Advance
0	1		0	No Change
0	0	X	X	No Change
0	X	X	X	Latched
0	X	X	1	Latched
1	X	X	0	Q0 = Q1 = Q2 = Q3 = 0

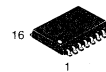
X = Don't Care



L SUFFIX
CERAMIC
CASE 620



P SUFFIX
PLASTIC
CASE 648



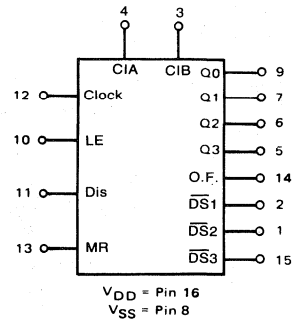
DW SUFFIX
SOIC
CASE 751G

ORDERING INFORMATION

MC14XXXBCP Plastic
 MC14XXXBCL Ceramic
 MC14XXXBDW SOIC

T_A = -55° to 125°C for all packages.

BLOCK DIAGRAM



This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range V_{SS} ≤ (V_{in} or V_{out}) ≤ V_{DD}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

MC14553B

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V _{DD} Vdc	-55°C		25°C			125°C		Unit	
			Min	Max	Min	Typ #	Max	Min	Max		
Output Voltage V _{in} = V _{DD} or 0 "0" Level	V _{OL}	5.0	—	0.05	—	0	0.05	—	0.05	Vdc	
		10	—	0.05	—	0	0.05	—	0.05		
15		—	0.05	—	0	0.05	—	0.05			
V _{in} = 0 or V _{DD} "1" Level	V _{OH}	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc	
		10	9.95	—	9.95	10	—	9.95	—		
		15	14.95	—	14.95	15	—	14.95	—		
Input Voltage (V _O = 4.5 or 0.5 Vdc) (V _O = 9.0 or 1.0 Vdc) (V _O = 13.5 or 1.5 Vdc) "0" Level	V _{IL}	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc	
		10	—	3.0	—	4.50	3.0	—	3.0		
		15	—	4.0	—	6.75	4.0	—	4.0		
	"1" Level (V _O = 0.5 or 4.5 Vdc) (V _O = 1.0 or 9.0 Vdc) (V _O = 1.5 or 13.5 Vdc)	V _{IH}	5.0	3.5	—	3.5	2.75	—	3.5	—	Vdc
			10	7.0	—	7.0	5.50	—	7.0	—	
			15	11	—	11	8.25	—	11	—	
Output Drive Current (V _{OH} = 4.6 Vdc) Source — Pin 3 (V _{OH} = 9.5 Vdc) (V _{OH} = 13.5 Vdc) (V _{OH} = 4.6 Vdc) Source — Other Outputs (V _{OH} = 9.5 Vdc) (V _{OH} = 13.5 Vdc) (V _{OL} = 0.4 Vdc) Sink — Pin 3 (V _{OL} = 0.5 Vdc) (V _{OL} = 1.5 Vdc) (V _{OL} = 0.4 Vdc) Sink — Other Outputs (V _{OL} = 0.5 Vdc) (V _{OL} = 1.5 Vdc)	I _{OH}	5.0	-0.25	—	-0.2	-0.36	—	0.14	—	mA _{dc}	
		10	-0.62	—	-0.5	-0.9	—	0.35	—		
		15	-1.8	—	-1.5	-3.5	—	—	—		
	I _{OL}	5.0	-0.64	—	-0.51	-0.88	—	-0.36	—	mA _{dc}	
		10	-1.6	—	-1.3	-2.25	—	-0.9	—		
		15	-4.2	—	-3.4	-8.8	—	-2.4	—		
I _{OL}	5.0	0.5	—	0.4	0.88	—	0.28	—	mA _{dc}		
	10	1.1	—	0.9	2.25	—	0.65	—			
	15	1.8	—	1.5	8.8	—	1.20	—			
I _{OL}	5.0	3.0	—	2.5	4.0	—	1.6	—	mA _{dc}		
	10	6.0	—	5.0	8.0	—	3.5	—			
	15	18	—	15	20	—	10	—			
Input Current	I _{in}	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	μA _{dc}	
Input Capacitance (V _{in} = 0)	C _{in}	—	—	—	—	5.0	7.5	—	—	pF	
Quiescent Current (Per Package) MR = V _{DD}	I _{DD}	5.0	—	5.0	—	0.010	5.0	—	150	μA _{dc}	
		10	—	10	—	0.020	10	—	300		
		15	—	20	—	0.030	20	—	600		
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C _L = 50 pF on all outputs, all buffers switching)	I _T	5.0	I _T = (0.35 μA/kHz) f + I _{DD}							μA _{dc}	
		10	I _T = (0.85 μA/kHz) f + I _{DD}								
		15	I _T = (1.50 μA/kHz) f + I _{DD}								

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) Vfk$$

where: I_T is in μA (per package), C_L in pF, V = (V_{DD} - V_{SS}) in volts, f in kHz is input frequency, and k = 0.004.

MC14553B

SWITCHING CHARACTERISTICS (C_L = 50 pF, T_A = 25°C)

Characteristic	Figure	Symbol	V _{DD}	Min	Typ #	Max	Unit
Output Rise and Fall Time t _{TLH} , t _{FHL} = (1.5 ns/pF) C _L + 25 ns t _{TLH} , t _{FHL} = (0.75 ns/pF) C _L + 12.5 ns t _{TLH} , t _{FHL} = (0.55 ns/pF) C _L + 9.5 ns	2a	t _{TLH} , t _{FHL}	5.0 10 15	— — —	100 50 40	200 100 80	ns
Clock to BCD Out	2a	t _{PLH} , t _{PHL}	5.0 10 15	— — —	900 500 200	1800 1000 400	ns
Clock to Overflow	2a	t _{PHL}	5.0 10 15	— — —	600 400 200	1200 800 400	ns
Reset to BCD Out	2b	t _{PHL}	5.0 10 15	— — —	900 500 300	1800 1000 600	ns
Clock to Latch Enable Setup Time Master Reset to Latch Enable Setup Time	2b	t _{su}	5.0 10 15	600 400 200	300 200 100	— — —	ns
Removal Time Latch Enable to Clock	2b	t _{rem}	5.0 10 15	-80 -10 0	-200 -70 -50	— — —	ns
Clock Pulse Width	2a	t _{WH(cl)}	5.0 10 15	550 200 150	275 100 75	— — —	ns
Reset Pulse Width	2b	t _{WH(R)}	5.0 10 15	1200 600 450	600 300 225	— — —	ns
Reset Removal Time	—	t _{rem}	5.0 10 15	-80 0 20	-180 -50 -30	— — —	ns
Input Clock Frequency	2a	f _{cl}	5.0 10 15	— — —	1.5 5.0 7.0	0.9 2.5 3.5	MHz
Input Clock Rise Time	2b	t _{TLH}	5.0 10 15	No Limit			ns
Disable, MR, Latch Enable Rise and Fall Times	—	t _{TLH} , t _{FHL}	5.0 10 15	— — —	— — —	15 5.0 4.0	μs
Scan Oscillator Frequency (C ₁ measured in μF)	1	f _{osc}	5.0 10 15	— — —	1.5/C ₁ 4.2/C ₁ 7.0/C ₁	— — —	Hz

*The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

MC14553B

FIGURE 1 — 3-DIGIT COUNTER TIMING DIAGRAM (Reference Figure 3)

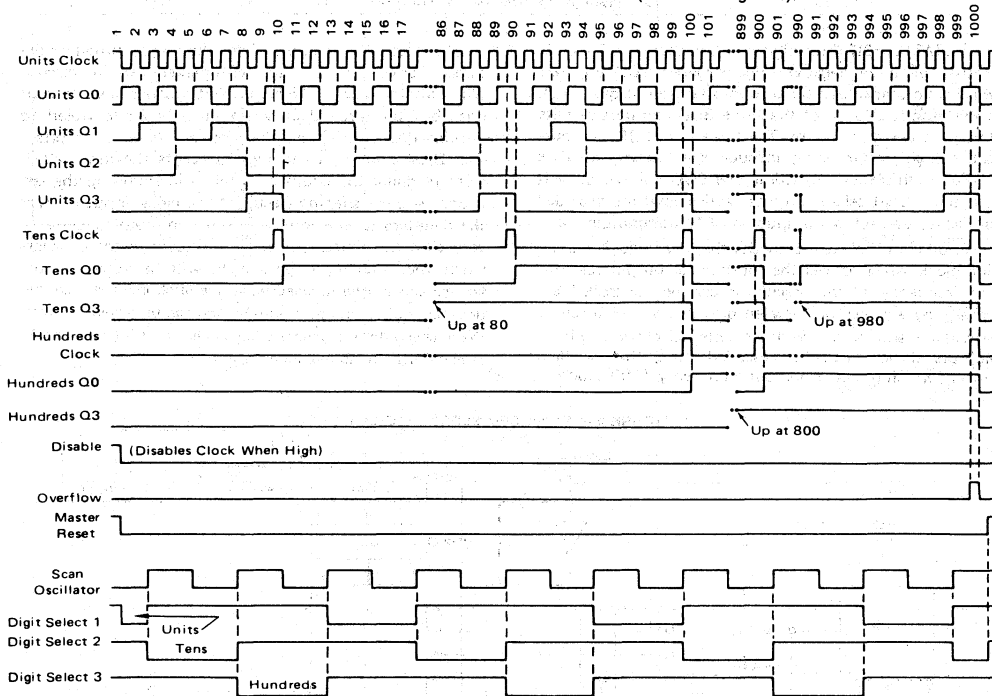
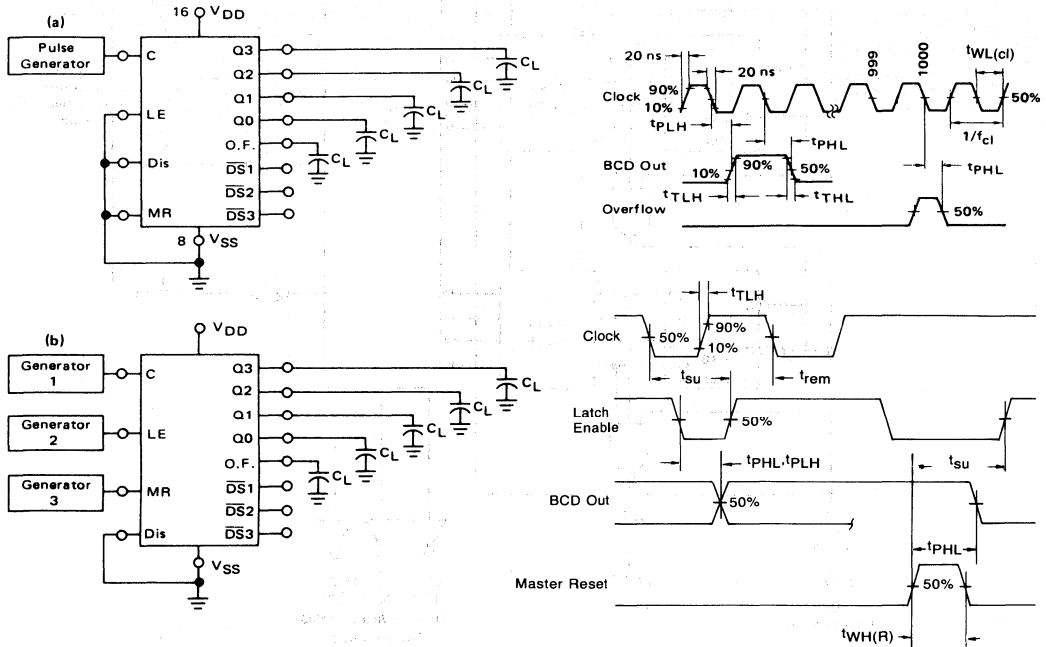


FIGURE 2 — SWITCHING TIME TEST CIRCUITS AND WAVEFORMS



MC14553B

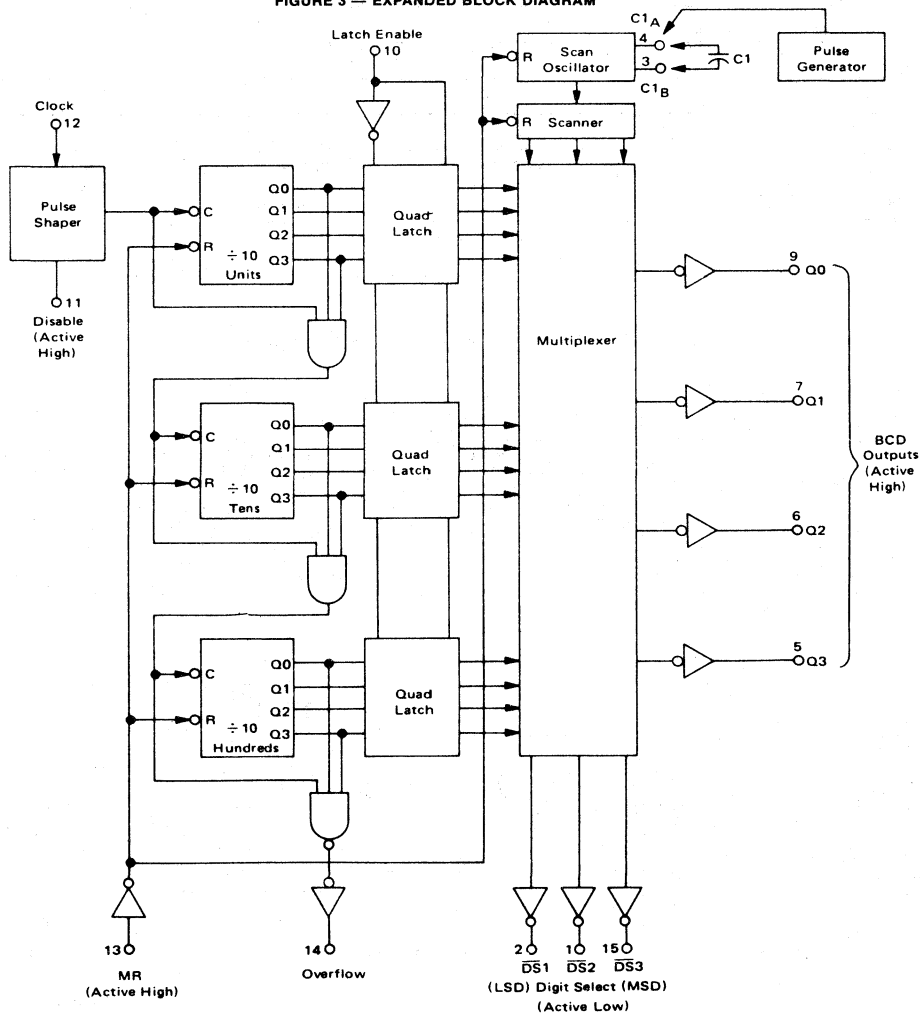
OPERATING CHARACTERISTICS

The MC14553B three-digit counter, shown in Figure 3, consists of three negative edge-triggered BCD counters which are cascaded in a synchronous fashion. A quad latch at the output of each of the three BCD counters permits storage of any given count. The three sets of BCD outputs (active high), after going through the latches, are time division multiplexed, providing one BCD number or digit at a time. Digit select outputs (active low) are provided for display control. All outputs are TTL compatible.

An on-chip oscillator provides the low frequency scanning clock which drives the multiplexer output selector. The frequency of the oscillator can be controlled externally by a capacitor between pins 3 and 4, or it can be overridden and driven with an external clock at pin 4. Multiple devices can be cascaded using the overflow output, which provides one pulse for every 1000 counts.

The Master Reset input, when taken high, initializes the three BCD counters and the multiplexer scanning circuit. While Master Reset is high the digit scanner is set to digit one; but all three digit select outputs are disabled to prolong display life, and the scan oscillator is inhibited. The Disable input, when high, prevents the input clock from reaching the counters, while still retaining the last count. A pulse shaping circuit at the clock input permits the counters to continue operating on input pulses with very slow rise times. Information present in the counters when the latch input goes high, will be stored in the latches and will be retained while the latch input is high, independent of other inputs. Information can be recovered from the latches after the counters have been reset if Latch Enable remains high during the entire reset cycle.

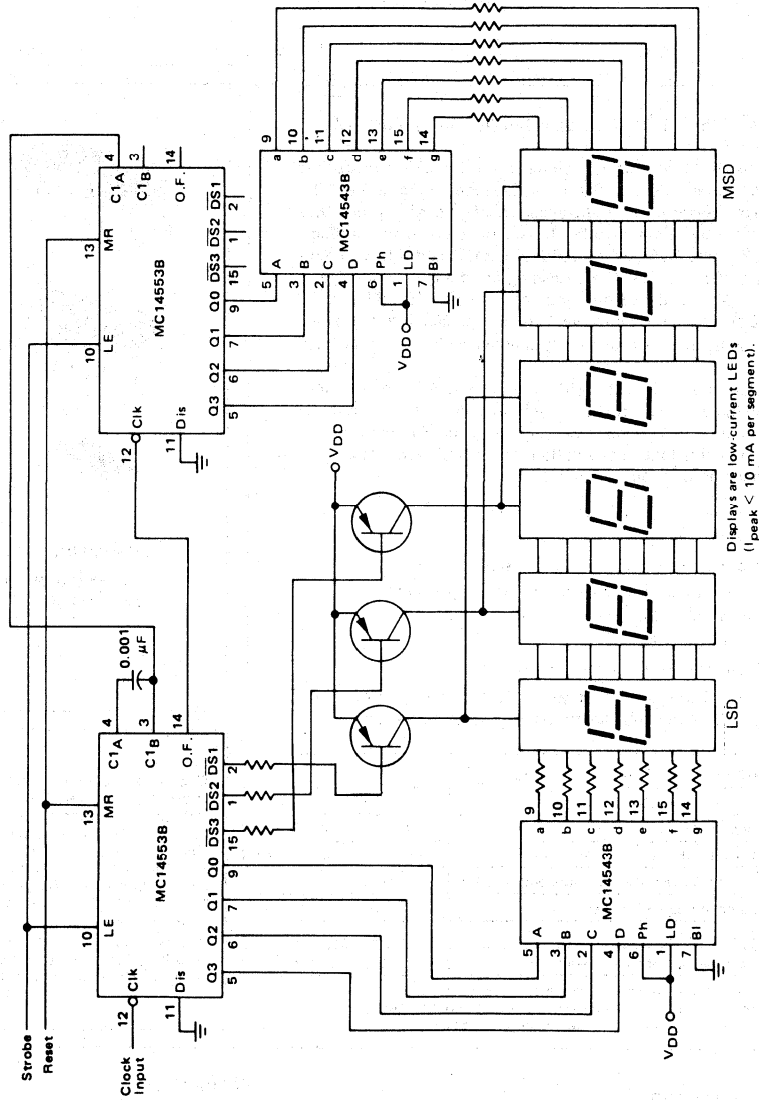
FIGURE 3 — EXPANDED BLOCK DIAGRAM



6

MC14553B

FIGURE 4 — SIX-DIGIT DISPLAY





MOTOROLA

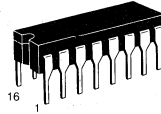
MC14554B

2-BIT BY 2-BIT PARALLEL BINARY MULTIPLIER

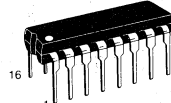
The MC14554B 2 x 2-bit parallel binary multiplier is constructed with complementary MOS (CMOS) enhancement mode devices. The multiplier can perform the multiplication of two binary numbers and simultaneously add two other binary numbers to the product. The MC14554B has two multiplicand inputs (X0 and X1), two multiplier inputs (Y0 and Y1), five cascading or adding inputs (K0, K1, M0, M1, and M2), and five sum and carry outputs (S0, S1, S2, C1 [S3], and C0). The basic multiplier can be expanded into a straight-forward m-bit by n-bit parallel multiplier without additional logic elements.

Application areas include arithmetic processing (multiplying/adding, obtaining square roots, polynomial evaluation, obtaining reciprocals, and dividing), Fast Fourier Transform processing, digital filtering, communications (convolution and correlation), and process and machine controls.

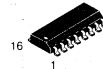
- Diode Protection on All Inputs
- All Outputs Buffered
- Straight-forward m-Bit By n-Bit Expansion
- No Additional Logic Elements Needed for Expansion
- Multiplies and Adds Simultaneously
- Positive Logic Design
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-Power TTL Loads or One Low-Power Schottky TTL Load Over the Rated Temperature Range



L SUFFIX
CERAMIC
CASE 620



P SUFFIX
PLASTIC
CASE 648



D SUFFIX
SOIC
CASE 751B

ORDERING INFORMATION

MC14XXXBCP Plastic
MC14XXXBCL Ceramic
MC14XXXBD SOIC

T_A = -55° to 125°C for all packages.

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V _{DD}	DC Supply Voltage	-0.5 to +18.0	V
V _{in} , V _{out}	Input or Output Voltage (DC or Transient)	-0.5 to V _{DD} + 0.5	V
I _{in} , I _{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
P _D	Power Dissipation, per Package†	500	mW
T _{stg}	Storage Temperature	-65 to +150	°C
T _L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.

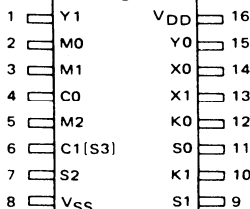
†Temperature Derating: Plastic "P and D/DW" Packages: -7.0 mW/°C From 65°C To 125°C
Ceramic "L" Packages: -12 mW/°C From 100°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range V_{SS} ≤ (V_{in} or V_{out}) ≤ V_{DD}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

6

PIN ASSIGNMENT



EQUATIONS

$$S = (X \times Y) + K + M$$

Where:

x Means Arithmetic Times.

+ Means Arithmetic Plus.

S = S3 S2 S1 S0, X = X1X0, Y = Y1Y0,

K = K1 K0, M = M1 M0 (Binary Numbers).

Example:

Given: X = 2(1), Y = 3(11)

K = 1(01), M = 2(10)

Then: S = (2 x 3) + 1 + 2 = 9

S = (10 x 11) + 01 + 10 = 1001

Note: C0 connected to M2 for this size multiplier.

See general expansion diagram for other size multipliers.

MC14554B

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V _{DD} Vdc	-55°C		25°C			125°C		Unit	
			Min	Max	Min	Typ #	Max	Min	Max		
Output Voltage V _{in} = V _{DD} or 0	"0" Level V _{OL}	5.0	—	0.05	—	0	0.05	—	0.05	Vdc	
		10	—	0.05	—	0	0.05	—	0.05		
		15	—	0.05	—	0	0.05	—	0.05		
	"1" Level V _{in} = 0 or V _{DD}	V _{OH}	5.0	4.95	—	4.95	5.0	—	4.95		—
			10	9.95	—	9.95	10	—	9.95		—
			15	14.95	—	14.95	15	—	14.95		—
Input Voltage (V _O = 4.5 or 0.5 Vdc) (V _O = 9.0 or 1.0 Vdc) (V _O = 13.5 or 1.5 Vdc)	"0" Level V _{IL}	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc	
		10	—	3.0	—	4.50	3.0	—	3.0		
		15	—	4.0	—	6.75	4.0	—	4.0		
	"1" Level (V _O = 0.5 or 4.5 Vdc) (V _O = 1.0 or 9.0 Vdc) (V _O = 1.5 or 13.5 Vdc)	V _{IH}	5.0	3.5	—	3.5	2.75	—	3.5		—
			10	7.0	—	7.0	5.50	—	7.0		—
			15	11	—	11	8.25	—	11		—
Output Drive Current (V _{OH} = 2.5 Vdc) (V _{OH} = 4.6 Vdc) (V _{OH} = 9.5 Vdc) (V _{OH} = 13.5 Vdc)	Source I _{OH}	5.0	-3.0	—	-2.4	-4.2	—	-1.7	—	mAdc	
		10	-0.64	—	-0.51	-0.88	—	-0.36	—		
		15	-4.2	—	-3.4	-8.8	—	-2.4	—		
	Sink I _{OL}	5.0	0.64	—	0.51	0.88	—	0.36	—		
		10	1.6	—	1.3	2.25	—	0.9	—		
		15	4.2	—	3.4	8.8	—	2.4	—		
Input Current	I _{in}	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	μAdc	
Input Capacitance (V _{in} = 0)	C _{in}	—	—	—	—	5.0	7.5	—	—	pF	
Quiescent Current (Per Package)	I _{DD}	5.0	—	5.0	—	0.005	5.0	—	150	μAdc	
		10	—	10	—	0.010	10	—	300		
		15	—	20	—	0.015	20	—	600		
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C _L = 50 pF on all outputs, all buffers switching)	I _T	5.0	I _T = (1.0 μA/kHz) f + I _{DD}						μAdc		
		10	I _T = (2.0 μA/kHz) f + I _{DD}								
		15	I _T = (3.0 μA/kHz) f + I _{DD}								

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) Vfk$$

where: I_T is in μA (per package), C_L in pF, V = (V_{DD} - V_{SS}) in volts, f in kHz is input frequency, and k = 0.0035.

MC14554B

SWITCHING CHARACTERISTICS* ($C_L = 50 \text{ pF}$, $T_A = 25^\circ\text{C}$)

Characteristic	Symbol	V _{DD}	Min	Typ #	Max	Unit
Output Rise and Fall Time	t_{TLH} , t_{THL}	5.0	—	100	200	ns
t_{TLH} , $t_{THL} = (1.5 \text{ ns/pF}) C_L + 25 \text{ ns}$		10	—	50	100	
t_{TLH} , $t_{THL} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$		15	—	40	80	
Propagation Delay Time	t_{PLH} , t_{PHL}	5.0	—	270	675	ns
K0 to C0		10	—	115	290	
t_{PLH} , $t_{PHL} = (1.7 \text{ ns/pF}) C_L + 185 \text{ ns}$		15	—	85	215	
t_{PLH} , $t_{PHL} = (0.66 \text{ ns/pF}) C_L + 82 \text{ ns}$		5.0	—	680	1700	
t_{PLH} , $t_{PHL} = (0.66 \text{ ns/pF}) C_L + 247 \text{ ns}$		10	—	280	750	
t_{PLH} , $t_{PHL} = (0.5 \text{ ns/pF}) C_L + 60 \text{ ns}$		15	—	210	570	
M0 to S2						

*The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

FIGURE 1 - DYNAMIC POWER DISSIPATION WAVEFORMS

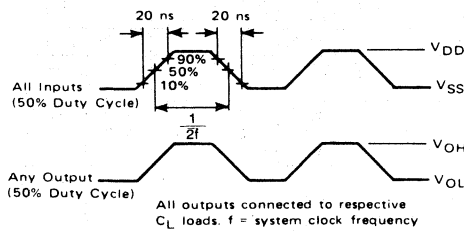
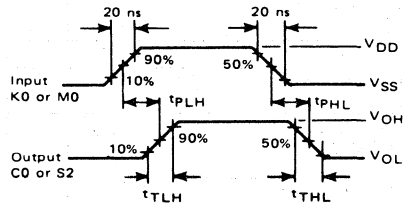


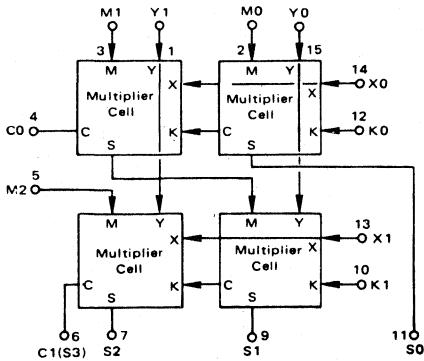
FIGURE 2 - DYNAMIC SIGNAL WAVEFORMS



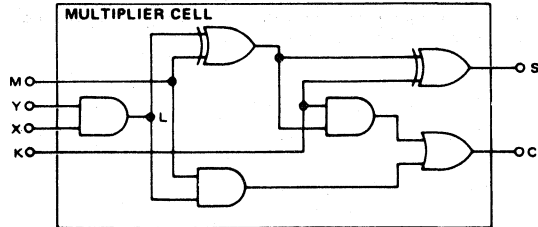
For K0 to C0:
Inputs X0, X1, Y0, Y1, K1, and M2 low, and inputs M0 and M1 high.

For M0 to S2:
Inputs X1, Y1, and K0 low, and inputs X0, Y0, K1, M1, and M2 high.

LOGIC DIAGRAM



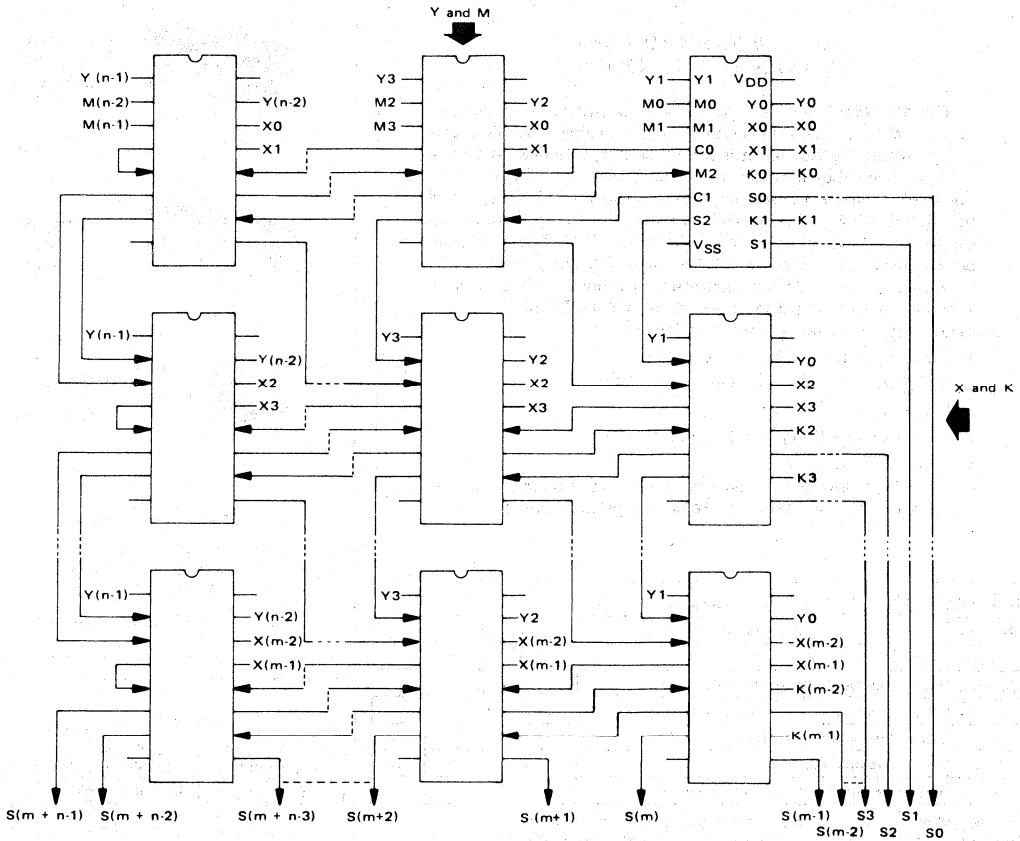
MULTIPLIER CELL



MC14554B

EXPANSION DIAGRAM

m-Bit by n-Bit Parallel Binary Multiplier (Top View)



$S = (X \times Y) + K + M$ Where: \times means Arithmetic Times.
 $+$ means Arithmetic Plus.

$S = S(m+n-1) S(m+n-2) \dots S2 S1 S0$

$X = X(m-1) X(m-2) \dots X2 X1 X0, Y = Y(n-1) Y(n-2) \dots Y2 Y1 Y0$

$K = K(m-1) K(m-2) \dots K2 K1 K0$ and $M = M(n-1) M(n-2) \dots M2 M1 M0$
 (Binary Numbers).

Number of output binary digits = $m + n$

Number of packages = $mn/4$ (For m or n or both odd select next highest even number.)



MOTOROLA

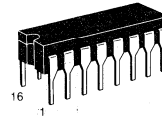
**MC14555B
MC14556B**

**DUAL BINARY TO 1-OF-4
DECODER/DEMULTIPLEXER**

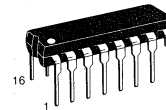
The MC14555B and MC14556B are constructed with complementary MOS (CMOS) enhancement mode devices. Each Decoder/Demultiplexer has two select inputs (A and B), an active low Enable input (E), and four mutually exclusive outputs (Q0, Q1, Q2, Q3). The MC14555B has the selected output go to the "high" state, and the MC14556B has the selected output go to the "low" state. Expanded decoding such as binary-to-hexadecimal (1-of-16), etc., can be achieved by using other MC14555B or MC14556B devices.

Applications include code conversion, address decoding, memory selection control, and demultiplexing (using the Enable input as a data input) in digital data transmission systems.

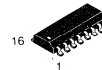
- Diode Protection on All Inputs
- Active High or Active Low Outputs
- Expandable
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- All Outputs Buffered
- Capable of Driving Two Low-Power TTL Loads or One Low-Power Schottky TTL Load Over the Rated Temperature Range



**L SUFFIX
CERAMIC
CASE 620**



**P SUFFIX
PLASTIC
CASE 648**



**D SUFFIX
SOIC
CASE 751B**

ORDERING INFORMATION

- MC14XXXBCP Plastic
- MC14XXXBCL Ceramic
- MC14XXXBD SOIC

T_A = -55° to 125°C for all packages.

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V _{DD}	DC Supply Voltage	-0.5 to +18.0	V
V _{in} , V _{out}	Input or Output Voltage (DC or Transient)	-0.5 to V _{DD} + 0.5	V
I _{in} , I _{out}	Input or Output Current (DC or Transient), per Pin	± 10	mA
P _D	Power Dissipation, per Package†	500	mW
T _{stg}	Storage Temperature	-65 to +150	°C
T _L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.

†Temperature Derating: Plastic "P and D/DW" Packages: -7.0 mW/°C From 65°C To 125°C
Ceramic "L" Packages: -12 mW/°C From 100°C To 125°C

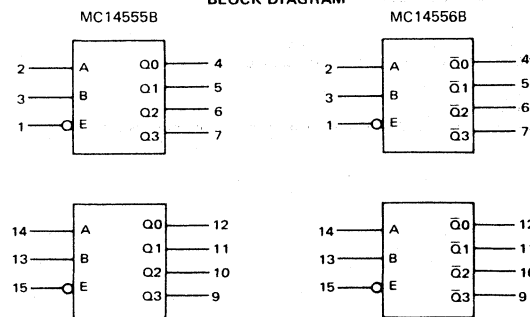
6

TRUTH TABLE

INPUTS			OUTPUTS MC14555B				OUTPUTS MC14556B			
ENABLE	SELECT		Q3	Q2	Q1	Q0	Q3	Q2	Q1	Q0
\bar{E}	B	A					$\bar{Q}3$	$\bar{Q}2$	$\bar{Q}1$	$\bar{Q}0$
0	0	0	0	0	0	1	1	1	1	0
0	0	1	0	0	1	0	1	1	0	1
0	1	0	0	1	0	0	1	0	1	1
0	1	1	1	0	0	0	0	1	1	1
1	X	X	0	0	0	0	1	1	1	1

X = Don't Care

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range V_{SS} ≤ (V_{in} or V_{out}) ≤ V_{DD}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

MC14555B•MC14556B

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V _{DD} Vdc	-55°C		25°C			125°C		Unit
			Min	Max	Min	Typ #	Max	Min	Max	
Output Voltage V _{in} = V _{DD} or 0	V _{OL}	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
		10	—	0.05	—	0	0.05	—	0.05	
V _{in} = 0 or V _{DD}	V _{OH}	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc
		10	9.95	—	9.95	10	—	9.95	—	
Input Voltage (V _O = 4.5 or 0.5 Vdc) (V _O = 9.0 or 1.0 Vdc) (V _O = 13.5 or 1.5 Vdc)	V _{IL}	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc
		10	—	3.0	—	4.50	3.0	—	3.0	
(V _O = 0.5 or 4.5 Vdc) (V _O = 1.0 or 9.0 Vdc) (V _O = 1.5 or 13.5 Vdc)	V _{IH}	5.0	3.5	—	3.5	2.75	—	3.5	—	Vdc
		10	7.0	—	7.0	5.50	—	7.0	—	
Output Drive Current (V _{OH} = 2.5 Vdc) (V _{OH} = 4.6 Vdc) (V _{OH} = 9.5 Vdc) (V _{OH} = 13.5 Vdc)	Source I _{OH}	5.0	-3.0	—	-2.4	-4.2	—	-1.7	—	mAdc
		5.0	-0.64	—	-0.51	-0.88	—	-0.36	—	
(V _{OL} = 0.4 Vdc) (V _{OL} = 0.5 Vdc) (V _{OL} = 1.5 Vdc)	Sink I _{OL}	5.0	0.64	—	0.51	0.88	—	0.36	—	mAdc
		10	1.6	—	1.3	2.25	—	0.9	—	
		15	4.2	—	3.4	8.8	—	2.4	—	
Input Current	I _{in}	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	μAdc
Input Capacitance (V _{in} = 0)	C _{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)	I _{DD}	5.0	—	5.0	—	0.005	5.0	—	150	μAdc
		10	—	10	—	0.010	10	—	300	
		15	—	20	—	0.015	20	—	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C _L = 50 pF on all outputs, all buffers switching)	I _T	5.0	I _T = (0.85 μA/kHz) f + I _{DD}						μAdc	
		10	I _T = (1.70 μA/kHz) f + I _{DD}							
		15	I _T = (2.60 μA/kHz) f + I _{DD}							

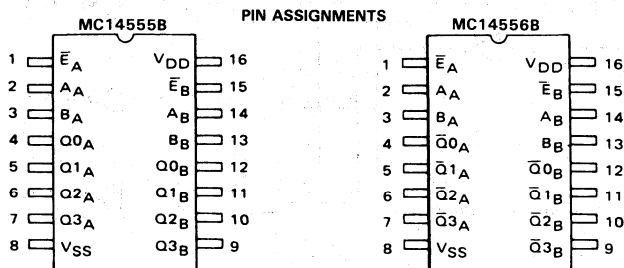
#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) \text{ Vfk}$$

where: I_T is in μA (per package), C_L in pF, V = (V_{DD} - V_{SS}) in volts, f in kHz is input frequency, and k = 0.002.



MC14555B•MC14556B

SWITCHING CHARACTERISTICS* ($C_L = 50 \text{ pF}$, $T_A = 25^\circ\text{C}$)

Characteristic	Symbol	V _{DD}	Min	Typ #	Max	Unit
Output Rise and Fall Time t_{TLH} , $t_{THL} = (1.5 \text{ ns/pF}) C_L + 25 \text{ ns}$ t_{TLH} , $t_{THL} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$ t_{TLH} , $t_{THL} = (0.55 \text{ ns/pF}) C_L + 9.5 \text{ ns}$	t_{TLH} , t_{THL}	5.0 10 15	— — —	100 50 40	200 100 80	ns
Propagation Delay Time — A, B to Output t_{PLH} , $t_{PHL} = (1.7 \text{ ns/pF}) C_L + 135 \text{ ns}$ t_{PLH} , $t_{PHL} = (0.66 \text{ ns/pF}) C_L + 62 \text{ ns}$ t_{PLH} , $t_{PHL} = (0.5 \text{ ns/pF}) C_L + 45 \text{ ns}$	t_{PLH} , t_{PHL}	5.0 10 15	— — —	220 95 70	440 190 140	ns
Propagation Delay Time — E to Output t_{PLH} , $t_{PHL} = (1.7 \text{ ns/pF}) C_L + 115 \text{ ns}$ t_{PLH} , $t_{PHL} = (0.66 \text{ ns/pF}) C_L + 52 \text{ ns}$ t_{PLH} , $t_{PHL} = (0.5 \text{ ns/pF}) C_L + 40 \text{ ns}$	t_{PLH} , t_{PHL}	5.0 10 15	— — —	200 85 65	400 170 130	ns

*The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

FIGURE 1 — DYNAMIC POWER DISSIPATION SIGNAL WAVEFORMS

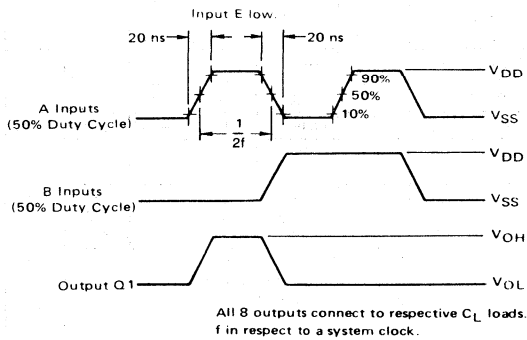
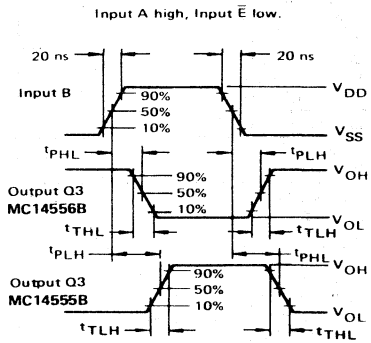
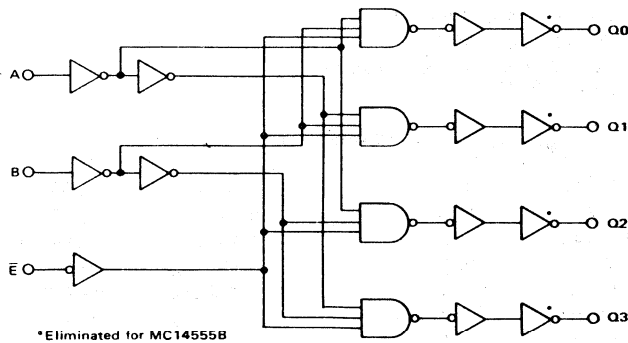


FIGURE 2 — DYNAMIC SIGNAL WAVEFORMS



LOGIC DIAGRAM
(1/2 of Dual)



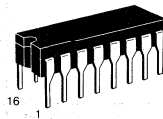
MC14557B

1-TO-64 BIT VARIABLE LENGTH SHIFT REGISTER

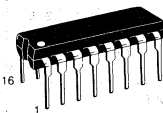
The MC14557B is a static clocked serial shift register whose length may be programmed to be any number of bits between 1 and 64. The number of bits selected is equal to the sum of the subscripts of the enabled Length Control inputs (L1, L2, L4, L8, L16, and L32) plus one. Serial data may be selected from the A or B data inputs with the A/B select input. This feature is useful for recirculation purposes. A Clock Enable (CE) input is provided to allow gating of the clock or negative edge clocking capability.

The device can be effectively used for variable digital delay lines or simply to implement odd length shift registers.

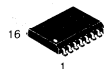
- 1-64 Bit Programmable Length
- Q and \bar{Q} Serial Buffered Outputs
- Asynchronous Master Reset
- All Inputs Buffered
- No Limit On Clock Rise and Fall Times
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or one Low-power Schottky TTL Load Over the Rated Temperature Range



L SUFFIX
CERAMIC
CASE 620



P SUFFIX
PLASTIC
CASE 648



DW SUFFIX
SOIC
CASE 751G

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	-0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	-0.5 to $V_{DD} + 0.5$	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	± 10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.

†Temperature Derating: Plastic "P and D/DW" Packages: -7.0 mW/°C From 65°C To 125°C
Ceramic "L" Packages: -12 mW/°C From 100°C To 125°C

ORDERING INFORMATION

MC14XXXBCP Plastic
MC14XXXBCL Ceramic
MC14XXXBDW SOIC

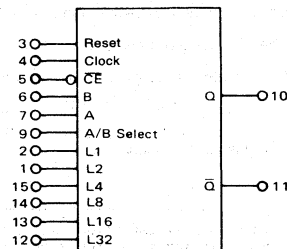
$T_A = -55^\circ$ to 125°C for all packages.

LENGTH SELECT TRUTH TABLE

L32	L16	L8	L4	L2	L1	Register Length
0	0	0	0	0	0	1-Bit
0	0	0	0	0	1	2-Bits
0	0	0	0	1	0	3-Bits
0	0	0	0	1	1	4-Bits
0	0	0	1	0	0	5-Bits
0	0	0	1	0	1	6-Bits
.
.
.
.
.
.
.
.
.
.
1	0	0	0	0	0	33-Bits
1	0	0	0	0	1	34-Bits
.
.
.
.
.
.
.
.
.
.
.
.
1	1	1	1	0	0	61-Bits
1	1	1	1	0	1	62-Bits
1	1	1	1	1	0	63-Bits
1	1	1	1	1	1	64-Bits

Note: Length equals the sum of the binary length control subscripts plus one.

BLOCK DIAGRAM



$V_{DD} = \text{Pin } 16$
 $V_{SS} = \text{Pin } 8$

TRUTH TABLE

Inputs				Output	
Rst	A/B	Clock	CE	Q	\bar{Q}
0	0		0	B	A
0	1		0	A	B
0	0	1		B	A
0	1	1		A	B
1	X	X	X	0	0

Q is the output of the first selected shift register stage.

X = Don't Care.

MC14557B

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V _{DD} Vdc	-55°C		25°C			125°C		Unit	
			Min	Max	Min	Typ #	Max	Min	Max		
Output Voltage "0" Level V _{in} = V _{DD} or 0	V _{OL}	5.0	—	0.05	—	0	0.05	—	0.05	Vdc	
		10	—	0.05	—	0	0.05	—	0.05		
15		—	0.05	—	0	0.05	—	0.05			
"1" Level V _{in} = 0 or V _{DD}	V _{OH}	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc	
		10	9.95	—	9.95	10	—	9.95	—		
		15	14.95	—	14.95	15	—	14.95	—		
Input Voltage (V _O = 4.5 or 0.5 Vdc) (V _O = 9.0 or 1.0 Vdc) (V _O = 13.5 or 1.5 Vdc)	V _{IL}	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc	
		10	—	3.0	—	4.50	3.0	—	3.0		
15		—	4.0	—	6.75	4.0	—	4.0			
"1" Level (V _O = 0.5 or 4.5 Vdc) (V _O = 1.0 or 9.0 Vdc) (V _O = 1.5 or 13.5 Vdc)	V _{IH}	5.0	3.5	—	3.5	2.75	—	3.5	—	Vdc	
		10	7.0	—	7.0	5.50	—	7.0	—		
		15	11	—	11	8.25	—	11	—		
Output Drive Current (V _{OH} = 2.5 Vdc) (V _{OH} = 4.6 Vdc) (V _{OH} = 9.5 Vdc) (V _{OH} = 13.5 Vdc)	Source	I _{OH}	5.0	-3.0	—	-2.4	-4.2	—	-1.7	—	mA _{dc}
			10	-0.64	—	-0.51	-0.88	—	-0.36	—	
(V _{OL} = 0.4 Vdc) (V _{OL} = 0.5 Vdc) (V _{OL} = 1.5 Vdc)	Sink	I _{OL}	5.0	0.64	—	0.51	0.88	—	0.36	—	mA _{dc}
			10	1.6	—	1.3	2.25	—	0.9	—	
15	4.2	—	3.4	8.8	—	2.4	—	—			
Input Current	I _{in}	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	μA _{dc}	
Input Capacitance (V _{in} = 0)	C _{in}	—	—	—	—	5.0	7.5	—	—	pF	
Quiescent Current (Per Package)	I _{DD}	5.0	—	5.0	—	0.010	5.0	—	150	μA _{dc}	
		10	—	10	—	0.020	10	—	300		
		15	—	20	—	0.030	20	—	600		
Total Supply Current**†† (Dynamic plus Quiescent, Per Package) (C _L = 50 pF on all outputs, all buffers switching)	I _T	5.0	I _T = (1.75 μA/kHz) f + I _{DD} I _T = (3.50 μA/kHz) f + I _{DD} I _T = (5.25 μA/kHz) f + I _{DD}							μA _{dc}	

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) Vfk$$

where: I_T is in μA (per package), C_L in pF, V = (V_{DD} - V_{SS}) in volts, f in kHz is input frequency, and k = 0.001.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range V_{SS} ≤ (V_{in} or V_{out}) ≤ V_{DD}. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

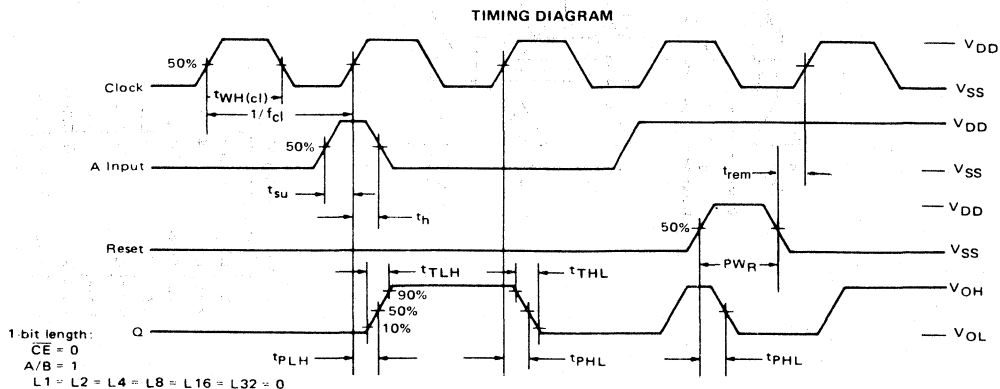
MC14557B

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V _{DD}	Min	Typ #	Max	Unit
Rise and Fall Time, Q or \bar{Q} Output $t_{TLH}, t_{THL} = (1.5 \text{ ns/pF}) C_L + 25 \text{ ns}$ $t_{TLH}, t_{THL} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$ $t_{TLH}, t_{THL} = (0.55 \text{ ns/pF}) C_L + 9.5 \text{ ns}$	t_{TLH}, t_{THL}	5 10 15	— — —	100 50 40	200 100 80	ns
Propagation Delay, Clock or \bar{CE} to Q or \bar{Q} $t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 215 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 97 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.55 \text{ ns/pF}) C_L + 65 \text{ ns}$	t_{PLH}, t_{PHL}	5 10 15	— — —	300 130 90	600 260 180	ns
Propagation Delay, Reset to Q or \bar{Q} $t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 215 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 97 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 70 \text{ ns}$	t_{PLH}, t_{PHL}	5 10 15	— — —	300 130 95	600 260 190	ns
Pulse Width, Clock	$t_{WH}(cl)$	5 10 15	200 100 75	95 45 35	— — —	ns
Pulse Width, Reset	$t_{WH}(rst)$	5 10 15	300 140 100	150 70 50	— — —	ns
Clock Frequency (50% Duty Cycle)	f_{cl}	5 10 15	— — —	3.0 7.5 13.0	1.7 5.0 6.7	MHz
Setup Time, A or B to Clock or \bar{CE} Worst case condition: L1 = L2 = L4 = L8 = L16 = L32 = V _{SS} (Register Length = 1) Best case condition: L32 = V _{DD} , L1 through L16 = Don't Care (Any register length from 33 to 64)	t_{su}	5 10 15	700 290 145	350 130 85	— — —	ns
Hold Time, Clock or \bar{CE} to A or B Best case condition: L1 = L2 = L4 = L8 = L16 = L32 = V _{SS} (Register Length = 1) Worst case condition: L32 = V _{DD} , L1 through L16 = Don't Care (Any register length from 33 to 64)	t_h	5 10 15	200 100 10	-150 -60 -50	— — —	ns
Rise and Fall Time, Clock	t_r, t_f	5 10 15	No Limit			—
Rise and Fall Time, Reset or \bar{CE}	t_r, t_f	5 10 15	— — —	— — —	15 5 4	μs
Removal Time, Reset to Clock or \bar{CE}	t_{rem}	5 10 15	160 80 70	80 40 35	— — —	ns

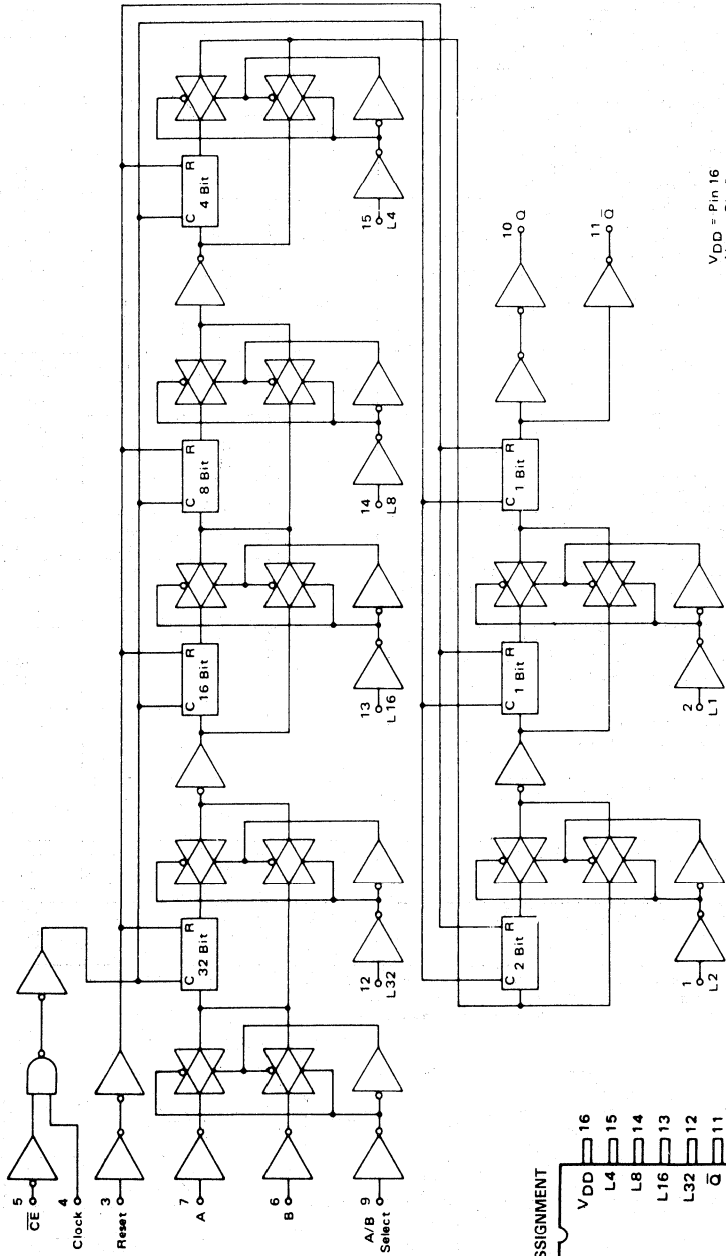
*The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

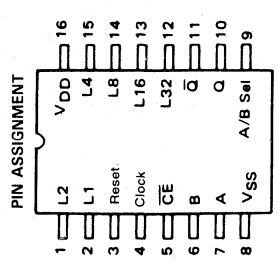


MC14557B

LOGIC DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8





MOTOROLA

MC14558B

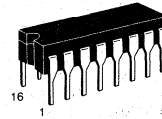
BCD-TO-SEVEN SEGMENT DECODER

The MC14558B decodes 4-bit binary coded decimal data dependent on the state of auxiliary inputs, Enable and \overline{RBI} , and provides an active-high seven-segment output for a display driver.

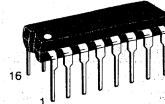
An auxiliary input truth table is shown, in addition to the BCD to seven-segment truth table, to indicate the functions available with the two auxiliary inputs.

Leading Zero blanking is easily obtained with an external flip-flop in time division multiplexed systems displaying most significant decade first.

- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Segment Blanking for All Illegal Input Combinations
- Lamp Test Function
- Capability for Suppression of Non-Significant Zeros
- Lamp Intensity Function
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range



L SUFFIX
CERAMIC
CASE 620



P SUFFIX
PLASTIC
CASE 648



D SUFFIX
SOIC
CASE 751B

ORDERING INFORMATION

MC14XXXBCP Plastic
MC14XXXBCL Ceramic
MC14XXXBD SOIC

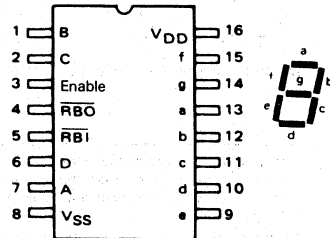
$T_A = -55^\circ$ to 125°C for all packages.

MAXIMUM RATINGS (Voltages referenced to V_{SS})

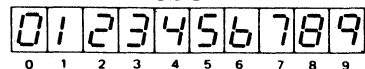
Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	V
Input Voltage, All Inputs	V_{in}	-0.5 to $V_{DD} + 0.5$	V
DC Input Current, per Pin	I_{in}	± 10	mAdc
Operating Temperature Range	T_A	-55 to +125	$^\circ\text{C}$
Power Dissipation, per Package†	P_D	500	mW
Storage Temperature Range	T_{stg}	-65 to +150	$^\circ\text{C}$

*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P and D/DW" Packages: -7.0 mW/ $^\circ\text{C}$ From 65°C To 125°C
Ceramic "L" Packages: -12 mW/ $^\circ\text{C}$ From 100°C To 125°C

PIN ASSIGNMENT



DISPLAY



AUXILIARY INPUT TRUTH TABLE

Enable Pin 3	\overline{RBI} Pin 5	BCD Input Code	\overline{RBO} Pin 4	Function Performed
0	0	X	0	Lamp Test
0	1	X	1	Blank Segments
1	1	0	1	Display Zero
1	0	0	0	Blank Segments
1	X	1-9	1	1-9 Displayed

X = Don't Care
 \overline{RBI} = Ripple Blanking Input
 \overline{RBO} = Ripple Blanking Output

6

MC14558B

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	-55°C		25°C			125°C		Unit
			Min	Max	Min	Typ #	Max	Min	Max	
Output Voltage $V_{in} = V_{DD}$ or 0 $V_{in} = 0$ or V_{DD}	VOL	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
		10	—	0.05	—	0	0.05	—	0.05	
		15	—	0.05	—	0	0.05	—	0.05	
	VOH	5.0	4.95	—	4.95	5.0	—	4.95	—	
		10	9.95	—	9.95	10	—	9.95	—	
		15	14.95	—	14.95	15	—	14.95	—	
Input Voltage # ($V_O = 4.5$ or 0.5 Vdc) ($V_O = 9.0$ or 1.0 Vdc) ($V_O = 13.5$ or 1.5 Vdc) ($V_O = 0.5$ or 4.5 Vdc) ($V_O = 1.0$ or 9.0 Vdc) ($V_O = 1.5$ or 13.5 Vdc)	VIL	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc
		10	—	3.0	—	4.50	3.0	—	3.0	
		15	—	4.0	—	6.75	4.0	—	4.0	
	VIH	5.0	3.5	—	3.5	2.75	—	3.5	—	
		10	7.0	—	7.0	5.50	—	7.0	—	
		15	11	—	11	8.25	—	11	—	
Output Drive Current ($V_{OH} = 2.5$ Vdc) ($V_{OH} = 4.6$ Vdc) ($V_{OH} = 9.5$ Vdc) ($V_{OH} = 13.5$ Vdc) ($V_{OL} = 0.4$ Vdc) ($V_{OL} = 0.5$ Vdc) ($V_{OL} = 1.5$ Vdc)	Source IOH	5.0	-3.0	—	-2.4	-4.2	—	-1.7	—	mAdc
		5.0	-0.64	—	-0.51	-0.88	—	-0.36	—	
		10	-1.6	—	-1.3	-2.25	—	-0.9	—	
	Sink IOL	5.0	0.64	—	0.51	0.88	—	0.36	—	
		10	1.6	—	1.3	2.25	—	0.9	—	
		15	4.2	—	3.4	8.8	—	2.4	—	
Input Current	I_{in}	15	—	± 0.1	—	± 0.00001	± 0.1	—	± 1.0	μ Adc
Input Capacitance	C_{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package) $V_{in} = 0$ or V_{DD} $I_{out} = 0 \mu A$	IDD	5.0	—	5.0	—	0.005	5.0	—	150	μ Adc
		10	—	10	—	0.010	10	—	300	
		15	—	20	—	0.015	20	—	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) ($C_L = 50$ pF on all outputs, all buffers switching)	IT	5.0	$I_T = (1.2 \mu A/kHz) f + I_{DD}$ $I_T = (2.4 \mu A/kHz) f + I_{DD}$ $I_T = (3.6 \mu A/kHz) f + I_{DD}$							μ Adc
		10								
		15								

#Noise immunity specified for worst-case input combination.

Noise Margin for both "1" and "0" level = 1.0 V min @ $V_{DD} = 5.0$ V
 2.0 V min @ $V_{DD} = 10$ V
 2.5 V min @ $V_{DD} = 15$ V

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + 3.5 \times 10^{-3} (C_L - 50) V_{DD} f$$

where: I_T is in μA (per package), C_L in pF, V_{DD} in V, and f in kHz is input frequency.

**The formulas given are for the typical characteristics only at 25°C.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$.
 Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

MC14558B

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C; see Figure 1)

Characteristic	Symbol	V _{DD}	Min	Typ	Max	Unit
Output Rise Time $t_{TLH} = (3.0 \text{ ns/pF}) C_L + 30 \text{ ns}$ $t_{TLH} = (1.5 \text{ ns/pF}) C_L + 15 \text{ ns}$ $t_{TLH} = (1.1 \text{ ns/pF}) C_L + 10 \text{ ns}$	t_{TLH}	5.0 10 15	— — —	100 50 40	200 100 80	ns
Output Fall Time $t_{THL} = (1.5 \text{ ns/pF}) C_L + 25 \text{ ns}$ $t_{THL} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$ $t_{THL} = (0.55 \text{ ns/pF}) C_L + 9.5 \text{ ns}$	t_{THL}	5.0 10 15	— — —	100 50 40	200 100 80	ns
Propagation Delay Time $t_{PLH} = (1.7 \text{ ns/pF}) C_L + 495 \text{ ns}$ $t_{PLH} = (0.66 \text{ ns/pF}) C_L + 187 \text{ ns}$ $t_{PLH} = (0.5 \text{ ns/pF}) C_L + 120 \text{ ns}$	t_{PLH}	5.0 10 15	— — —	580 220 145	1160 440 230	ns
Propagation Delay Time $t_{PHL} = (1.7 \text{ ns/pF}) C_L + 695 \text{ ns}$ $t_{PHL} = (0.66 \text{ ns/pF}) C_L + 242 \text{ ns}$ $t_{PHL} = (0.5 \text{ ns/pF}) C_L + 160 \text{ ns}$	t_{PHL}	5.0 10 15	— — —	780 275 185	1560 550 370	ns

* The formulae given are for the typical characteristics only.

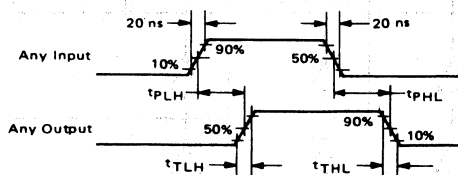
TRUTH TABLE

INPUTS						OUTPUTS*									
Enable Pin 3	RBI Pin 5	D Pin 6	C Pin 2	B Pin 1	A Pin 7	a Pin 13	b Pin 12	c Pin 11	d Pin 10	e Pin 9	f Pin 15	g Pin 14	RBO Pin 4	DISPLAY	
1	1	0	0	0	0	1	1	1	1	1	1	0	1	0	
1	x	0	0	0	1	0	0	0	0	1	1	0	1	1	
1	x	0	0	1	0	1	1	0	1	1	0	1	1	2	
1	x	0	0	1	1	1	1	1	1	0	0	1	1	3	
1	x	0	1	0	0	0	1	1	0	0	1	1	1	4	
1	x	0	1	0	1	1	0	1	1	0	1	1	1	5	
1	x	0	1	1	0	0	0	1	1	1	1	1	1	6	
1	x	0	1	1	1	1	1	1	0	0	0	0	1	7	
1	x	1	0	0	0	1	1	1	1	1	1	1	1	8	
1	x	1	0	0	1	1	1	1	0	0	1	1	1	9	
1	0	0	0	0	0	0	0	0	0	0	0	0	0	Blank	
0	0	x	x	x	x	1	1	1	1	1	1	1	0	8	
0	1	x	x	x	x	0	0	0	0	0	0	0	1	Blank	

* All non-valid BCD input codes produce a blank display

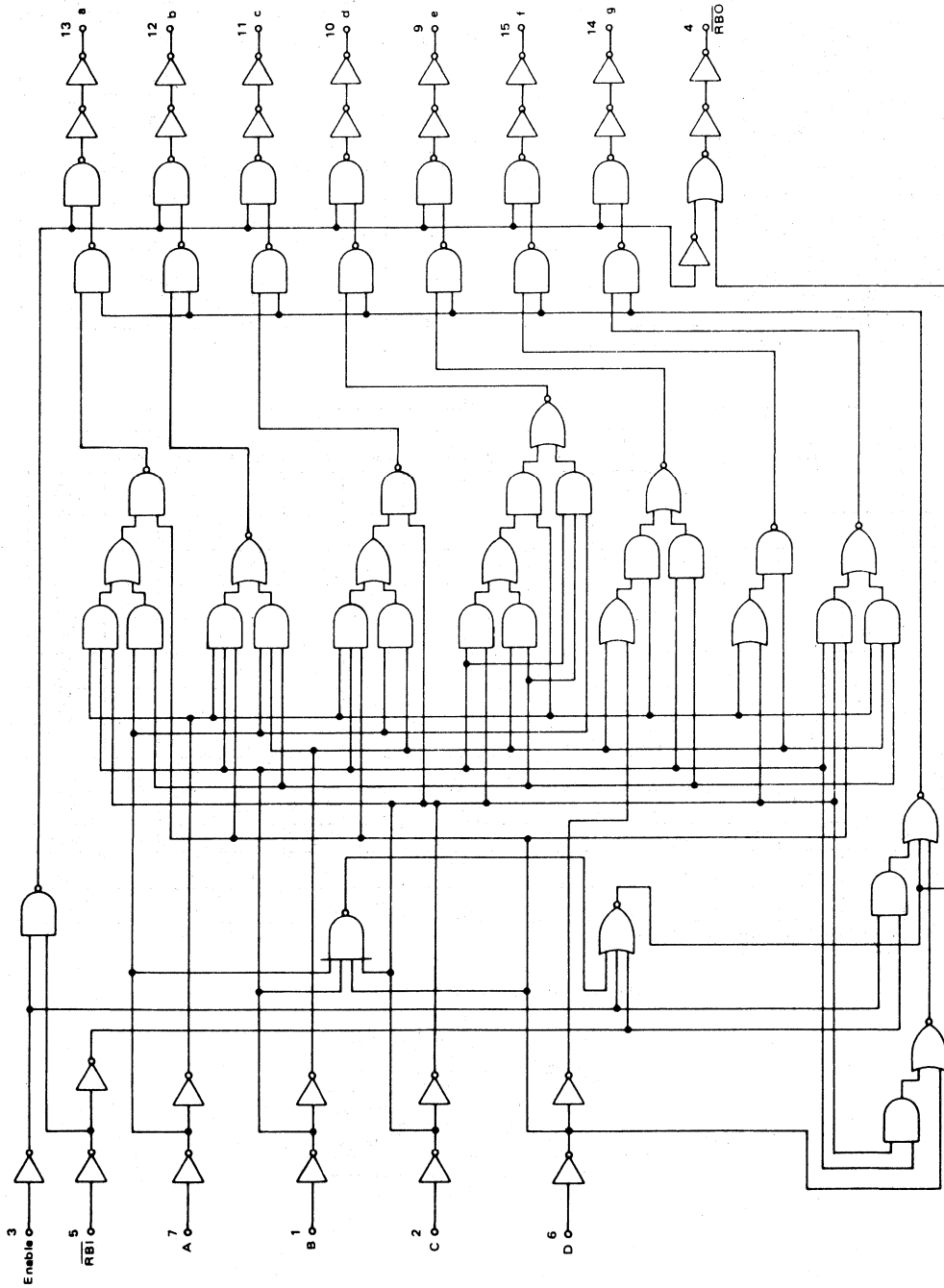
x = Don't Care

FIGURE 1 - SIGNAL WAVEFORMS



MC14558B

LOGIC DIAGRAM



6

MC14558B

TYPICAL APPLICATIONS

FIGURE 2 – LEADING AND TRAILING ZERO SUPPRESSION WITH LAMP TEST

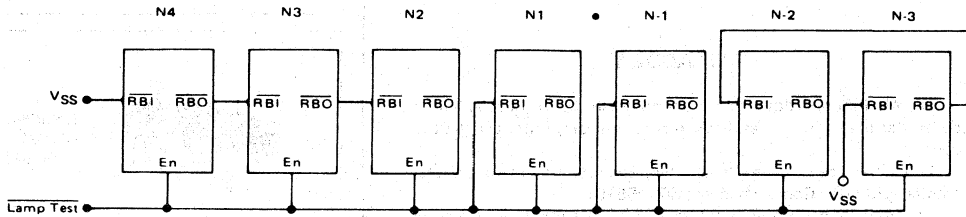


FIGURE 3 – LEADING AND TRAILING ZERO SUPPRESSION WITH PWM INTENSITY BLANKING AND NO LAMP TEST

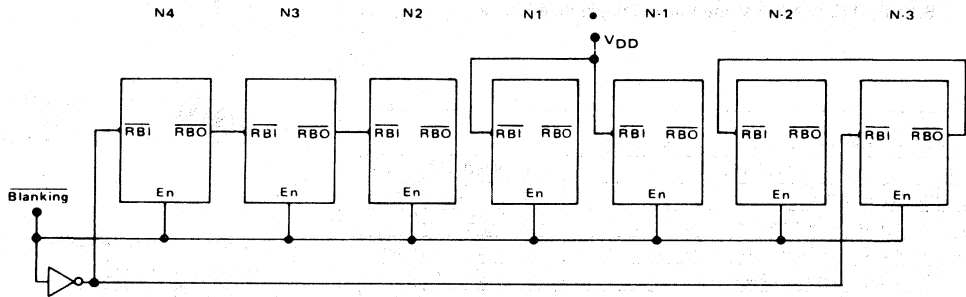
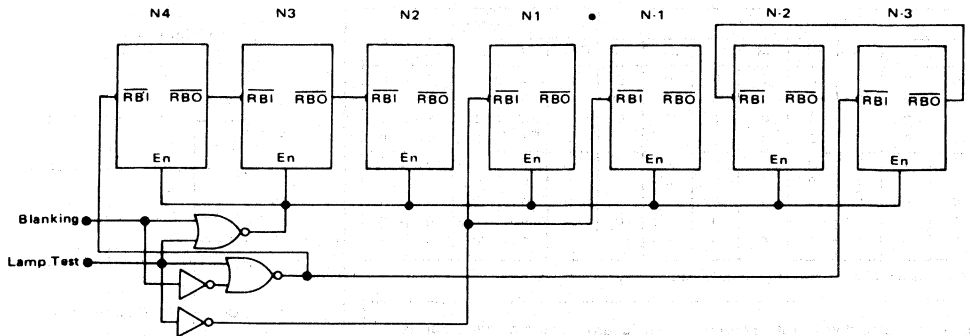


FIGURE 4 – ZERO SUPPRESSION WITH LAMP TEST AND INTENSITY BLANKING





MC14559B
See Page 398

MC14560B

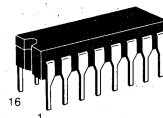
NBCD ADDER

The MC14560B adds two 4-bit numbers in NBCD (natural binary coded decimal) format, resulting in sum and carry outputs in NBCD code.

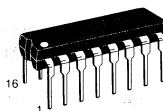
This device can also subtract when one set of inputs is complemented with a 9's Complementer (MC14561B).

All inputs and outputs are active high. The carry input for the least significant digit is connected to V_{SS} for no carry in.

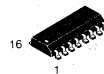
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range



L SUFFIX
CERAMIC
CASE 620



P SUFFIX
PLASTIC
CASE 648



D SUFFIX
SOIC
CASE 751B

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	-0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	-0.5 to $V_{DD} + 0.5$	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	± 10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.

†Temperature Derating: Plastic "P and D/DW" Packages: -7.0 mW/°C From 65°C To 125°C
Ceramic "L" Packages: -12 mW/°C From 100°C To 125°C

ORDERING INFORMATION

MC14XXXBCP Plastic
MC14XXXBCL Ceramic
MC14XXXBD SOIC

$T_A = -55^\circ$ to 125°C for all packages.

6

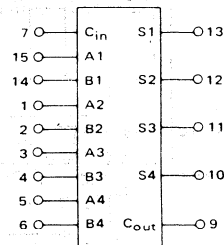
TRUTH TABLE*

INPUT									OUTPUT				
A4	A3	A2	A1	B4	B3	B2	B1	C_{in}	C_{out}	S4	S3	S2	S1
0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	1	0	0	0	0	1
0	1	0	0	0	0	1	1	0	0	0	1	1	1
0	1	0	0	0	0	1	1	1	0	1	0	0	0
0	1	1	1	0	1	0	0	0	1	0	0	0	1
0	1	1	1	0	1	0	0	1	1	0	0	1	0
1	0	0	0	0	1	0	1	0	1	0	0	1	1
0	1	1	0	1	0	0	0	0	1	0	1	0	0
1	0	0	1	1	0	0	1	1	1	1	0	0	1

*Partial truth table to show logic operation for representative input values.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

BLOCK DIAGRAM



$V_{DD} = \text{Pin } 16$
 $V_{SS} = \text{Pin } 8$

MC14560B

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V _{DD} Vdc	-55°C		25°C			125°C		Unit
			Min	Max	Min	Typ #	Max	Min	Max	
Output Voltage V _{in} = V _{DD} or 0	V _{OL}	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
		10	—	0.05	—	0	0.05	—	0.05	
V _{in} = 0 or V _{DD}	V _{OH}	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc
		10	9.95	—	9.95	10	—	9.95	—	
Input Voltage (V _O = 4.5 or 0.5 Vdc) (V _O = 9.0 or 1.0 Vdc) (V _O = 13.5 or 1.5 Vdc)	V _{IL}	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc
		10	—	3.0	—	4.50	3.0	—	3.0	
(V _O = 0.5 or 4.5 Vdc) (V _O = 1.0 or 9.0 Vdc) (V _O = 1.5 or 13.5 Vdc)	V _{IH}	5.0	3.5	—	3.5	2.75	—	3.5	—	Vdc
		10	7.0	—	7.0	5.50	—	7.0	—	
Output Drive Current (V _{OH} = 2.5 Vdc) (V _{OH} = 4.6 Vdc) (V _{OH} = 9.5 Vdc) (V _{OH} = 13.5 Vdc)	I _{OH}	5.0	-3.0	—	-2.4	-4.2	—	-1.7	—	mAdc
		10	-0.64	—	-0.51	-0.88	—	-0.36	—	
(V _{OL} = 0.4 Vdc) (V _{OL} = 0.5 Vdc) (V _{OL} = 1.5 Vdc)	I _{OL}	5.0	0.64	—	0.51	0.88	—	0.36	—	mAdc
		10	1.6	—	1.3	2.25	—	0.9	—	
		15	4.2	—	3.4	8.8	—	2.4	—	
Input Current	I _{in}	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	μAdc
Input Capacitance (V _{in} = 0)	C _{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)	I _{DD}	5.0	—	5.0	—	0.005	5.0	—	150	μAdc
		10	—	10	—	0.010	10	—	300	
		15	—	20	—	0.015	20	—	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C _L = 50 pF on all outputs, all buffers switching)	I _T	5.0	I _T = (1.68 μA/kHz) f + I _{DD}							μAdc
10	I _T = (3.35 μA/kHz) f + I _{DD}									
15	I _T = (5.03 μA/kHz) f + I _{DD}									

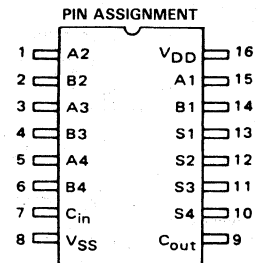
#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) \text{ Vfk}$$

where: I_T is in μA (per package), C_L in pF, V = (V_{DD} - V_{SS}) in volts, f in kHz is input frequency, and k = 0.005.



MC14560B

SWITCHING CHARACTERISTICS* ($C_L = 50 \text{ pF}$, $T_A = 25^\circ\text{C}$)

Characteristic	Symbol	V _{DD}	Min	Typ #	Max	Unit
Output Rise and Fall Time t_{TLH} , $t_{THL} = (1.5 \text{ ns/pF}) C_L + 25 \text{ ns}$ t_{TLH} , $t_{THL} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$ t_{TLH} , $t_{THL} = (0.55 \text{ ns/pF}) C_L + 9.5 \text{ ns}$	t_{TLH} , t_{THL}	5.0 10 15	— — —	100 50 40	200 100 80	ns
Propagation Delay Time A or B to S t_{PLH} , $t_{PHL} = (1.7 \text{ ns/pF}) C_L + 665 \text{ ns}$ t_{PLH} , $t_{PHL} = (0.66 \text{ ns/pF}) C_L + 297 \text{ ns}$ t_{PLH} , $t_{PHL} = (0.5 \text{ ns/pF}) C_L + 195 \text{ ns}$ A or B to C _{out} t_{PLH} , $t_{PHL} = (1.7 \text{ ns/pF}) C_L + 565 \text{ ns}$ t_{PLH} , $t_{PHL} = (0.66 \text{ ns/pF}) C_L + 197 \text{ ns}$ t_{PLH} , $t_{PHL} = (0.5 \text{ ns/pF}) C_L + 145 \text{ ns}$ C _{in} to C _{out} t_{PLH} , $t_{PHL} = (1.7 \text{ ns/pF}) C_L + 465 \text{ ns}$ t_{PLH} , $t_{PHL} = (0.66 \text{ ns/pF}) C_L + 187 \text{ ns}$ t_{PLH} , $t_{PHL} = (0.5 \text{ ns/pF}) C_L + 135 \text{ ns}$	t_{PLH} , t_{PHL}	5.0 10 15	— — —	750 330 220	2100 900 675	ns
Turn-Off Delay Time C _{in} to S $t_{PLH} = (1.7 \text{ ns/pF}) C_L + 715 \text{ ns}$ $t_{PLH} = (0.66 \text{ ns/pF}) C_L + 197 \text{ ns}$ $t_{PLH} = (0.5 \text{ ns/pF}) C_L + 215 \text{ ns}$	t_{PLH}	5.0 10 15	— — —	800 350 240	2250 975 750	ns
Turn-On Delay Time C _{in} to S $t_{PHL} = (1.7 \text{ ns/pF}) C_L + 565 \text{ ns}$ $t_{PHL} = (0.66 \text{ ns/pF}) C_L + 197 \text{ ns}$ $t_{PHL} = (0.5 \text{ ns/pF}) C_L + 145 \text{ ns}$	t_{PHL}	5.0 10 15	— — —	650 230 170	1800 600 450	ns

*The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

FIGURE 1 – POWER DISSIPATION WAVEFORMS

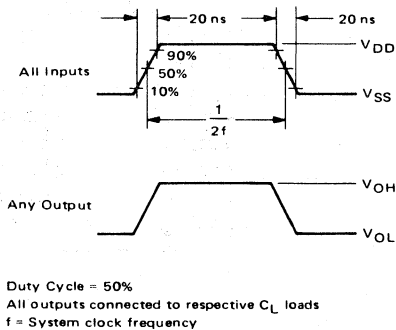
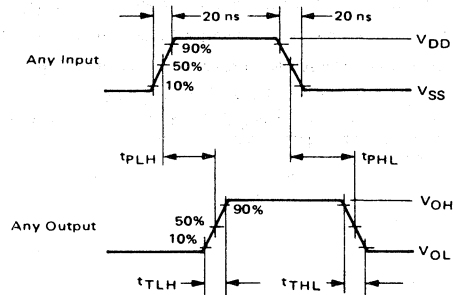


FIGURE 2 – SWITCHING TIME WAVEFORMS



MC14560B

FUNCTIONAL EQUIVALENT LOGIC DIAGRAM

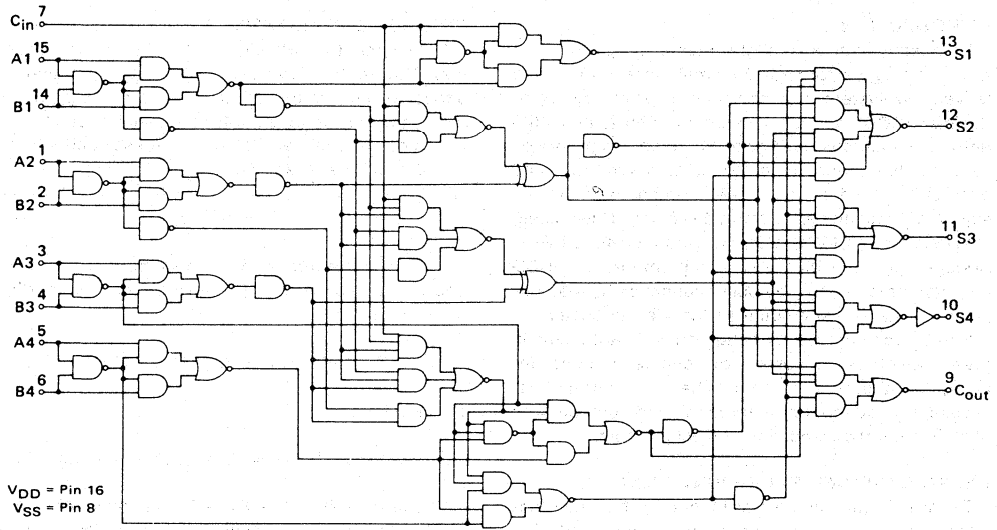
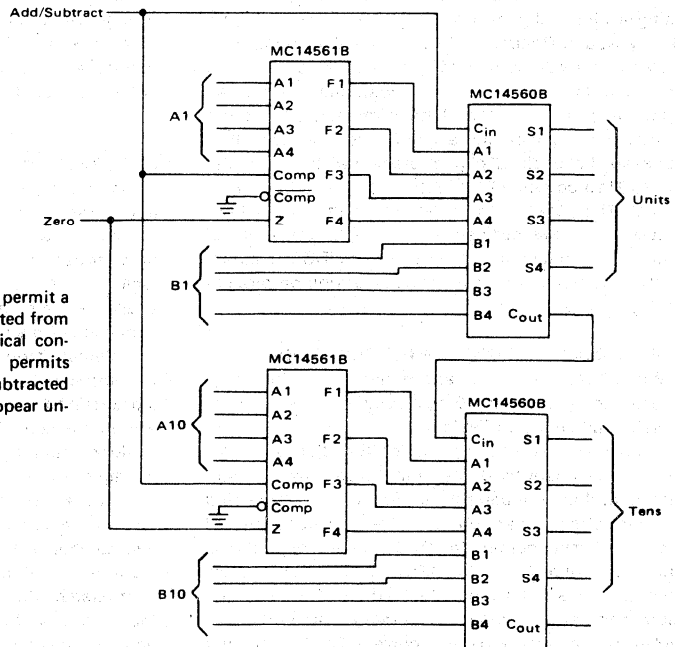


FIGURE 3 - PARALLEL ADD/SUBTRACT CIRCUIT



One MC14560B and MC14561B permit a BCD digit to be added to or subtracted from a second digit, such as in this typical configuration. A second MC14561B permits either digit to be added to or subtracted from the other, or either word to appear unmodified at the output.

TRUTH TABLE

Zero	Add/Subtract	Result
0	0	B plus A
0	1	B minus A
1	X	B

X = Don't Care

APPLICATIONS INFORMATION

INTRODUCTION

Frequently in small digital systems, simple decimal arithmetic is performed. Decimal data enters and leaves the system arithmetic unit in a binary coded decimal (BCD) format. The adder/subtractor in the arithmetic unit may be required to accept sign as well as magnitude, and generate sign, magnitude, and overflow. In the past, it has been cumbersome to build sign and magnitude adder/subtractors. Now, using Motorola's MSI CMOS functions, the MC14560 NBCD Adders and MC14561 9's Complementers, NBCD adder/subtractors may be built economically, with surprisingly low package count and moderate speed.

Some background information on BCD arithmetic is presented here, followed by simple circuits for unsigned adder/subtractors. The final circuit discussed is an adder/subtractor for signed numbers with complete overflow and sign correction logic.

DECIMAL NUMBER REPRESENTATION

Because logic elements are binary or two-state devices, decimal digits are generally represented as a group of bits in a weighted format. There are many possible binary codes which can be used to represent a decimal number. One of the most popular codes using 4 binary digits to represent 0 thru 9 is Natural Binary Coded Decimal (NBCD or 8-4-2-1 code).

NBCD is a weighted code. If a value of "0" or "1" is assigned to each of the bit positions, where the rightmost position is 2^0 and the leftmost is 2^3 , and the values are summed for a given code, the result is equal to the decimal digit represented by the code. Thus, 0110 equals $0 \cdot 2^3 + 1 \cdot 2^2 + 1 \cdot 2^1 + 0 \cdot 2^0 = 4 + 2 = 6$. The 1010, 1011, 1100, 1101, 1110, and 1111 binary codes are not used. Because of these illegal states, the addition and subtraction of NBCD numbers is more complex than similar calculations on straight binary numbers.

ADDITION OF UNSIGNED NBCD NUMBERS

When 2 NBCD digits, A and B, and a possible carry, C, are added, a total of 20 digit sums ($A + B + C$) are possible as shown in Table 1.

The binary representations for the digit sums 10 thru 19 are offset by 6, the number of unused binary states, and are not correct. An algorithm for obtaining the correct sum is shown in Figure 1. A conventional method of implementing the BCD addition algorithm is shown in Figure 2(a). The NBCD digits, A and B, are summed by a 4 bit binary full adder. The resultant (sum and carry) is input to a binary/BCD code converter which generates the correct BCD code and carry.

An NBCD adder block which performs the above function is available in a single CMOS package (MC14560). Figure 2(b) shows n decades cascaded for addition of n digit unsigned NBCD numbers. Add time is typically $0.1 + 0.2n \mu\text{s}$ for n decades. When the carry out of the most significant decade is a logical "1", an overflow is indicated.

COMPLEMENT ARITHMETIC

Complement arithmetic is used in NBCD subtraction. That is, the "complement" of the subtrahend is added to the minuend. The complementing process amounts to biasing the subtrahend such that all possible sums are positive. Consider the subtraction of the NBCD numbers, A and B:

$$R = A - B$$

where R is the result. Now bias both sides of the equation by $10^N - 1$ where N is the number of digits in A and B.

$$R + 10^N - 1 = A - B + 10^N - 1$$

Rearranging,

$$R + 10^N - 1 = A + (10^N - 1 - B)$$

The term $(10^N - 1 - B)$, $-B$ biased by $10^N - 1$, is known as the 9's complement of B. When $A > B$, $R + 10^N - 1 > 10^N - 1$; thus R is a positive number. To obtain R, 1 is added to $R + 10^N - 1$, and the carry term, 10^N , is dropped. The addition of 1 is called End Around Carry (EAC).

When $A < B$, $R + 10^N - 1 < 10^N - 1$, no EAC results and R is a negative number biased by $10^N - 1$; thus $R + 10^N - 1$ is the 9's complement of R.

SUBTRACTION OF UNSIGNED NBCD NUMBERS

Nine's complement arithmetic requires an element to perform the complementing function. An NBCD 9's complementer may be implemented using a 4 bit binary adder and 4 inverters, or with combinatorial logic. The Motorola MC14561 9's complementer is available in a single package. It has true and inverted complement disable, which allow straight-through or complement modes of operation. A "zero" line forces the output to "0". Figure 3 shows an NBCD subtractor block using the MC14560 and MC14561. Also shown are n cascaded blocks for subtraction of n digit unsigned numbers. Subtract time is $0.6 + 0.4n \mu\text{s}$ for n stages. Underflow (borrow) is indicated by a logical "0" on the carry output of the most significant digit. A "0" carry also indicates that the difference is a negative number in 9's complement form. If the result is input to a 9's complementer, as shown, and its mode controlled by the carry out of the most significant digit, the output of the complementer will be the correct negative magnitude. Note that the carry out of the most significant digit (MSD) is the input to carry in of the least significant digit (LSD). This End Around Carry is required because subtraction is done in 9's complement arithmetic.

By controlling the complement and overflow logic with an add/subtract line, both addition and subtraction are performed using the basic subtractor blocks (Figure 4).

MC14560B

TABLE 1 — Sum = A + B + C

Binary Sums	Decimal Number	Corrected Binary Sums
0000	0	0000
0001	1	0001
0010	2	0010
0011	3	0011
0100	4	0100
0101	5	0101
0110	6	0110
0111	7	0111
1000	8	1000
1001	9	1001
1010	10	0000 + Carry
1011	11	0001 + Carry
1100	12	0010 + Carry
1101	13	0011 + Carry
1110	14	0100 + Carry
1111	15	0101 + Carry
0000 + Carry	16	0110 + Carry
0001 + Carry	17	0111 + Carry
0010 + Carry	18	1000 + Carry
0011 + Carry	19	1001 + Carry

ADDITION AND SUBTRACTION OF SIGNED NBCD NUMBERS

Using MC14560 NBCD Adders and MC14561 9's Complementers, a sign and magnitude adder/subtractor can be configured (Figure 5). Inputs A and B are signed positive ($A_S, B_S = "0"$) or negative ($A_S, B_S = "1"$). B is added to or subtracted from A under control of an Add/Sub line (subtraction = "1"). The result, R, of the operation is positive signed, positive signed with overflow, negative signed, or negative signed with overflow. Add/subtract time is typically 0.6 + 0.4n μ s for n decades.

An exclusive-OR of Add/Sub line and B_S produces B' , which controls the B complementers. If B_S , the sign of B, is a logical "1" (B is negative) and the Add/Sub line is a "0" (add B to A), then the output of the exclusive-OR (B_S') is a logical "1" and B is complemented. If $B_S = "1"$ and Add/Sub = "1", B is not complemented since subtracting a negative number is the same as adding a positive number. When Add/Sub is a "1" and $B_S = "0"$, B_S' is a "1" and B is complemented. The A complementer is controlled by the A sign bit, A_S . When $A_S = "1"$, A is complemented.

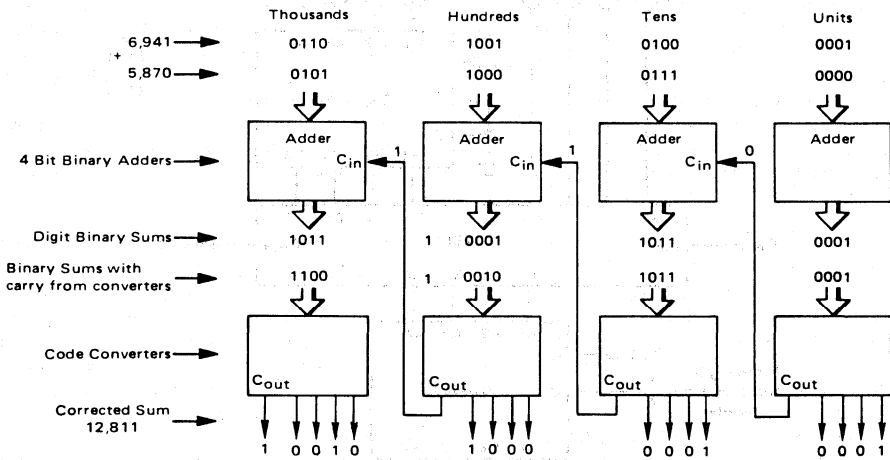


FIGURE 4 — Unsigned NBCD Addition Algorithm

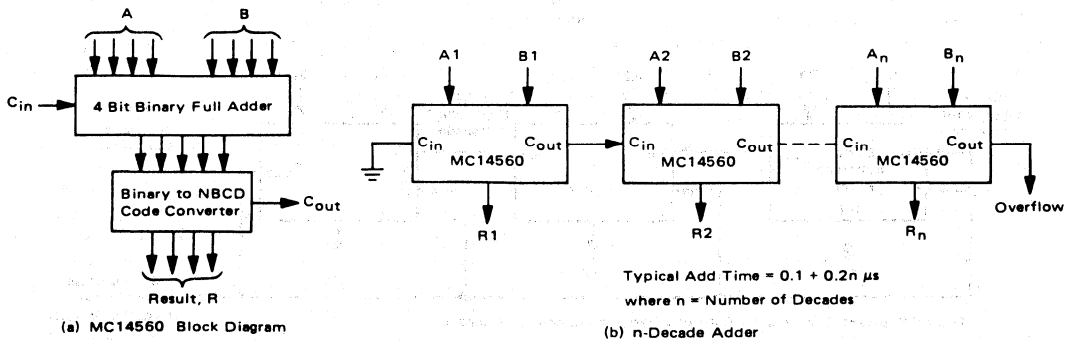


FIGURE 5 — Addition of Unsigned NBCD Numbers

MC14560B

The truth table and Karnaugh maps for sign, overflow, and End Around Carry are shown in Figures 6 and 7. Note the use of B_S' from the exclusive-OR of Add/Sub and B_S . B_S' eliminates Add/Sub as a variable in the truth table. As an example of truth table generation, consider an n decade adder/subtractor where $A_S = "0"$, $B_S = "1"$, and Add/Sub = $"0"$. B is in 9's complement form, $10^N - 1 - B$. Thus $A + (10^N - 1 - B) = 10^N - 1 + (A - B)$. There is no carry when $A \leq B$, and the sign is negative (sign = $"1"$). When A_S and B_S are opposite states and Add/Sub is a $"0"$ (add mode), no overflow can occur (overflow = $"0"$). The other output states are determined in a similar manner (see Figure 6).

From the Karnaugh maps it is apparent that End Around Carry is composed of the two symmetrical functions S2 and S3 of three variables with $A_S B_S' C_{out}$ as the center of symmetry. This is the definition of the majority logic function $M_3(ABC)$. Similarly the Sign is composed of the symmetrical functions S2(3) and S3(3) but with the center of symmetry translated

to $A_S B_S' C_{out}$. This is equivalent to the majority function $M_3(A_S B_S' \bar{C}_{out})$. Further evaluation of the maps and truth table reveal that Overflow can be generated by the exclusive-OR function of End Around Carry and Carry Out. This analysis results in a minimum device count consisting of one exclusive-OR package and one dual Majority Logic package to implement B_S' , EAC, Sign and Overflow. The logic connections of these devices are shown in Figure 5.

The output sign, R_S , complements the result of the add/subtract operation when $R_S = "1"$. This is required because the adder performs 9's complement arithmetic. Complementing, when R_S indicates the result is negative, restores sign and magnitude convention.

Several variations of the adder/subtractor are possible. For example, 9's complement is available at the output of the NBCD adders, and output complementers are eliminated if sign and magnitude output is not required.

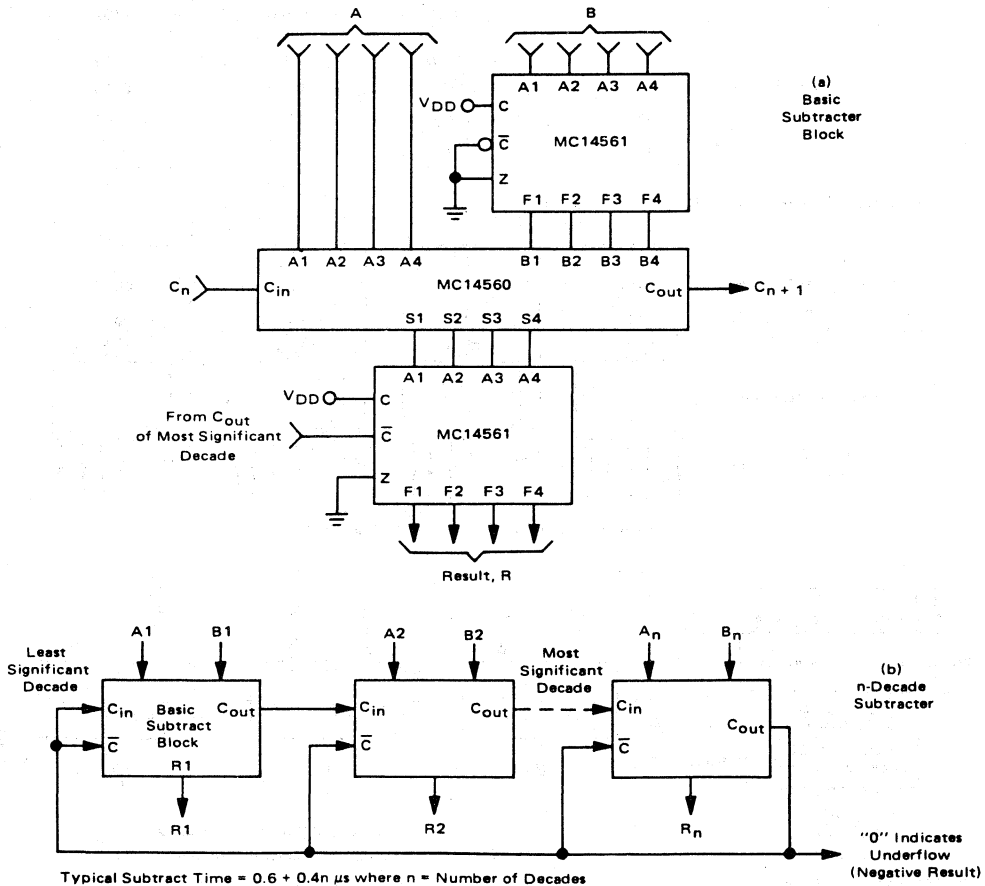


FIGURE 6 — Subtraction of Unsigned NBCD Numbers

MC14560B

SUMMARY

The concepts of binary code representations for decimal numbers, addition, and complement subtraction were discussed in detail. Using the basic Adder and Complementer MSI blocks, adder/subtractors for both signed and unsigned numbers were illustrated with examples.

REFERENCES

1. Chu, Y.: *Digital Computer Design Fundamentals*, New York, McGraw-Hill, 1962.
2. *McMOS Handbook*, Motorola Inc., 1st Edition.
3. Beuscher, H.: *Electronic Switching Theory and Circuits*, New York, Van Nostrand Reinhold, 1971.
4. Garrett, L.: CMOS May Help Majority Logic Win Designer's Vote, *Electronics*, July 19, 1973.
5. Richards, R.: *Digital Design*, New York, Wiley-Interscience, 1971.

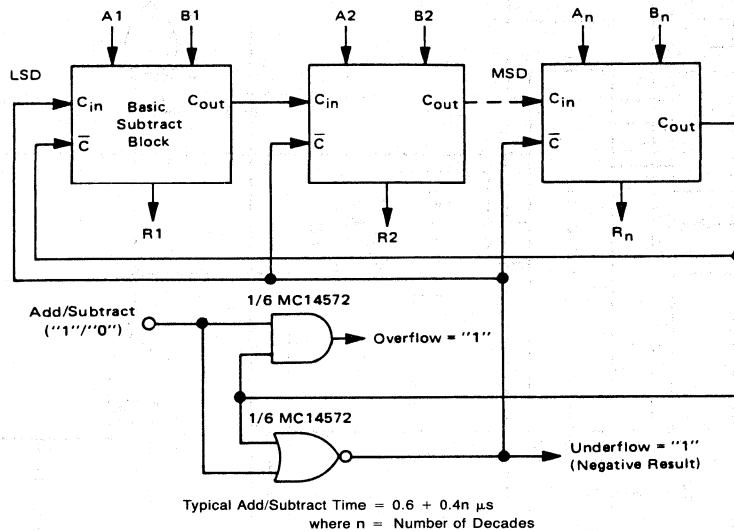
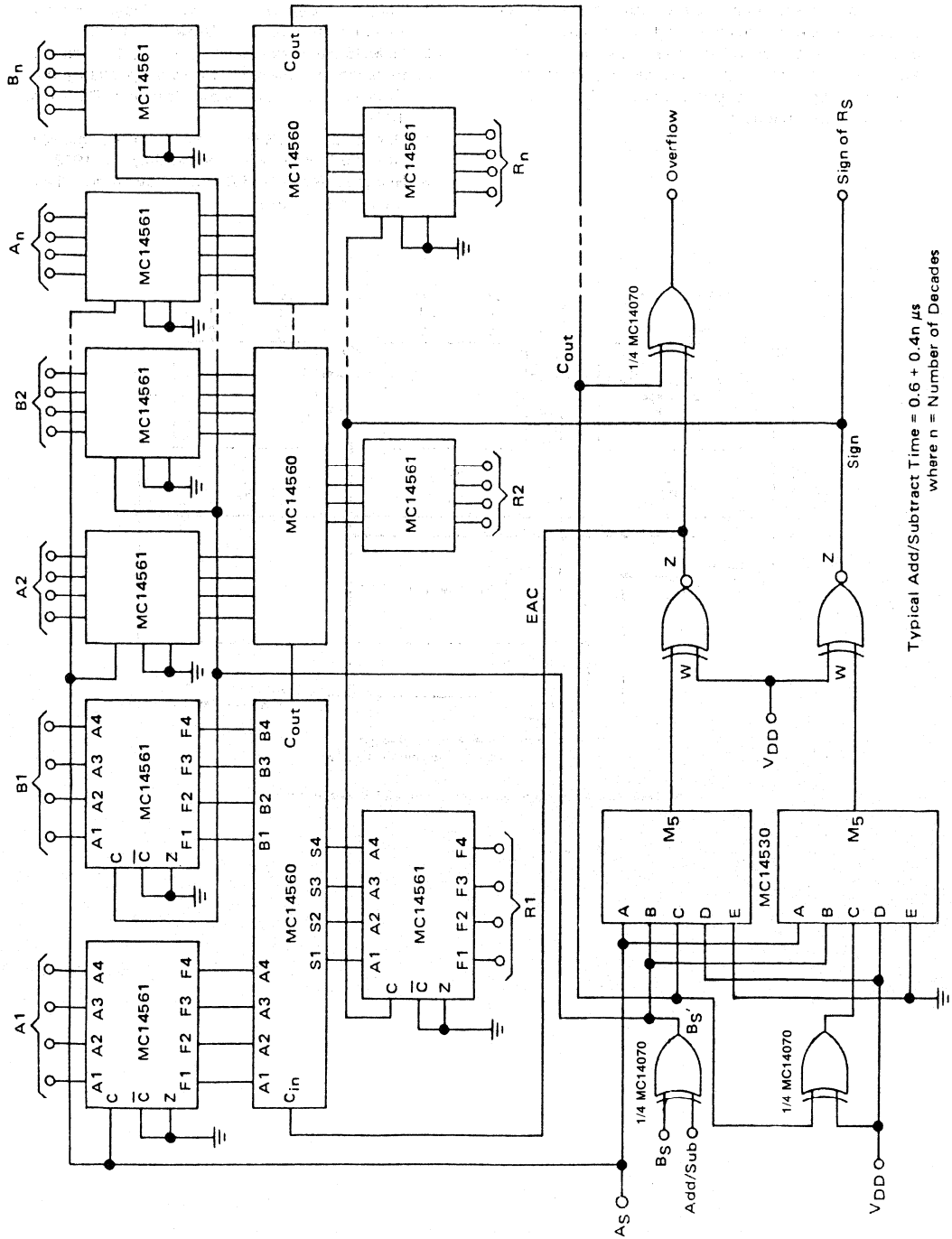


FIGURE 7 — Adder/Subtractor for Unsigned NBCD Numbers

MC14560B

FIGURE 9 — SIGN AND MAGNITUDE ADDER/SUBTRACTOR WITH OVERFLOW



Typical Add/Subtract Time = $0.6 + 0.4n \mu\text{s}$
 where n = Number of Decades

INPUTS		Arithmetic Expression for R* (Result) (N = Number of Digits, 10N = Modulus A, B, R are Positive Magnitudes)	OUTPUTS		
AS "1" = Neg	BS "1" = Neg		Cout "1" = Carry	End Around Carry (EAC) "1" = EAC	Sign of R "1" = Negative
0	0	$R = A + B$	No EAC ("0") because R is correct result.	Since A and B are positive signed, R is positive signed ("0").	When Cout = "0", there is no carry ($R < 10^N$) and thus no overflow ("0").
0	0				When Cout = "1", there is a carry ($R \geq 10^N$) and thus overflow ("1").
0	1	$R = A - B$ $= A + (10^N - 1 - B)$ $= A - B + 10^N - 1$	No EAC ("0") because 9's complement expression for R is correct result. EAC = "1" because expression for R is in error by 1.	$A \leq B$ when Cout = "0", thus sign of R must be negative ("1"). $A > B$ when Cout = "1", thus sign of R must be positive ("0").	
0	1				
1	0	$R = B - A$ $= B + (10^N - 1 - A)$ $= B - A + 10^N - 1$	No EAC ("0") because 9's complement expression for R is correct result. EAC = "1" because expression for R is in error by 1.	$B \leq A$ when Cout = "0", thus sign of R must be negative ("1"). $B > A$ when Cout = "1", thus sign of R must be positive ("0").	There is never an overflow when numbers of opposite sign are added.
1	0				
1	1	$R = -A - B$ $= (10^N - 1 - A) + (10^N - 1 - B)$ $= -(A + B) + 2 \times 10^N - 2$	EAC = "1" because 9's complement expression for R is in error by 1.	Since A and B are negative signed, R is negative signed ("1").	When Cout = "0", there is no carry ($R < 10^N$) and ($A + B$) > $10^N - 1$ indicating overflow ("1"). When Cout = "1", there is a carry ($R \geq 10^N$) and ($A + B$) $\leq 10^N - 1$ indicating no overflow ("0").
1	1				

*Output of Adders

FIGURE 9 — Truth Table Generation for EAC, Sign, and Overflow Logic

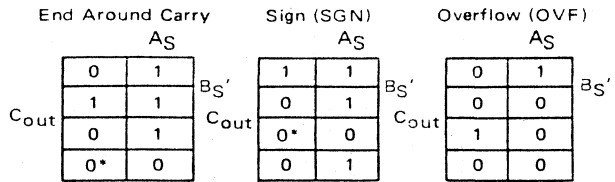
MC14560B

TRUTH TABLE

INPUTS			OUTPUTS		
A _S	B _S '	C _{out}	EAC	SGN	OVF
0	0	0	0	0	0
0	1	0	0	1	0
1	0	0	0	1	0
1	1	0	1	1	1
0	0	1	0	0	1
0	1	1	1	0	0
1	0	1	1	0	0
1	1	1	1	1	0

B_S = (Add/Sub) ⊕ B_S
 A_S = Sign of A ("1" = Negative)
 B_S = Sign of B ("1" = Negative)
 C_{out} = Adder Carry Out

KARNAUGH MAPS



* = Center of Symmetry

$$\begin{aligned}
 \text{EAC} &= \text{S2} (A_S B_S' C_{out}) + \text{S3} (A_S B_S' \bar{C}_{out}) \\
 &= \text{M}_3 (A_S B_S' C_{out})
 \end{aligned}$$

$$\begin{aligned}
 \text{SGN} &= \text{S2} (A_S B_S' \bar{C}_{out}) + \text{S3} (A_S B_S' C_{out}) \\
 &= \text{M}_3 (A_S B_S' C_{out})
 \end{aligned}$$

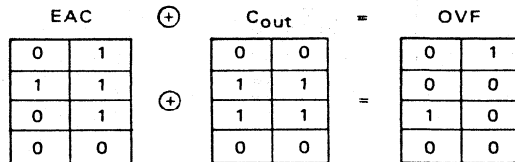


FIGURE 10 — Mapping of EAC, Sign and Overflow Logic



MOTOROLA

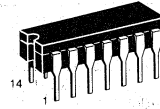
9's COMPLEMENTER

The MC14561B 9's complementer is a companion to the MC14560B NBCD adder to allow BCD subtraction. A BCD number (8-4-2-1 code) is applied to the inputs ($A_1 = 2^0$, $A_2 = 2^1$, $A_3 = 2^2$, $A_4 = 2^3$). If the complement control (Comp) is low, the BCD number appears at the outputs unmodified. The complement disable (Comp) allows the complement control to be gated, or an inverted control signal to be used. If the complement input is high and the disable input low, the 9's complement of the number is displayed at the outputs. The zero control (Z), when high, forces the outputs low regardless of the state of the other inputs.

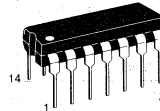
When the MC14561B is used to perform BCD subtraction in conjunction with the MC14560B NBCD adder, the complement control becomes an add/subtract control.

- All Inputs Buffered
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-Power TTL Loads or One Low-Power Schottky TTL Load Over the Rated Temperature Range

MC14561B



L SUFFIX
CERAMIC
CASE 632



P SUFFIX
PLASTIC
CASE 646



D SUFFIX
SOIC
CASE 751A

ORDERING INFORMATION

- MC14XXXBCP Plastic
- MC14XXXBCL Ceramic
- MC14XXXBD SOIC

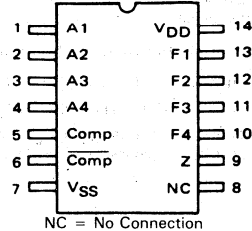
$T_A = -55^\circ$ to 125°C for all packages.

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	-0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	-0.5 to $V_{DD} + 0.5$	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	± 10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	-65 to +150	$^\circ\text{C}$
T_L	Lead Temperature (8-Second Soldering)	260	$^\circ\text{C}$

*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P and D/DW" Packages: -7.0 mW/ $^\circ\text{C}$ From 65 $^\circ\text{C}$ To 125 $^\circ\text{C}$
Ceramic "L" Packages: -12 mW/ $^\circ\text{C}$ From 100 $^\circ\text{C}$ To 125 $^\circ\text{C}$

PIN ASSIGNMENT



NC = No Connection

TRUTH TABLE

Z	Comp	Comp	F1	F2	F3	F4	Mode
0	0	0	A1	A2	A3	A4	Straight-through
0	0	1					
0	1	1					
0	1	0	$\bar{A}1$	A2	$A2\bar{A}3 + \bar{A}2A3$	$\bar{A}2\bar{A}3\bar{A}4$	Complement
1	X	X	0	0	0	0	Zero

X = Don't Care.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

MC14561B

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V _{DD} Vdc	-55°C		25°C			125°C		Unit
			Min	Max	Min	Typ #	Max	Min	Max	
Output Voltage V _{in} = V _{DD} or 0	V _{OL}	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
		10	—	0.05	—	0	0.05	—	0.05	
V _{in} = 0 or V _{DD}	V _{OH}	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc
		10	9.95	—	9.95	10	—	9.95	—	
Input Voltage (V _O = 4.5 or 0.5 Vdc) (V _O = 9.0 or 1.0 Vdc) (V _O = 13.5 or 1.5 Vdc)	V _{IL}	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc
		10	—	3.0	—	4.50	3.0	—	3.0	
(V _O = 0.5 or 4.5 Vdc) (V _O = 1.0 or 9.0 Vdc) (V _O = 1.5 or 13.5 Vdc)	V _{IH}	5.0	3.5	—	3.5	2.75	—	3.5	—	Vdc
		10	7.0	—	7.0	5.50	—	7.0	—	
Output Drive Current (V _{OH} = 2.5 Vdc) (V _{OH} = 4.6 Vdc) (V _{OH} = 9.5 Vdc) (V _{OH} = 13.5 Vdc)	Source I _{OH}	5.0	-3.0	—	-2.4	-4.2	—	-1.7	—	mAdc
		5.0	-0.64	—	-0.51	-0.88	—	-0.36	—	
(V _{OL} = 0.4 Vdc) (V _{OL} = 0.5 Vdc) (V _{OL} = 1.5 Vdc)	Sink I _{OL}	5.0	0.64	—	0.51	0.88	—	0.36	—	mAdc
		10	1.6	—	1.3	2.25	—	0.9	—	
15	4.2	—	3.4	8.8	—	2.4	—	—		
Input Current	I _{in}	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	μAdc
Input Capacitance (V _{in} = 0)	C _{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)	I _{DD}	5.0	—	5.0	—	0.005	5.0	—	150	μAdc
		10	—	10	—	0.010	10	—	300	
		15	—	20	—	0.015	20	—	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C _L = 50 pF on all outputs, all buffers switching)	I _T	5.0	I _T = (1.5 μA/kHz) f + I _{DD}							μAdc
		10	I _T = (3.0 μA/kHz) f + I _{DD}							
		15	I _T = (4.5 μA/kHz) f + I _{DD}							

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) \text{ Vfk}$$

where: I_T is in μA (per package), C_L in pF, V = (V_{DD} - V_{SS}) in volts, f in kHz is input frequency, and k = 0.004.

MC14561B

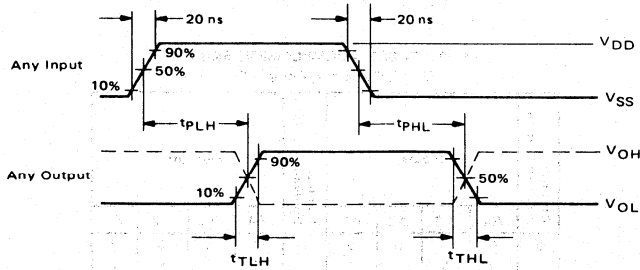
SWITCHING CHARACTERISTICS* ($C_L = 50 \text{ pF}$, $T_A = 25^\circ\text{C}$)

Characteristic	Symbol	V_{DD}	Min	Typ #	Max	Unit
Output Rise and Fall Time	t_{TLH} , t_{THL}					ns
t_{TLH} , $t_{THL} = (1.5 \text{ ns/pF}) C_L + 25 \text{ ns}$		5.0	—	100	200	
t_{TLH} , $t_{THL} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$		10	—	50	100	
t_{TLH} , $t_{THL} = (0.55 \text{ ns/pF}) C_L + 9.5 \text{ ns}$		15	—	40	80	
Propagation Delay Time	t_{PLH} , t_{PHL}					ns
t_{PLH} , $t_{PHL} = (1.7 \text{ ns/pF}) C_L + 315 \text{ ns}$		5.0	—	400	1000	
t_{PLH} , $t_{PHL} = (0.66 \text{ ns/pF}) C_L + 127 \text{ ns}$		10	—	160	400	
t_{PLH} , $t_{PHL} = (0.5 \text{ ns/pF}) C_L + 95 \text{ ns}$		15	—	120	300	

*The formulas given are for the typical characteristics only at 25°C .

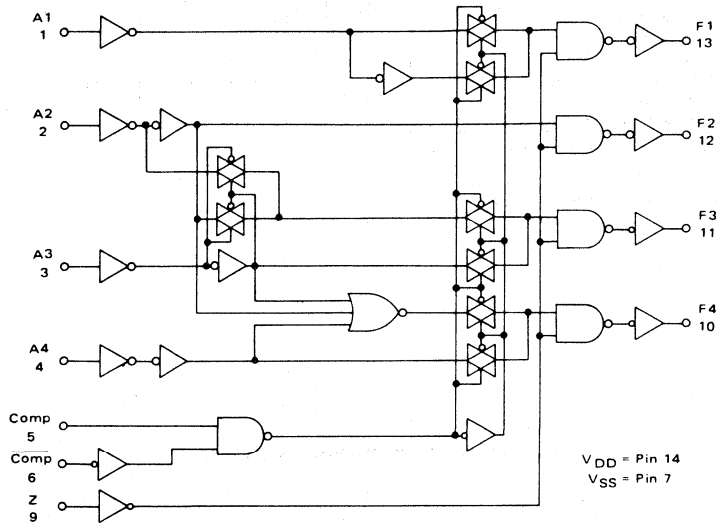
#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

FIGURE 1 – SWITCHING TIME WAVEFORMS



MC14561B

LOGIC DIAGRAM



TRUTH TABLE – COMPLEMENT MODE
(Z = 0, Comp = 1, Comp = 0)

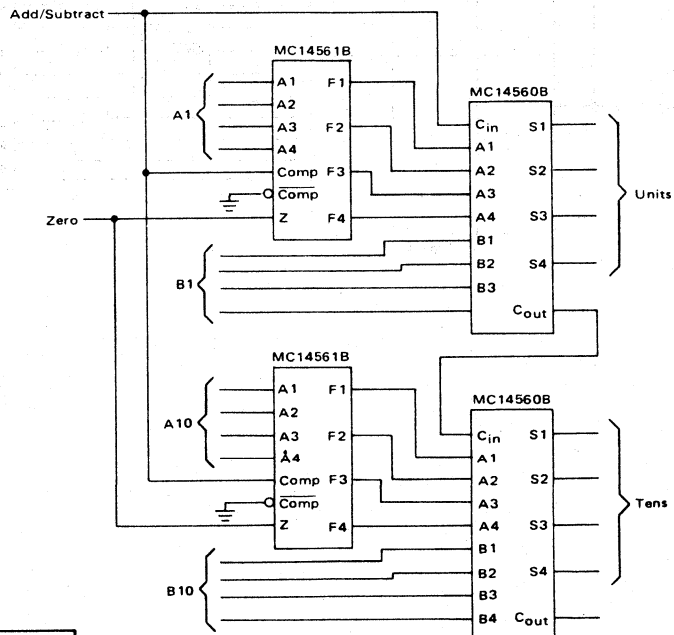
Decimal Equivalent Input	Inputs				Decimal Equivalent Output	Outputs				
	A4	A3	A2	A1		F4	F3	F2	F1	
0	0	0	0	0	9	1	0	0	1	
1	0	0	0	1	8	1	0	0	0	
2	0	0	1	0	7	0	1	1	1	
3	0	0	1	1	6	0	1	1	0	
4	0	1	0	0	5	0	1	0	1	
5	0	1	0	1	4	0	1	0	0	
6	0	1	1	0	3	0	0	1	1	
7	0	1	1	1	2	0	0	1	0	
8	1	0	0	0	1	0	0	0	1	
9	1	0	0	1	0	0	0	0	0	
Illegal BCD Input Codes	10	1	0	1	0	7	0	1	1	1
	11	1	0	1	1	6	0	1	1	0
	12	1	1	0	0	5	0	1	0	1
	13	1	1	0	1	4	0	1	0	0
	14	1	1	1	0	3	0	0	1	1
	15	1	1	1	1	2	0	0	1	0

MC14561B

TYPICAL APPLICATIONS

One MC14560B and one MC14561B permit a BCD digit to be added to or subtracted from a second digit, such as in the typical configurations in Figures 2 and 3. A second MC14561B permits either digit to be added to or subtracted from the other, or either word to appear unmodified at the output.

FIGURE 2 - PARALLEL ADD/SUBTRACT CIRCUIT (10's COMPLEMENT)



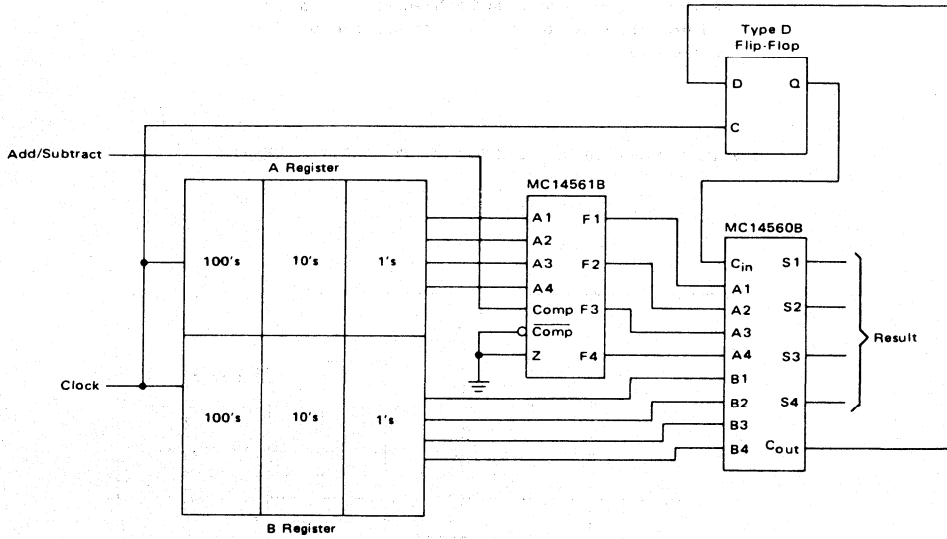
TRUTH TABLE

Zero	Add/Subtract	Result
0	0	B plus A
0	1	B minus A
1	X	B

X = Don't Care

MC14561B

FIGURE 3 – SERIAL ADD/SUBTRACT CIRCUIT



6



MOTOROLA

MC14562B

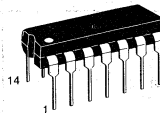
128-BIT STATIC SHIFT REGISTER

The MC14562B is a 128-bit static shift register constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. Data is clocked in and out of the shift register on the positive edge of the clock input. Data outputs are available every 16 bits, from 16 through bit 128. This complementary MOS shift register is primarily used where low power dissipation and/or high noise immunity is desired.

- Diode Protection on All Inputs
- Fully Static Operation
- Cascadable to Provide Longer Shift Register Lengths
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range



L SUFFIX
CERAMIC
CASE 632



P SUFFIX
PLASTIC
CASE 646



D SUFFIX
SOIC
CASE 751A

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V _{DD}	DC Supply Voltage	-0.5 to +18.0	V
V _{in} , V _{out}	Input or Output Voltage (DC or Transient)	-0.5 to V _{DD} + 0.5	V
I _{in} , I _{out}	Input or Output Current (DC or Transient), per Pin	± 10	mA
P _D	Power Dissipation, per Package†	500	mW
T _{stg}	Storage Temperature	-65 to +150	°C
T _L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.

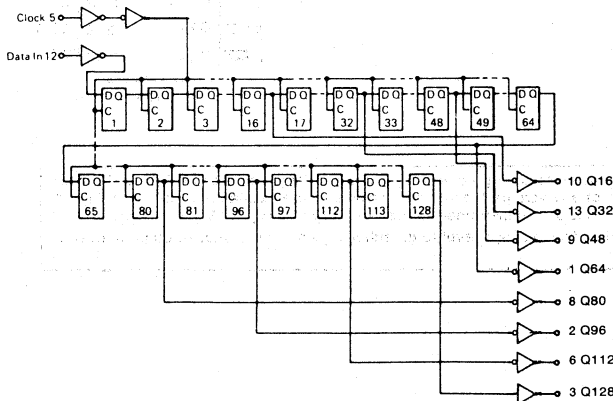
†Temperature Derating: Plastic "P and D/DW" Packages: -7.0 mW/°C From 65°C To 125°C
Ceramic "L" Packages: -12 mW/°C From 100°C To 125°C

ORDERING INFORMATION

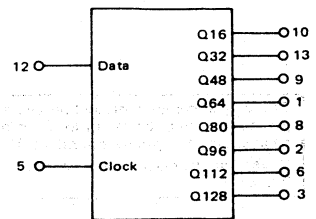
MC14XXXBCP Plastic
MC14XXXBCL Ceramic
MC14XXXBD SOIC

T_A = -55° to 125°C for all packages.

LOGIC DIAGRAM



BLOCK DIAGRAM



Pins 4 and 11
not used.

V_{DD} = Pin 14
V_{SS} = Pin 7

MC14562B

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V _{DD} Vdc	-55°C		25°C			125°C		Unit
			Min	Max	Min	Typ #	Max	Min	Max	
Output Voltage V _{in} = V _{DD} or 0 V _{in} = 0 or V _{DD}	V _{OL}	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
		10	—	0.05	—	0	0.05	—	0.05	
		15	—	0.05	—	0	0.05	—	0.05	
	V _{OH}	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc
		10	9.95	—	9.95	10	—	9.95	—	
		15	14.95	—	14.95	15	—	14.95	—	
Input Voltage (V _O = 4.5 or 0.5 Vdc) (V _O = 9.0 or 1.0 Vdc) (V _O = 13.5 or 1.5 Vdc) (V _O = 0.5 or 4.5 Vdc) (V _O = 1.0 or 9.0 Vdc) (V _O = 1.5 or 13.5 Vdc)	V _{IL}	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc
		10	—	3.0	—	4.50	3.0	—	3.0	
		15	—	4.0	—	6.75	4.0	—	4.0	
	V _{IH}	5.0	3.5	—	3.5	2.75	—	3.5	—	Vdc
		10	7.0	—	7.0	5.50	—	7.0	—	
		15	11	—	11	8.25	—	11	—	
Output Drive Current (V _{OH} = 2.5 Vdc) (V _{OH} = 4.6 Vdc) (V _{OH} = 9.5 Vdc) (V _{OH} = 13.5 Vdc) (V _{OL} = 0.4 Vdc) (V _{OL} = 0.5 Vdc) (V _{OL} = 1.5 Vdc)	Source I _{OH}	5.0	-3.0	—	-2.4	-4.2	—	-1.7	—	mAdc
		5.0	-0.64	—	-0.51	-0.88	—	-0.36	—	
		10	-1.6	—	-1.3	-2.25	—	-0.9	—	
		15	-4.2	—	-3.4	-8.8	—	-2.4	—	
	Sink I _{OL}	5.0	0.64	—	0.51	0.88	—	0.36	—	mAdc
		10	1.6	—	1.3	2.25	—	0.9	—	
15		4.2	—	3.4	8.8	—	2.4	—		
Input Current	I _{in}	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	μAdc
Input Capacitance (V _{in} = 0)	C _{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)	I _{DD}	5.0	—	5.0	—	0.010	5.0	—	150	μAdc
		10	—	10	—	0.020	10	—	300	
		15	—	20	—	0.030	20	—	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C _L = 50 pF on all outputs, all buffers switching)	I _T	5.0	I _T = (1.94 μA/kHz) f + I _{DD}						μAdc	
		10	I _T = (3.81 μA/kHz) f + I _{DD}							
		15	I _T = (5.52 μA/kHz) f + I _{DD}							

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

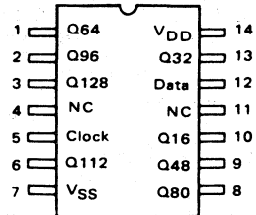
**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) V_{fk}$$

where: I_T is in μA (per package), C_L in pF, V = (V_{DD} - V_{SS}) in volts, f in kHz is input frequency, and k = 0.004.

PIN ASSIGNMENT



NC = No Connection

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range V_{SS} ≤ (V_{in} or V_{out}) ≤ V_{DD}. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

MC14562B

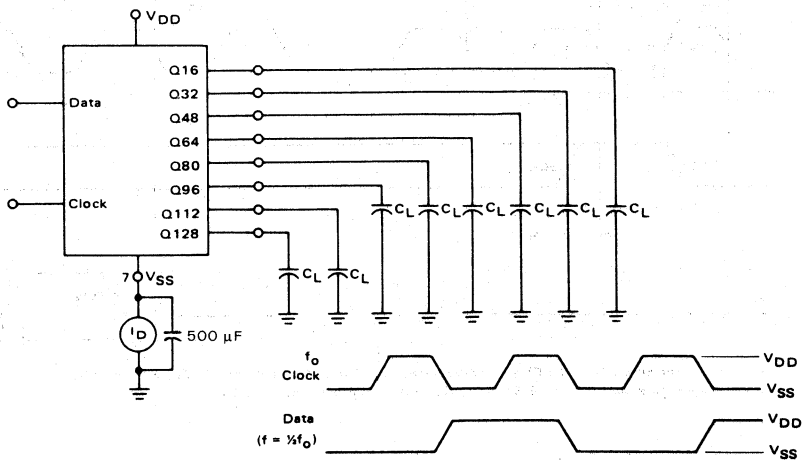
SWITCHING CHARACTERISTICS* ($C_L = 50 \text{ pF}$, $T_A = 25^\circ\text{C}$)

Characteristic	Symbol	V_{DD}	Min	Typ #	Max	Unit
Output Rise and Fall Time t_{TLH} , $t_{THL} = (1.5 \text{ ns/pF}) C_L + 25 \text{ ns}$ t_{TLH} , $t_{THL} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$ t_{TLH} , $t_{THL} = (0.55 \text{ ns/pF}) C_L + 9.5 \text{ ns}$	t_{TLH} , t_{THL}	5.0 10 15	— — —	100 50 40	200 100 80	ns
Propagation Delay Time Clock to Q t_{PLH} , $t_{PHL} = (1.7 \text{ ns/pF}) C_L + 515 \text{ ns}$ t_{PLH} , $t_{PHL} = (0.66 \text{ ns/pF}) C_L + 217 \text{ ns}$ t_{PLH} , $t_{PHL} = (0.5 \text{ ns/pF}) C_L + 145 \text{ ns}$	t_{PLH} , t_{PHL}	5.0 10 15	— — —	600 250 170	1200 500 340	ns
Clock Pulse Width (50% Duty Cycle)	t_{WH}	5.0 10 15	600 220 150	300 110 75	— — —	ns
Clock Pulse Frequency	f_{cl}	5.0 10 15	— — —	1.9 5.6 8.0	1.1 3.0 4.0	MHz
Data to Clock Setup Time	$t_{su}(1)$	5.0 10 15	-20 -10 0	-170 -64 -60	— — —	ns
	$t_{su}(0)$	5.0 10 15	-20 -10 0	-91 -58 -48	— — —	ns
Data to Clock Hold Time	$t_h(1)$	5.0 10 15	350 165 155	263 109 100	— — —	ns
	$t_h(0)$	5.0 10 15	350 200 140	267 93 140	— — —	ns
Clock Input Rise and Fall Times	t_r , t_f	5.0 10 15	— — —	— — —	15 5 4	μs

*The formulas given are for the typical characteristics only at 25°C.

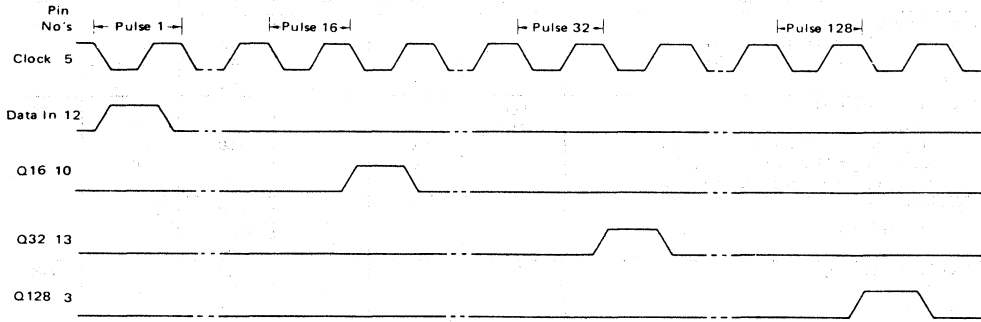
#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

FIGURE 1 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORMS

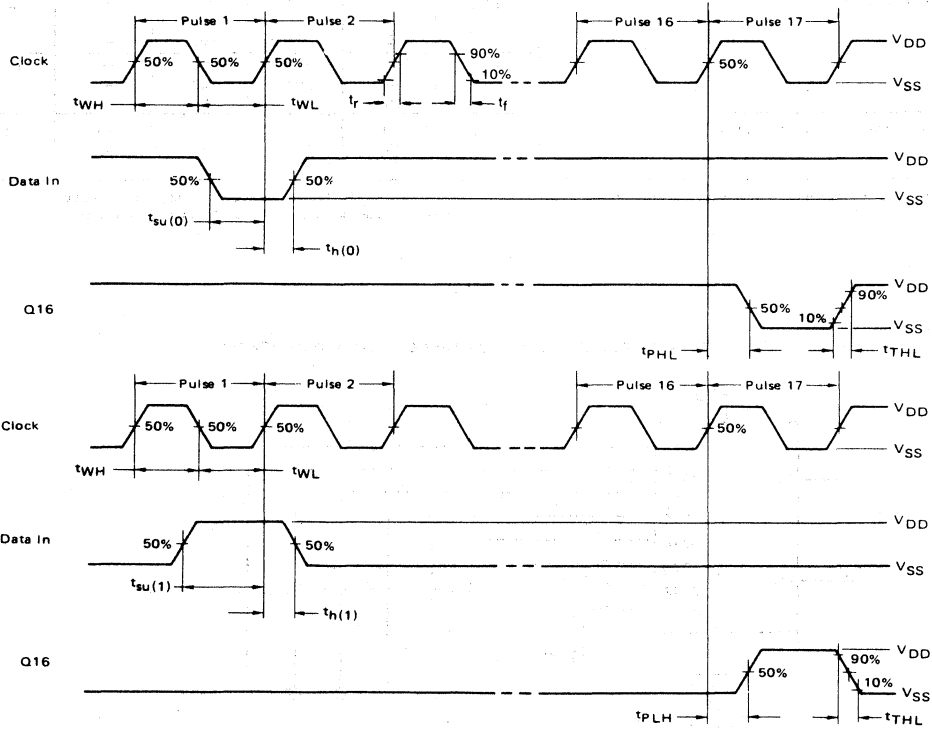


MC14562B

TIMING DIAGRAM



AC TEST WAVEFORMS



Note: The remaining Data-Bit Outputs (Q32, Q48, Q64, Q80, Q96, Q112 and Q128) will occur at Clock Pulse 32, 48, 64, 80, 96, 112, 128 in the same relationship as Q16.

6



MOTOROLA

MC14566B

INDUSTRIAL TIME BASE GENERATOR

The MC14566B industrial time base generator is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. This device consists of a divide-by-10 ripple counter and a divide-by-5 or divide-by-6 ripple counter to permit stable time generation from a 50 or 60 Hz line. By cascading this device as divide-by-60 counters, seconds and minutes can be counted and are available in BCD format at the circuit outputs. An internal monostable multivibrator is included whose output can be used as a reset or clock pulse providing additional frequency flexibility. Also a pin has been included to allow divide-by-5 counting for generating 1.0 Hz from European 50 Hz line. Pin 11 = V_{DD} will cause $\div 5$.

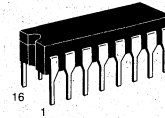
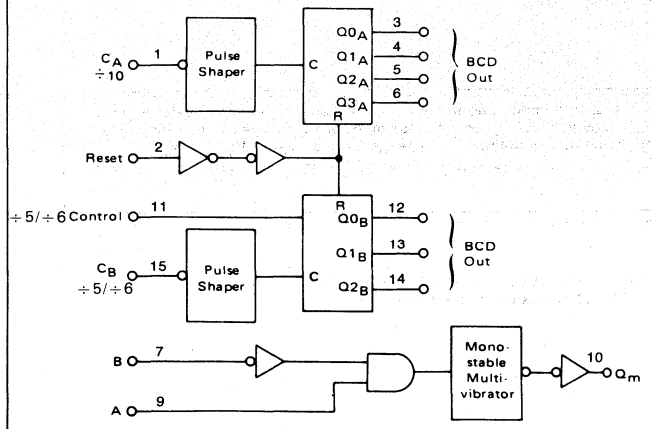
- Negative Edge Triggered Counters for Ease of Cascading
- Pulse Shapers on Counter Inputs Accept Slow Input Rise Times
- Monostable Multivibrator Positive or Negative Edge Triggered
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	-0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	-0.5 to $V_{DD} + 0.5$	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	± 10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
 †Temperature Derating: Plastic "P and D/DW" Packages: -7.0 mW/°C From 65°C To 125°C
 Ceramic "L" Packages: -12 mW/°C From 100°C To 125°C

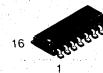
BLOCK DIAGRAM



L SUFFIX
 CERAMIC
 CASE 620



P SUFFIX
 PLASTIC
 CASE 648



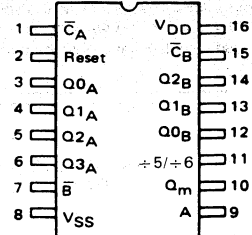
D SUFFIX
 SOIC
 CASE 751B

ORDERING INFORMATION

- MC14XXXBCP Plastic
- MC14XXXBCL Ceramic
- MC14XXXBD SOIC

$T_A = -55^\circ$ to 125° C for all packages.

PIN ASSIGNMENT



MC14566B

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V _{DD} Vdc	-55°C		25°C			125°C		Unit	
			Min	Max	Min	Typ #	Max	Min	Max		
Output Voltage V _{in} = V _{DD} or 0	V _{OL}	5.0	—	0.05	—	0	0.05	—	0.05	Vdc	
		10	—	0.05	—	0	0.05	—	0.05		
15		—	0.05	—	0	0.05	—	0.05			
V _{in} = 0 or V _{DD}	V _{OH}	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc	
		10	9.95	—	9.95	10	—	9.95	—		
		15	14.95	—	14.95	15	—	14.95	—		
Input Voltage (V _O = 4.5 or 0.5 Vdc) (V _O = 9.0 or 1.0 Vdc) (V _O = 13.5 or 1.5 Vdc)	V _{IL}	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc	
		10	—	3.0	—	4.50	3.0	—	3.0		
		15	—	4.0	—	6.75	4.0	—	4.0		
(V _O = 0.5 or 4.5 Vdc) (V _O = 1.0 or 9.0 Vdc) (V _O = 1.5 or 13.5 Vdc)	V _{IH}	5.0	3.5	—	3.5	2.75	—	3.5	—	Vdc	
		10	7.0	—	7.0	5.50	—	7.0	—		
		15	11	—	11	8.25	—	11	—		
Output Drive Current (V _{OH} = 2.5 Vdc) (V _{OH} = 4.6 Vdc) (V _{OH} = 9.5 Vdc) (V _{OH} = 13.5 Vdc)	Source	I _{OH}	5.0	-3.0	—	-2.4	—	-1.7	—	mAdc	
			5.0	-0.64	—	-0.51	-0.88	—	-0.36		—
			10	-1.6	—	-1.3	-2.25	—	-0.9		—
	Sink	I _{OL}	5.0	0.64	—	0.51	0.88	—	0.36	—	
			10	1.6	—	1.3	2.25	—	0.9	—	
			15	4.2	—	3.4	8.8	—	2.4	—	
Input Current	I _{in}	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	μAdc	
Input Capacitance (V _{in} = 0)	C _{in}	—	—	—	—	5.0	7.5	—	—	pF	
Quiescent Current (Per Package)	I _{DD}	5.0	—	5.0	—	0.005	5.0	—	150	μAdc	
		10	—	10	—	0.010	10	—	300		
		15	—	20	—	0.015	20	—	600		
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C _L = 50 pF on all outputs, all buffers switching)	I _T	5.0	I _T = (1.0 μA/kHz) f + I _{DD}							μAdc	
		10	I _T = (2.0 μA/kHz) f + I _{DD}								
		15	I _T = (3.0 μA/kHz) f + I _{DD}								

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) Vfk$$

where: I_T is in μA (per package), C_L in pF, V = (V_{DD} - V_{SS}) in volts, f in kHz is input frequency, and k = 0.001.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range V_{SS} ≤ (V_{in} or V_{out}) ≤ V_{DD}. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

MC14566B

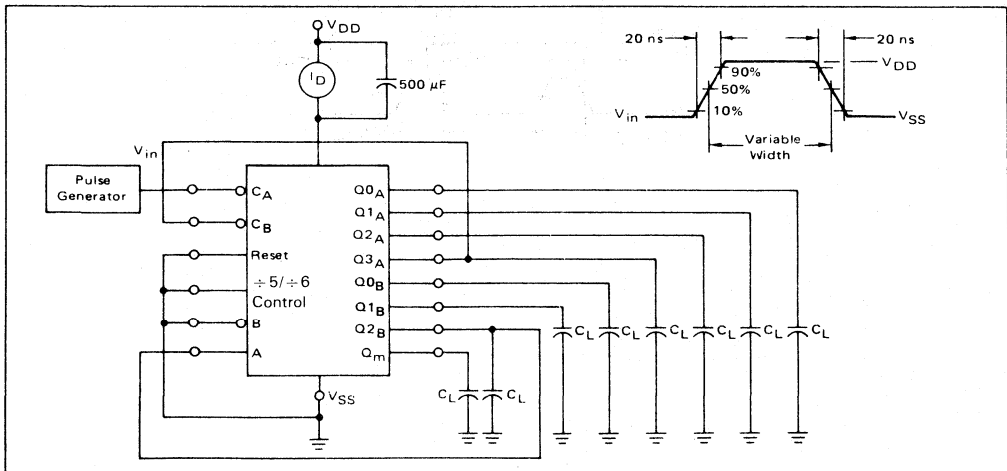
SWITCHING CHARACTERISTICS* ($C_L = 50 \text{ pF}$, $T_A = 25^\circ\text{C}$)

Characteristic	Symbol	V_{DD}	Min	Typ #	Max	Unit
Output Rise and Fall Time $t_{TLH}, t_{THL} = (1.5 \text{ ns/pF}) C_L + 25 \text{ ns}$ $t_{TLH}, t_{THL} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$ $t_{TLH}, t_{THL} = (0.55 \text{ ns/pF}) C_L + 9.5 \text{ ns}$	t_{TLH} , t_{THL}	5.0 10 15	— — —	100 50 40	200 100 80	ns
Propagation Delay Time, Clock to Q3A $t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 1365 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 497 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 295 \text{ ns}$	t_{PLH} , t_{PHL}	5.0 10 15	— — —	1450 530 320	4500 1500 1000	ns
Propagation Delay Time, Reset to Q3A $t_{PHL} = (1.7 \text{ ns/pF}) C_L + 845 \text{ ns}$ $t_{PHL} = (0.66 \text{ ns/pF}) C_L + 282 \text{ ns}$ $t_{PHL} = (0.5 \text{ ns/pF}) C_L + 185 \text{ ns}$	t_{PHL}	5.0 10 15	— — —	930 315 210	3000 1000 750	ns
Clock Pulse Width	$t_{WH(c)}$	5.0 10 15	1200 400 270	400 125 90	— — —	ns
Reset Pulse Width	$t_{WH(R)}$	5.0 10 15	1200 400 270	400 125 90	— — —	ns
Clock Pulse Frequency	f_{cl}	5.0 10 15	— — —	1.0 2.5 4.2	0.3 1.0 1.5	MHz
Clock Pulse Rise and Fall Time	t_{TLH} , t_{THL}	5.0 10 15	No Limit			—
Monostable Multivibrator Pulse Width	$t_{WH(Q_m)}$	5.0 10 15	1200 400 300	2800 900 600	— — —	ns

*The formulas given are for the typical characteristics only at 25°C.

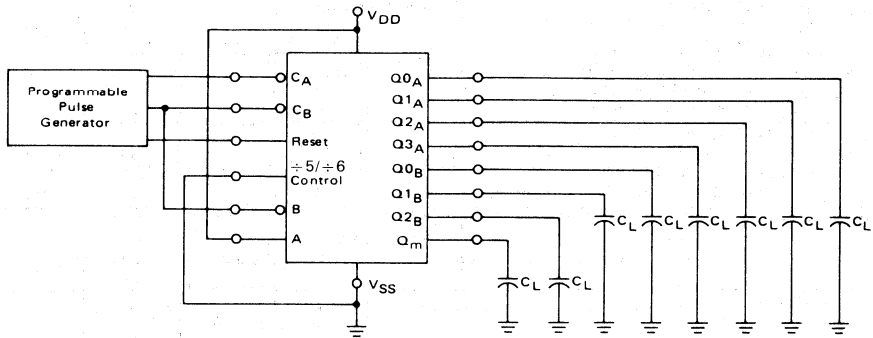
#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

FIGURE 1 - POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

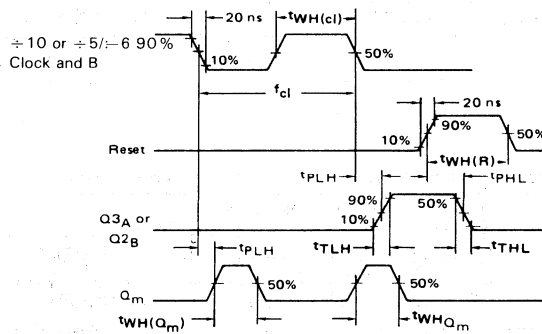


MC14566B

FIGURE 2 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

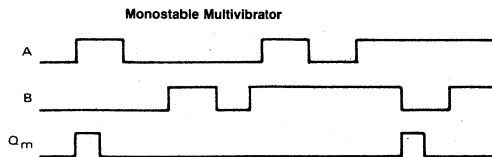
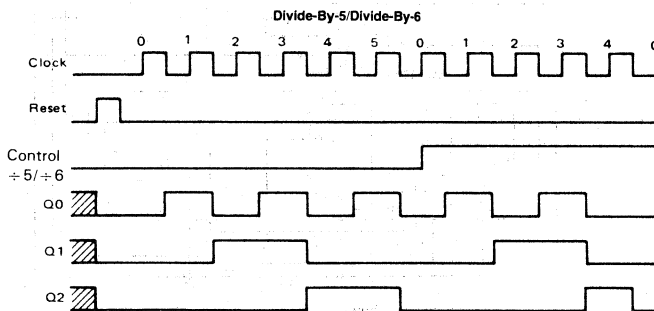
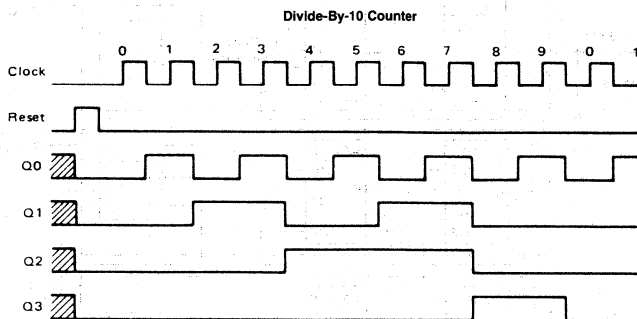


Note: Assume $\div 10$ Counter at "6" and $\div 5/\div 6$ Counter at "2" at beginning of sequence.



MC14566B

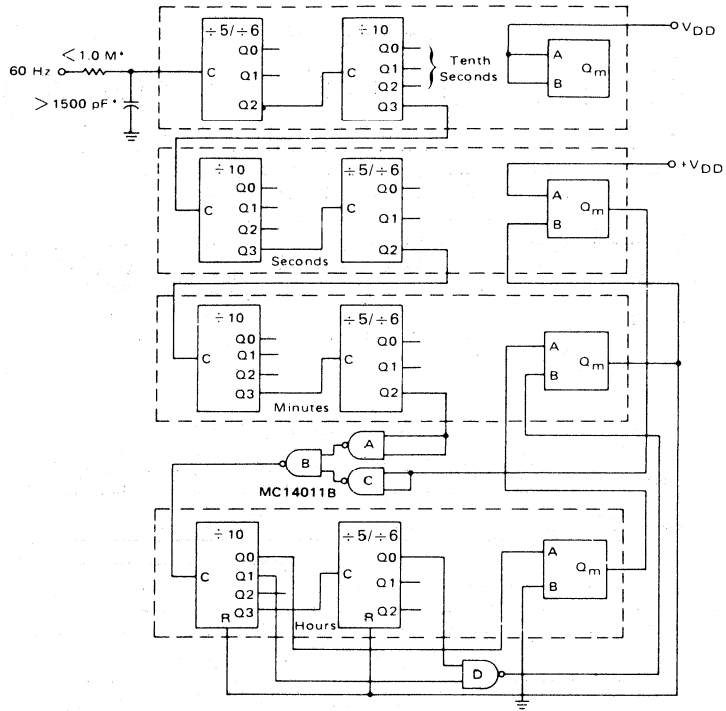
TIMING DIAGRAM



▨ = Don't Care

MC14566B

APPLICATION - 12 HOUR CLOCK



÷5/÷6 Control not shown = V_{SS}
 Reset pins not shown = V_{SS}

*Care must be taken in the indicated circuit to filter line transients which may cause "false" counting.



MOTOROLA

MC14568B

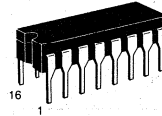
PHASE COMPARATOR AND PROGRAMMABLE COUNTERS

The MC14568B consists of a phase comparator, a divide-by-4, 16, 64 or 100 counter and a programmable divide-by-N 4-bit binary counter (all positive-edge triggered) constructed with MOS P-channel and N-channel enhancement mode devices (complementary MOS) in a monolithic structure.

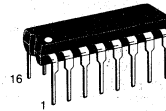
The MC14568B has been designed for use in conjunction with a programmable divide-by-N counter for frequency synthesizers and phase-locked loop applications requiring low power dissipation and/or high noise immunity.

This device can be used with both counters cascaded and the output of the second counter connected to the phase comparator (CTL high), or used independently of the programmable divide-by-N counter, for example cascaded with a MC14569B, MC14522B or MC14526B (CTL low).

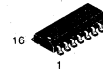
- Supply Voltage Range = 3.0 to 18 V
- Capable of Driving Two Low-Power TTL Loads, One Low-Power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range.
- Chip Complexity: 549 FETs or 137 Equivalent Gates



L SUFFIX
CERAMIC
CASE 620



P SUFFIX
PLASTIC
CASE 648



D SUFFIX
SOIC
CASE 751B

MAXIMUM RATINGS* (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V _{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V _{in}	-0.5 to V _{DD} +0.5	Vdc
DC Input Current, per Pin	I _{in}	±10	mAdc
Power Dissipation, per Package†	P _D	500	mW
Operating Temperature Range	T _A	-55 to +125	°C
Storage Temperature Range	T _{stg}	-65 to +150	°C

*Maximum Ratings are those values beyond which damage to the device may occur.

†Temperature Derating: Plastic "P and D/DW" Packages: -7.0 mW/°C From 65°C To 125°C
Ceramic "L" Packages: -12 mW/°C From 100°C To 125°C

ORDERING INFORMATION

MC14XXXBCP Plastic
MC14XXXBCL Ceramic
MC14XXXBD SOIC

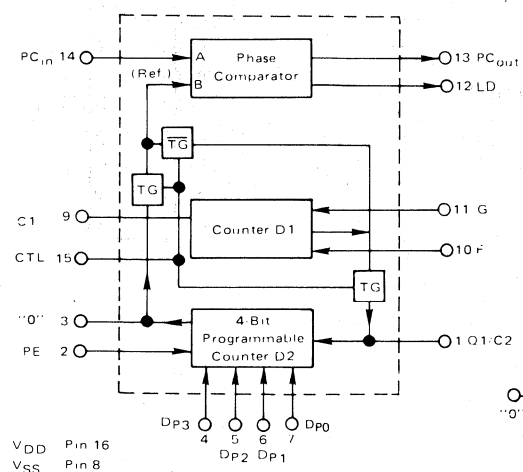
T_A = -55° to 125°C for all packages.

TRUTH TABLE

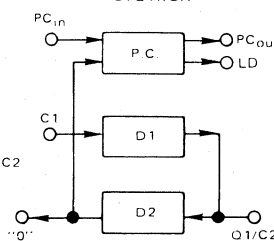
F Pin 10	G Pin 11	Division Ratio of Counter D1
0	0	4
0	1	16
1	0	64
1	1	100

The divide-by-zero state on the programmable divide-by-N 4-bit binary counter, D2, is illegal.

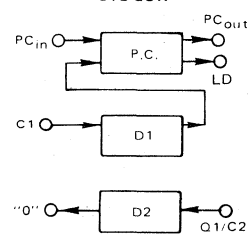
BLOCK DIAGRAM



CTL HIGH



CTL LOW



MC14568B

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V _{DD} Vdc	-55°C		25°C			125°C		Unit	
			Min	Max	Min	Typ #	Max	Min	Max		
Output Voltage V _{in} = V _{DD} or 0 V _{in} = 0 or V _{DD}	"0" Level VOL	5.0	—	0.05	—	0	0.05	—	0.05	Vdc	
		10	—	0.05	—	0	0.05	—	0.05		
		15	—	0.05	—	0	0.05	—	0.05		
	"1" Level VOH	5.0	4.95	—	4.95	5.0	—	4.95	—		
		10	9.95	—	9.95	10	—	9.95	—		
		15	14.95	—	14.95	15	—	14.95	—		
Input Voltage ‡ (V _O = 4.5 or 0.5 Vdc) (V _O = 9.0 or 1.0 Vdc) (V _O = 13.5 or 1.5 Vdc) (V _O = 0.5 or 4.5 Vdc) (V _O = 1.0 or 9.0 Vdc) (V _O = 1.5 or 13.5 Vdc)	"0" Level V _{IL}	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc	
		10	—	3.0	—	4.50	3.0	—	3.0		
		15	—	4.0	—	6.75	4.0	—	4.0		
	"1" Level V _{IH}	5.0	3.5	—	3.5	2.75	—	3.5	—		
		10	7.0	—	7.0	5.50	—	7.0	—		
		15	11	—	11	8.25	—	11	—		
Output Drive Current (V _{OH} = 2.5 Vdc) (V _{OH} = 4.6 Vdc) (V _{OH} = 9.5 Vdc) (V _{OH} = 13.5 Vdc) (V _{OL} = 0.4 Vdc) (V _{OL} = 0.5 Vdc) (V _{OL} = 1.5 Vdc)	Source I _{OH}	5.0	-1.2	—	-1.0	-1.7	—	-0.7	—	mAdc	
		5.0	-0.25	—	-0.2	-0.36	—	-0.14	—		
		10	-1.62	—	-0.5	-0.9	—	-0.35	—		
	Sink I _{OL}	5.0	0.64	—	0.51	0.88	—	0.36	—		
		10	1.6	—	1.3	2.25	—	0.9	—		
		15	4.2	—	3.4	8.8	—	2.4	—		
Input Current	I _{in}	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	μAdc	
Input Capacitance	C _{in}	—	—	—	—	5.0	7.5	—	—	pF	
Quiescent Current (Per Package) V _{in} = 0 or V _{DD} , I _{out} = 0 μA	I _{DD}	5.0	—	5.0	—	0.005	5.0	—	150	μAdc	
		10	—	10	—	0.010	10	—	300		
		15	—	20	—	0.015	20	—	600		
		Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C _L = 50 pF on all outputs, all buffers switching)	I _T	5.0	I _T = (0.2 μA/kHz) f + I _{DD} I _T = (0.4 μA/kHz) f + I _{DD} I _T = (0.9 μA/kHz) f + I _{DD}						—
		10							—	—	
		15							—	—	
		Three-State Leakage Current Pins 1, 13	I _{TL}	15	—	±0.1	—	±0.00001	±0.1	—	±3.0

#Noise immunity specified for worst-case input combination.

Noise Margin for both "1" and "0" level = 1.0 V min (α V_{DD} = 5.0 V)
2.0 V min (α V_{DD} = 10 V)
2.5 V min (α V_{DD} = 15 V)

†To calculate total supply current at loads other than 50 pF:

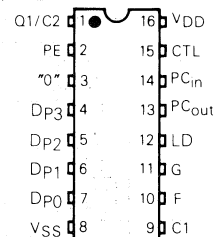
$$I_T(C_L) = I_T(50 \text{ pF}) + 1 \times 10^{-3} (C_L - 50) V_{DD} f$$

where: I_T is in μA (per package), C_L in pF, V_{DD} in V, and f in kHz is input frequency.

**The formulas given are for the typical characteristics only at 25°C.

‡Pin 15 is connected to V_{SS} or V_{DD} for input voltage test.

PIN ASSIGNMENT



MC14568B

SWITCHING CHARACTERISTICS (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V _{DD} V	Min	Typ	Max	Unit
Output Rise Time	t _{TLH}	5.0	—	180	360	ns
		10	—	90	180	
		15	—	65	130	
Output Fall Time	t _{THL}	5.0	—	100	200	ns
		10	—	50	100	
		15	—	40	80	
Minimum Pulse Width, C ₁ , Q1/C2, or PC _{in} Input	t _{WH}	5.0	—	125	250	ns
		10	—	60	120	
		15	—	45	90	
Maximum Clock Rise and Fall Time, C ₁ , Q1/C2, or PC _{in} Input	t _{TLH}	5.0	15	—	—	μs
	t _{THL}	10	15	—	—	
		15	15	—	—	

PHASE COMPARATOR

Input Resistance	R _{in}	5.0 to 15	—	10 ⁶	—	MΩ
Input Sensitivity, dc Coupled	—	5.0 to 15	See Input Voltage			
Turn-Off Delay Time, PC _{out} and LD Outputs	t _{PHL}	5.0	—	550	1100	ns
		10	—	195	390	
		15	—	120	240	
Turn-On Delay Time, PC _{out} and LD Outputs	t _{PLH}	5.0	—	675	1350	ns
		10	—	300	600	
		15	—	190	380	

DIVIDE-BY-4, 16, 64 OR 100 COUNTER (D1)

Maximum Clock Pulse Frequency Division Ratio = 4, 64 or 100	f _{cl}	5.0	3.0	6.0	—	MHz
		10	8.0	16	—	
		15	10	22	—	
		5.0	1.0	2.5	—	
		10	3.0	6.3	—	
		15	5.0	9.7	—	
Propagation Delay Time, Q1/C2 Output Division Ratio = 4, 64 or 100	t _{PLH} , t _{PHL}	5.0	—	450	900	ns
		10	—	190	380	
		15	—	130	260	
		5.0	—	720	1440	
		10	—	300	600	
		15	—	200	400	

PROGRAMMABLE DIVIDE-BY-N 4-BIT COUNTER (D2)

Maximum Clock Pulse Frequency (Figure 3a)	f _{cl}	5.0	1.2	1.8	—	MHz
		10	3.0	8.5	—	
		15	4.0	12	—	
Turn-On Delay Time, "0" Output (Figure 3a)	t _{PLH}	5.0	—	450	900	ns
		10	—	190	380	
		15	—	130	260	
Turn-Off Delay Time, "0" Output (Figure 3a)	t _{PHL}	5.0	—	225	450	ns
		10	—	85	170	
		15	—	60	150	
Minimum Preset Enable Pulse Width	t _{WH(PE)}	5.0	—	75	250	ns
		10	—	40	100	
		15	—	30	75	

MC14568B

SWITCHING TIME TEST CIRCUITS AND WAVEFORMS

FIGURE 1 - PHASE COMPARATOR

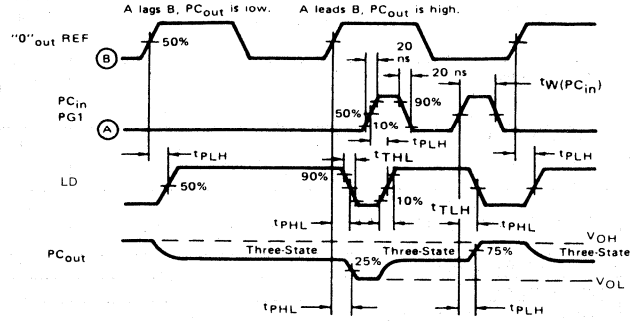
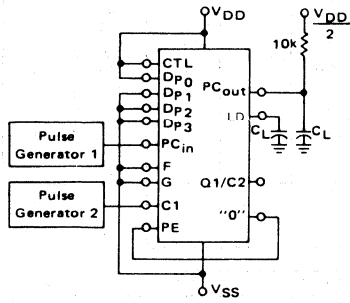


FIGURE 2 - COUNTER D1

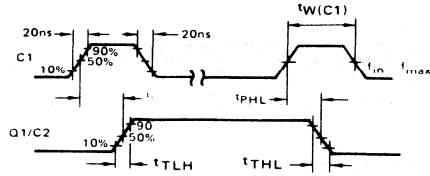
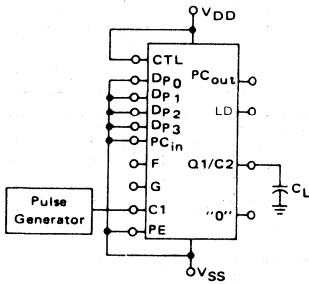
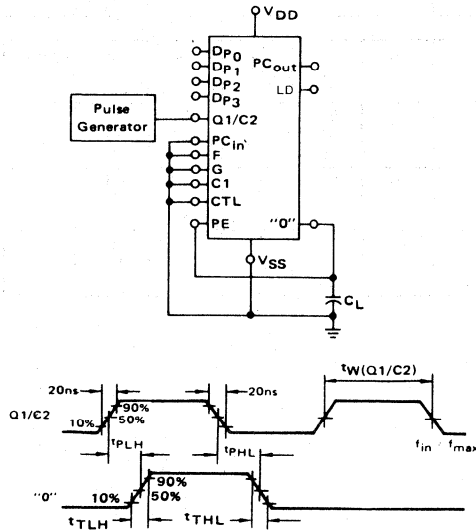
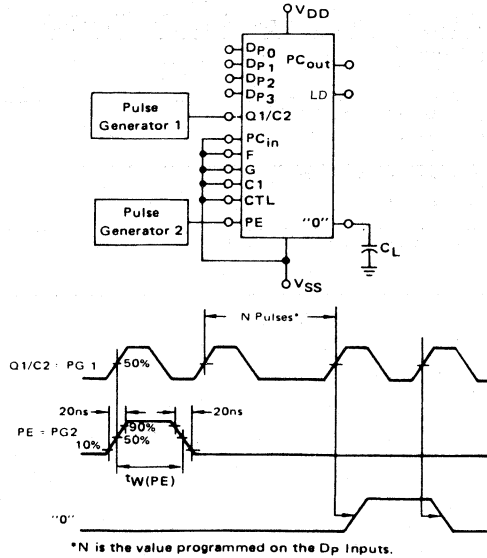


FIGURE 3 - COUNTER D2

a.

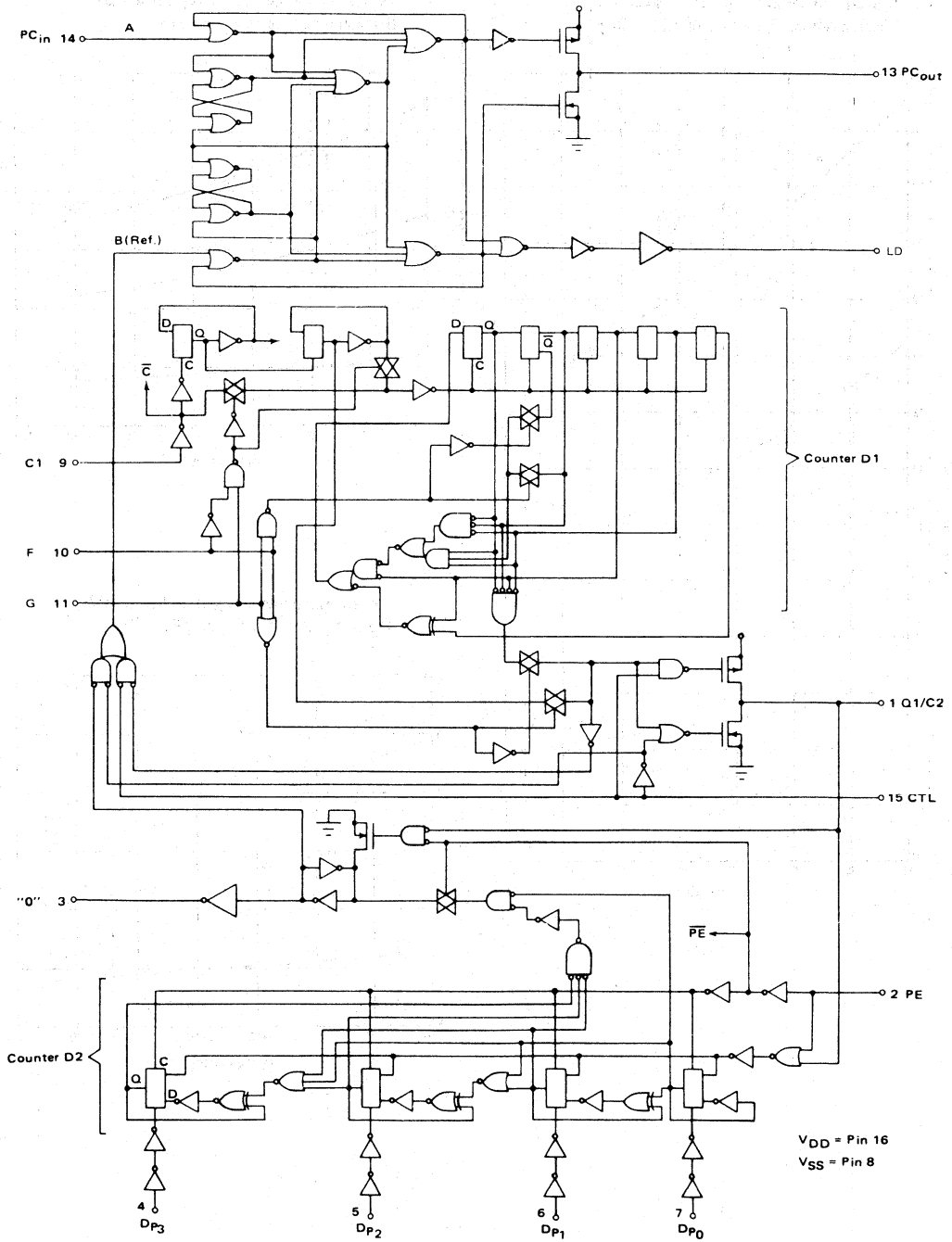


b.



MC14568B

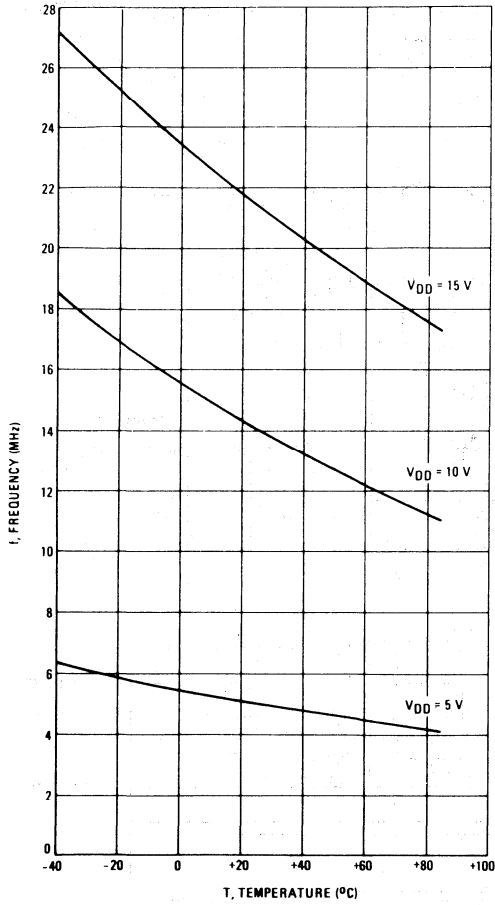
LOGIC DIAGRAM



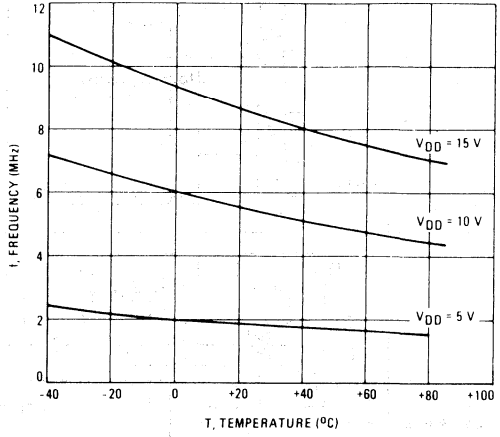
6

MC14568B

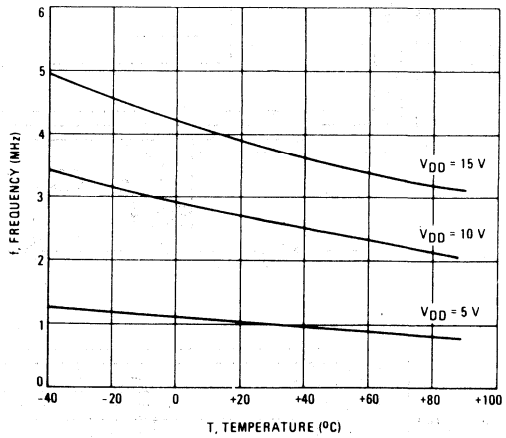
Typical Maximum Frequency Divider D1
Division ratios: 4, 64 or 100 (CL = 50 pF)



Typical Maximum Frequency Divider D1
Division ratio: 16 (CL = 50 pF)



Typical Maximum Frequency Divider D2
Division ratio: 2 (CL = 50 pF)



MC14568B

OPERATING CHARACTERISTICS

The MC14568B contains a phase comparator, a fixed divider ($\div 4$, $\div 16$, $\div 64$, $\div 100$) and a programmable divide-by-N 4-bit counter.

PHASE COMPARATOR

The phase comparator is a positive edge controlled logic circuit. It essentially consists of four flip-flops and an output pair of MOS transistors. Only one of its inputs (PC_{in} , pin 14) is accessible externally. The second is connected to the output of one of the two counters D1 or D2 (see block diagram).

Duty cycles of both input signals (at A and B) need not be taken into consideration since the comparator responds to leading edges only.

If both input signals have identical frequencies but different phases, with signal A (pin 14) leading signal B (Ref.), the comparator output will be high for the time equal to the phase difference.

If signal A lags signal B, the output will be low for the same time. In between, the output will be in a three-state condition and the voltage on the capacitor of an RC filter normally connected at this point will have some intermediate value (see Figure 4). When used in a phase locked loop, this value will adjust the Voltage Controlled Oscillator frequency by reducing the phase difference between the reference signal and the divided VCO frequency to zero.

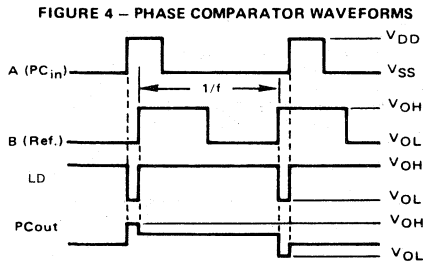
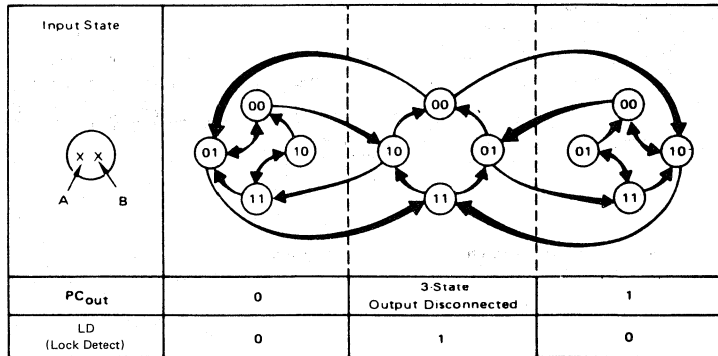


FIGURE 5 – PHASE COMPARATOR STATE DIAGRAM



If the input signals have different frequencies, the output signal will be high when signal B has a lower frequency than signal A, and low otherwise.

Under the same conditions of frequency difference, the output will vary between V_{OH} (or V_{OL}) and some intermediate value until the frequencies of both signals are equal and their phase difference equal to zero, i.e. until locked condition is obtained.

Capture and lock range will be determined by the VCO frequency range. The comparator is provided with a lock indicator output, which will stay at logic 1 in locked conditions.

The state diagram (Figure 5) depicts the internal state transitions. It assumes that only one transition on either signal occurs at any time. It shows that a change of the output state is always associated with a positive transition of either signal. For a negative transition, the output does not change state. A positive transition may not cause the output to change; this happens when the signals have different frequencies.

DIVIDE BY 4, 16, 64 OR 100 COUNTER (D1)

This counter is able to work at an input frequency of 5 MHz for a V_{DD} value of 10 volts over the standard temperature range when dividing by 4, 64 and 100. Programming is accomplished by use of inputs F and G (pins 10 and 11) according to the truth table shown. Connecting the Control input (CTL, pin 15) to V_{DD} allows cascading this counter with the programmable divide-by-N counter provided in the same package. Independent operation is obtained when the Control input is connected to V_{SS} .

The different division ratios have been chosen to generate the reference frequencies corresponding to the channel spacings normally required in frequency synthesizer applications. For example, with the division ratio 100 and a 5 MHz crystal stabilized source a reference frequency of 50 kHz is supplied to the comparator. The lower division ratios permit operation with low frequency crystals.

MC14568B

If used in cascade with the programmable divide-by-N counter, practically all usual reference frequencies, or channel spacings of 25, 20, 12.5, 10, 6.25 kHz, etc. are easily achievable.

PROGRAMMABLE DIVIDE-BY-N 4-BIT COUNTER (D2)

This counter is programmable by using inputs $D_{P0} \dots$

D_{P3} (pins 7 ... 4). The Preset Enable input enables the parallel preset inputs $D_{P0} \dots D_{P3}$. The "0" output must be externally connected to the PE input for single stage applications. Since there is not a cascade feedback input, this counter, when cascaded, must be used as the most significant digit. Because of this, it can be cascaded with binary counters as well as with BCD counters (MC14569B, MC14522B, MC14526B).

TYPICAL APPLICATIONS

FIGURE 6 – CASCADING MC14568B AND MC14522B OR MC14526B WITH MC14569B

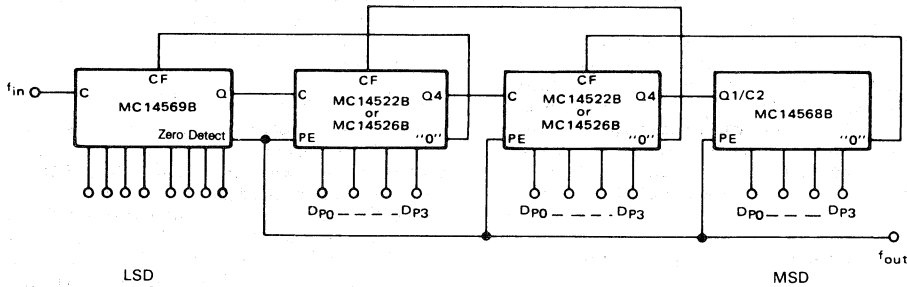
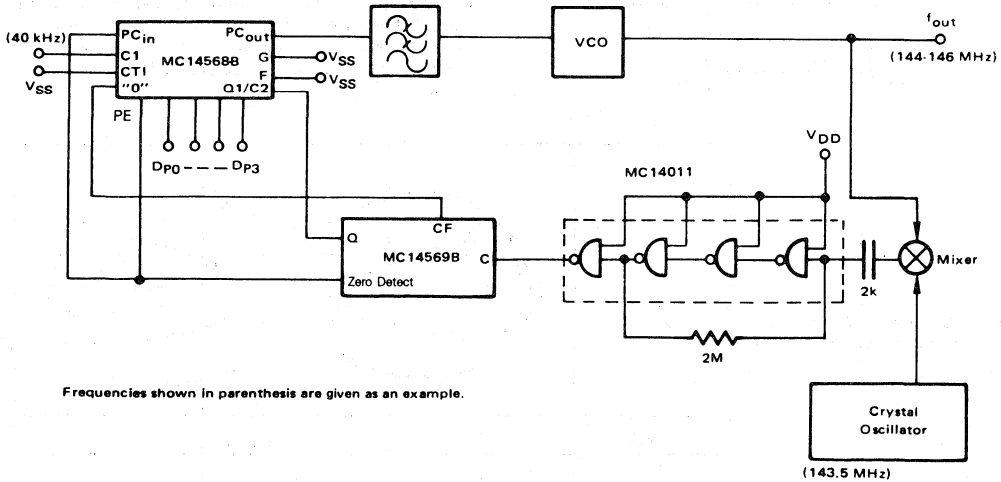


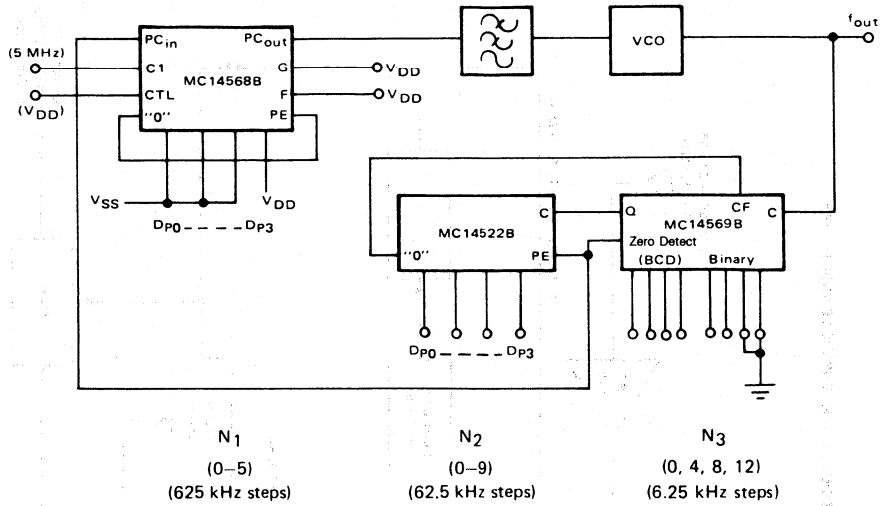
FIGURE 7 – FREQUENCY SYNTHESIZER WITH MC14568B and MC14569B USING A MIXER
(Channel Spacing 10 kHz)



Frequencies shown in parenthesis are given as an example.

MC14568B

FIGURE 8 – FREQUENCY SYNTHESIZER USING MC14568B, MC14569B AND MC14522B
(Without Mixer)



$$\text{Divide ratio} = 160N_1 + 16N_2 + N_3$$

Example:

$$f_{out} = N_1 \text{ (MHz)} + N_2 \text{ (x100 kHz)} + N_3 \text{ (x25 kHz)}$$

Frequency range = 5 MHz

Channel spacing = 25 kHz

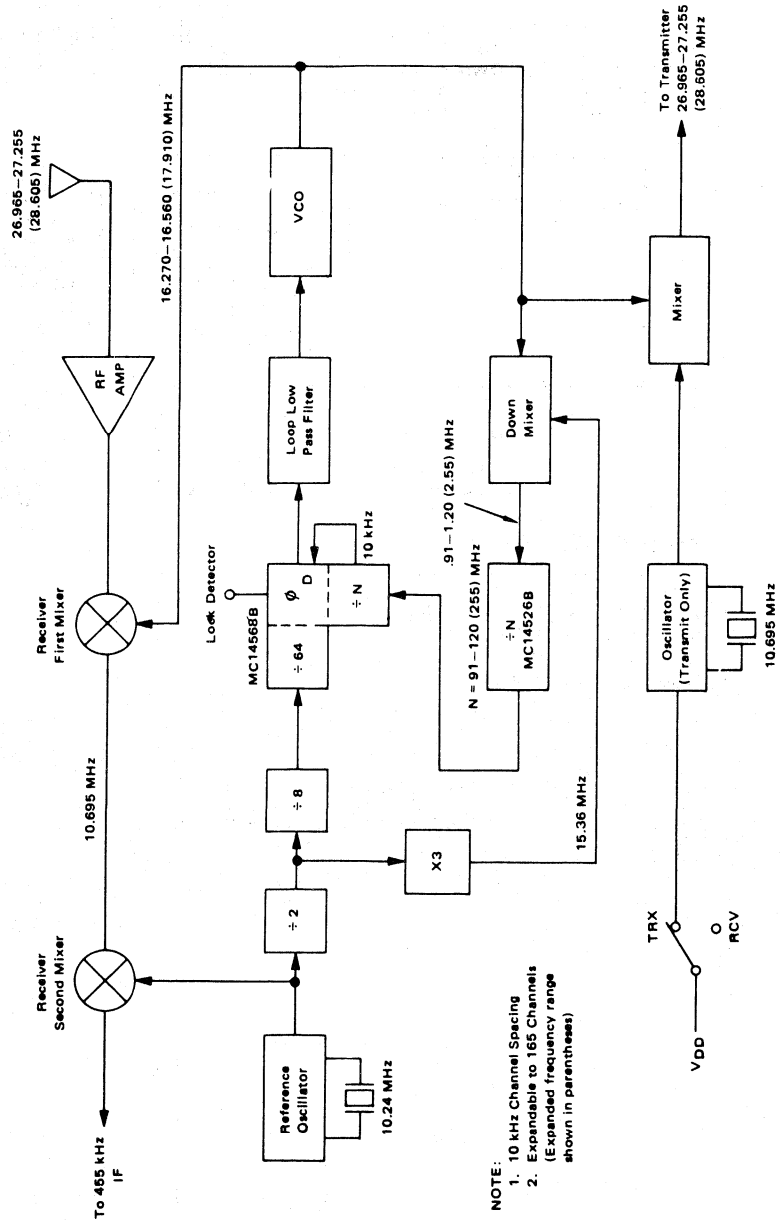
Reference frequency = 6.25 kHz

Figures shown in parenthesis refer to example.

Recommended reading:

- (1) AN535: "Phase-Lock Techniques"
- (2) AR254: "Phase-Locked Loop Design Articles"

FIGURE 9 - TYPICAL 23-CHANNEL CB FREQUENCY SYNTHESIZER FOR DOUBLE CONVERSION TRANSCEIVERS



6



MOTOROLA

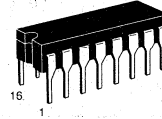
MC14569B

PROGRAMMABLE DIVIDE-BY-N DUAL 4-BIT BINARY/BCD DOWN COUNTER

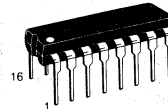
The MC14569B is a programmable divide-by-N dual 4-bit binary or BCD down counter constructed with MOS P-channel and N-channel enhancement mode devices (complementary MOS) in a monolithic structure.

This device has been designed for use with the MC14568B phase comparator/counter in frequency synthesizers, phase-locked loops, and other frequency division applications requiring low power dissipation and/or high noise immunity.

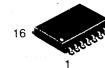
- Speed-up Circuitry for Zero Detection
- Each 4-Bit Counter Can Divide Independently in BCD or Binary Mode
- Can be Cascaded With MC14568B, MC14522B or MC14526B for Frequency Synthesizer Applications
- All Outputs are Buffered
- Schmitt Triggered Clock Conditioning



L SUFFIX
CERAMIC
CASE 620



P SUFFIX
PLASTIC
CASE 648



DW SUFFIX
SOIC
CASE 751G

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V _{DD}	DC Supply Voltage	-0.5 to +18.0	V
V _{in, Vout}	Input or Output Voltage (DC or Transient)	-0.5 to V _{DD} + 0.5	V
I _{in, Iout}	Input or Output Current (DC or Transient), per Pin	± 10	mA
P _D	Power Dissipation, per Package†	500	mW
T _{stg}	Storage Temperature	-65 to +150	°C
T _L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.

†Temperature Derating: Plastic "P and D/DW" Packages: -7.0 mW/°C From 65°C To 125°C

Ceramic "L" Packages: -12 mW/°C From 100°C To 125°C

ORDERING INFORMATION

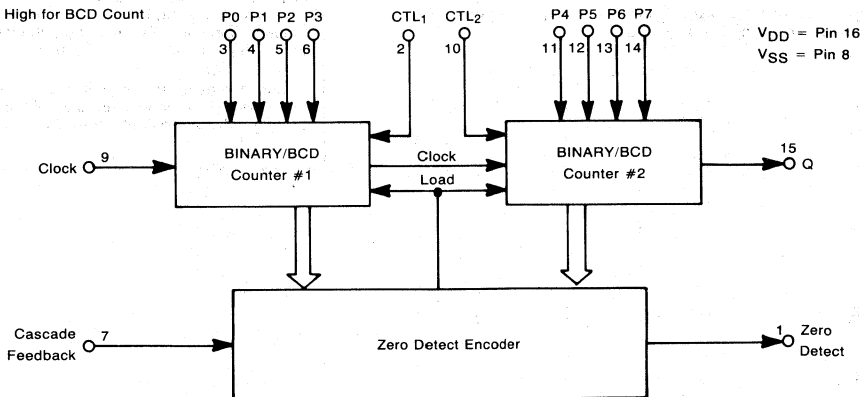
MC14XXXBCP Plastic
MC14XXXBCL Ceramic
MC14XXXBDW SOIC

T_A = -55° to 125°C for all packages.

6

BLOCK DIAGRAM

CTL = Low for Binary Count
CTL = High for BCD Count



MC14569B

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V _{DD} Vdc	-55°C		25°C			125°C		Unit
			Min	Max	Min	Typ #	Max	Min	Max	
Output Voltage V _{in} = V _{DD} or 0 V _{in} = 0 or V _{DD}	"0" Level V _{OL}	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
		10	—	0.05	—	0	0.05	—	0.05	
		15	—	0.05	—	0	0.05	—	0.05	
	"1" Level V _{OH}	5.0	4.95	—	4.95	5.0	—	4.95	—	
		10	9.95	—	9.95	10	—	9.95	—	
		15	14.95	—	14.95	15	—	14.95	—	
Input Voltage (V _O = 4.5 or 0.5 Vdc) (V _O = 9.0 or 1.0 Vdc) (V _O = 13.5 or 1.5 Vdc) (V _O = 0.5 or 4.5 Vdc) (V _O = 1.0 or 9.0 Vdc) (V _O = 1.5 or 13.5 Vdc)	"0" Level V _{IL}	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc
		10	—	3.0	—	4.50	3.0	—	3.0	
		15	—	4.0	—	6.75	4.0	—	4.0	
	"1" Level V _{IH}	5.0	3.5	—	3.5	2.75	—	3.5	—	
		10	7.0	—	7.0	5.50	—	7.0	—	
		15	11	—	11	8.25	—	11	—	
Output Drive Current (V _{OH} = 2.5 Vdc) (V _{OH} = 4.6 Vdc) (V _{OH} = 9.5 Vdc) (V _{OH} = 13.5 Vdc) (V _{OL} = 0.4 Vdc) (V _{OL} = 0.5 Vdc) (V _{OL} = 1.5 Vdc)	Source I _{OH}	5.0	-3.0	—	-2.4	-4.2	—	-1.7	—	mAdc
		5.0	-0.64	—	-0.51	-0.88	—	-0.36	—	
		10	-1.6	—	-1.3	-2.25	—	-0.9	—	
	Sink I _{OL}	5.0	0.64	—	0.51	0.88	—	0.36	—	
		10	1.6	—	1.3	2.25	—	0.9	—	
		15	4.2	—	3.4	8.8	—	2.4	—	
Input Current	I _{in}	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	μAdc
Input Capacitance (V _{in} = 0)	C _{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)	I _{DD}	5.0	—	5.0	—	0.005	5.0	—	150	μAdc
		10	—	10	—	0.010	10	—	300	
		15	—	20	—	0.015	20	—	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C _L = 50 pF on all outputs, all buffers switching)	I _T	5.0	I _T = (0.58 μA/kHz) f + I _{DD}							μAdc
		10	I _T = (1.20 μA/kHz) f + I _{DD}							
		15	I _T = (1.95 μA/kHz) f + I _{DD}							

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) Vfk$$

where: I_T is in μA (per package), C_L in pF, V = (V_{DD} - V_{SS}) in volts, f in kHz is input frequency, and k = 0.001.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range V_{SS} ≤ (V_{in} or V_{out}) ≤ V_{DD}.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

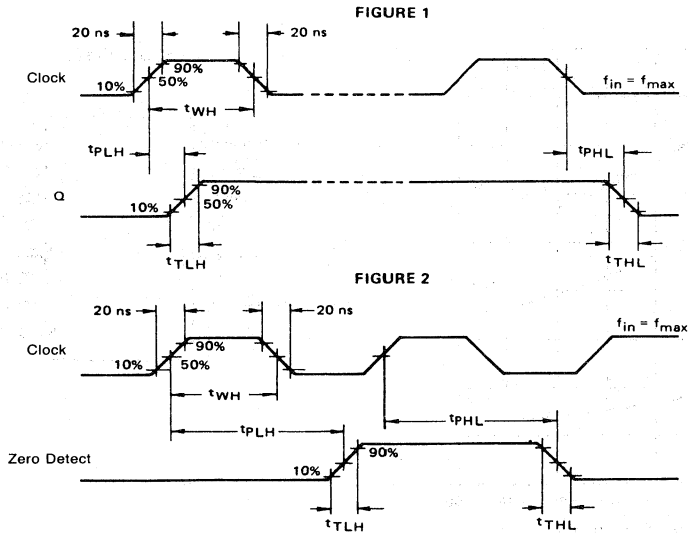
MC14569B

SWITCHING CHARACTERISTICS* ($C_L = 50 \text{ pF}$, $T_A = 25^\circ\text{C}$)

Characteristic	Symbol	VDD Vdc	All Types			Unit
			Min	Typ #	Max	
Output Rise Time	t_{TLH}	5.0	—	100	200	ns
		10	—	50	100	
		15	—	40	80	
Output Fall Time	t_{THL}	5.0	—	100	200	ns
		10	—	50	100	
		15	—	40	80	
Turn-On Delay Time Zero Detect Output	t_{PLH}	5.0	—	420	700	ns
		10	—	175	300	
		15	—	125	250	
Q Output		5.0	—	675	1200	ns
		10	—	285	500	
		15	—	200	400	
Turn-Off Delay Time Zero Detect Output	t_{PHL}	5.0	—	380	600	ns
		10	—	150	300	
		15	—	100	200	
Q Output		5.0	—	530	1000	ns
		10	—	225	400	
		15	—	155	300	
Clock Pulse Width	t_{WH}	5.0	300	100	—	ns
		10	150	45	—	
		15	115	30	—	
Clock Pulse Frequency	f_{cl}	5.0	—	3.5	2.1	MHz
		10	—	9.5	5.7	
		15	—	13.0	7.8	
Clock Pulse Rise and Fall Time	t_{TLH} , t_{THL}	5.0	NO LIMIT			μs
		10				
		15				

*Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

SWITCHING WAVEFORMS



MC14569B

PIN DESCRIPTIONS

INPUTS

P0, P1, P2, P3 (Pins 3, 4, 5, 6) — Preset Inputs. Programmable inputs for the least significant counter. May be binary or BCD depending on the control input.

P4, P5, P6, P7 (Pins 11, 12, 13, 14) — Preset Inputs. Programmable inputs for the most significant counter. May be binary or BCD depending on the control input.

Clock (Pin 9) — Preset data is decremented by one on each positive transition of this signal.

OUTPUTS

Zero Detect (Pin 1) — This output is normally low and goes high for one clock cycle when the counter has decremented to zero.

Q (Pin 15) — Output of the last stage of the most significant counter. This output will be inactive unless the preset input P7 has been set high.

CONTROLS

Cascade Feedback (Pin 7) — This pin is normally set high. When low, loading of the preset inputs (P0 through P7) is inhibited, i.e., P0 through P7 are "don't cares." Refer to Table 1 for output characteristics.

CTL₁ (Pin 2) — This pin controls the counting mode of the least significant counter. When set high, counting mode is BCD. When set low, counting mode is binary.

CTL₂ (Pin 10) — This pin controls the counting mode of the most significant counter. When set high, counting mode is BCD. When set low, counting mode is binary.

SUPPLY PINS

V_{SS} (Pin 18) — Negative Supply Voltage. This pin is usually connected to ground.

V_{DD} (Pin 16) — Positive Supply Voltage. This pin is connected to a positive supply voltage ranging from 3.0 volts to 18.0 volts.

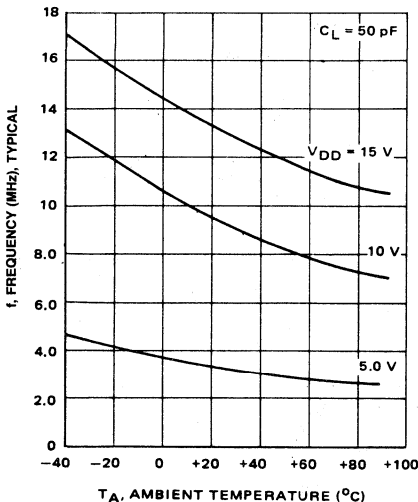
OPERATING CHARACTERISTICS

The MC14569B is a programmable divide-by-N dual 4-bit down counter. This counter may be programmed (i.e., preset) in BCD or binary code through inputs P0 to P7. For each counter, the counting sequence may be chosen independently by applying a high (for BCD count) or a low (for binary count) to the control inputs CTL₁ and CTL₂.

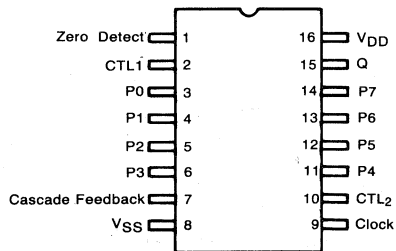
The divide ratio N (N being the value programmed on the preset inputs P0 to P7) is automatically loaded into the counter as soon as the count 1 is detected. Therefore, a division ratio of one is not possible. After N clock

cycles, one pulse appears on the Zero Detect output. (See Timing Diagram.) The Q output is the output of the last stage of the most significant counter (See Tables 1 through 5, Mode Controls.)

When cascading the MC14569B to the MC14568B, MC14522B or the MC14526B, the Cascade Feedback input, Q, and Zero Detect outputs must be respectively connected to "0", Clock, and Load of the following counter. If the MC14569B is used alone, Cascade Feedback must be connected to V_{DD}.



PIN ASSIGNMENT



MC14569B

TABLE 1 — MODE CONTROLS (Cascade Feedback = Low)

Counter Control Values		Divide Ratio	
CTL ₁	CTL ₂	Zero Detect	Q
0	0	256	256
0	1	160	160
1	0	160	160
1	1	100	100

Note: Data Preset Inputs (P0-P7) are "Don't Cares" while Cascade Feedback is Low.

TABLE 2 — MODE CONTROLS (CTL₁ = Low, CTL₂ = Low, Cascade Feedback = High)

Preset Inputs								Divide Ratio		Comments
P7	P6	P5	P4	P3	P2	P1	P0	Zero Detect	Q	
0	0	0	0	0	0	0	0	256	256	Max Count Illegal State Min Count
0	0	0	0	0	0	0	1	X	X	
0	0	0	0	0	0	1	0	2	X	
0	0	0	0	0	0	1	1	3	X	
.	X	
.	X	
0	0	0	0	1	1	1	1	15	X	
0	0	0	1	0	0	0	0	16	X	
.	X	
.	X	
0	0	1	0	0	0	0	0	32	X	
.	X	
.	X	
0	1	0	0	0	0	0	0	64	X	
.	X	
.	X	
0	1	1	1	1	1	1	1	127	X	
1	0	0	0	0	0	0	0	128	128	
.	
.	
1	0	0	0	1	0	0	0	136	136	
.	
.	
1	1	1	1	1	1	1	1	255	255	
2 ⁷ 128	2 ⁶ 64	2 ⁵ 32	2 ⁴ 16	2 ³ 8	2 ² 4	2 ¹ 2	2 ⁰ 1			Bit Value
Counter #2 Binary				Counter #1 Binary						Counting Sequence

X = No Output (Always Low)

6

MC14569B

TABLE 4 — MODE CONTROLS (CTL₁ = Low, CTL₂ = High, Cascade Feedback = High)

Preset Values								Divide Ratio		Comments	
P7	P6	P5	P4	P3	P2	P1	P0	Zero Detect	Q		
0	0	0	0	0	0	0	0	160	160	Max Count Illegal State Min Count	
0	0	0	0	0	0	0	1	X	X		
0	0	0	0	0	0	1	0	2	X		
0	0	0	0	0	0	1	1	3	X		
.	X		
.	X		
.	X		
0	0	0	0	1	1	1	1	15	X		
0	0	0	1	0	0	0	0	16	X		
.	X		
.	X		
0	0	0	1	1	1	1	1	31	X		
0	0	1	0	0	0	0	0	32	X		
.	X		
.	X		
0	0	1	1	0	0	0	0	48	X		
.		
.		
0	1	0	0	0	0	0	0	64	X		
.		
.		
0	1	0	1	0	0	0	0	80	X		
.		
.		
0	1	1	1	0	0	0	0	112	X		
.		
.		
1	0	0	0	0	0	0	0	128	128	Q Output Active ↓	
.		
.		
1	0	0	1	0	0	0	0	144	144		
.		
.		
1	0	0	1	1	1	1	1	159	159		
2 ⁷	2 ⁶	2 ⁵	2 ⁴	2 ³	2 ²	2 ¹	2 ⁰				Bit Value
128	64	32	16	8	4	2	1				Counting Sequence
Counter #2 BCD			Counter #1 Binary								

X = No Output (Always Low)

MC14569B

TABLE 5 — MODE CONTROLS (CTL₁ = High, CTL₂ = High, Cascade Feedback = High)

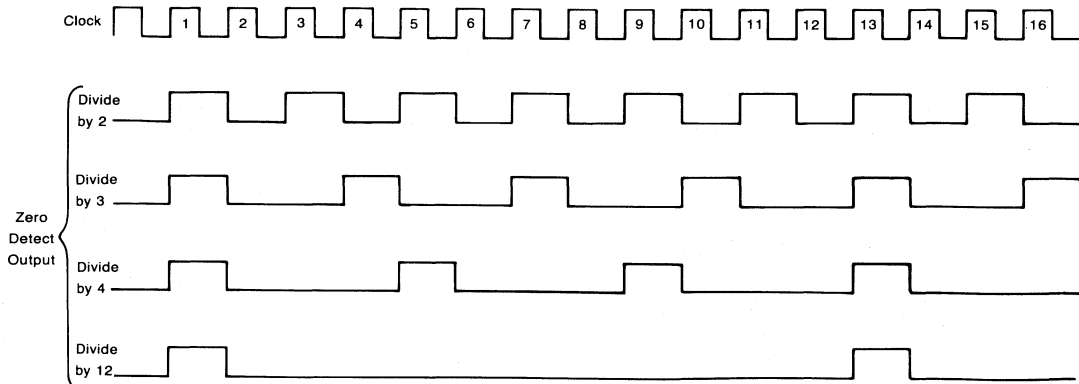
Preset Values								Divide Ratio		Comments	
P7	P6	P5	P4	P3	P2	P1	P0	Zero Detect	Q		
0	0	0	0	0	0	0	0	100	100	Max Count Illegal State Min Count	
0	0	0	0	0	0	0	1	X	X		
0	0	0	0	0	0	0	1	2	X		
0	0	0	0	0	0	1	1	3	X		
.	X		
.	X		
0	0	0	0	1	0	0	1	9	X		
0	0	0	1	0	0	0	0	10	X		
.	X		
.	X		
0	0	1	1	0	0	0	0	30	X		
.	X		
.	X		
0	1	0	0	0	0	0	0	40	X		
.	X		
.	X		
0	1	0	1	0	0	0	0	50	X		
.	X		
.	X		
0	1	1	1	0	0	0	0	70	X		
.	X		
.	X		
1	0	0	0	0	0	0	0	80	80		
.		
.		
1	0	0	1	0	0	0	0	90	90		
.		
.		
1	0	0	1	1	0	0	1	99	99		
80	40	20	10	8	4	2	1			Bit Value	
Counter #2 BCD				Counter #1 BCD							Counting Sequence

X = No Output (Always Low)

Q Output Active

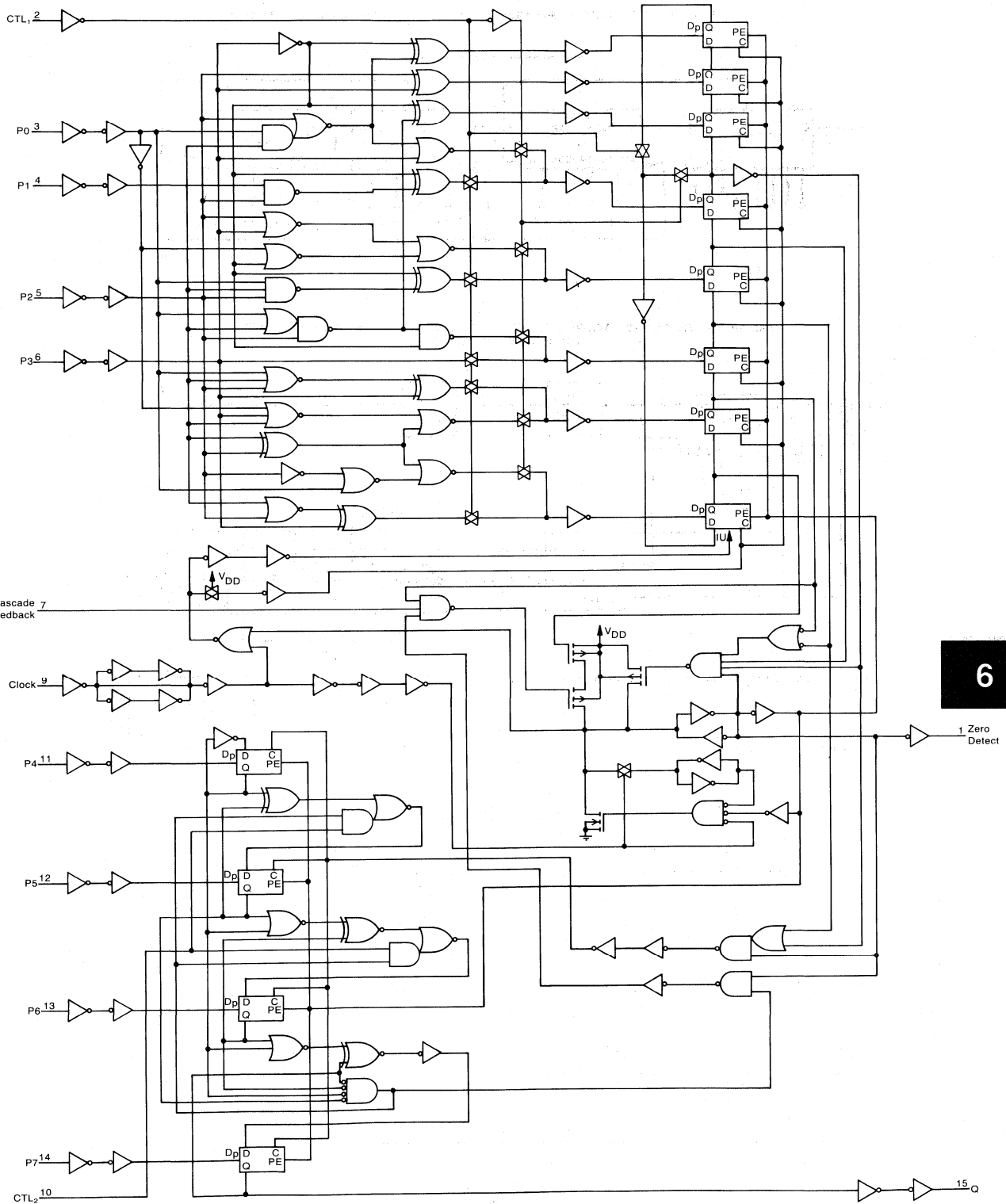


TIMING DIAGRAM MC14569B



MC14569B

LOGIC DIAGRAM



6

1 Zero Detect

15_Q

MC14569B

TYPICAL APPLICATIONS

FIGURE 6 — CASCADING MC14568B AND MC14522B OR MC14526B WITH MC14569B

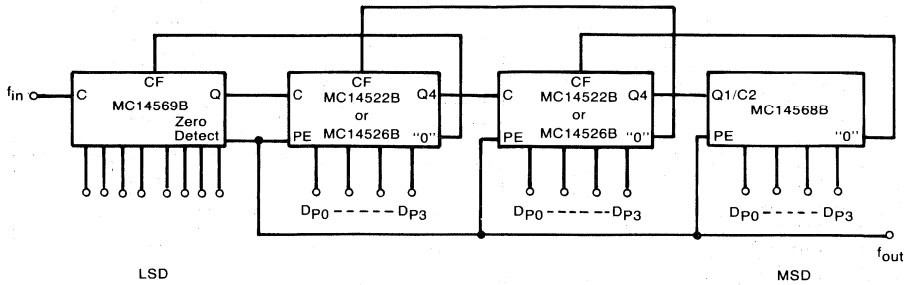
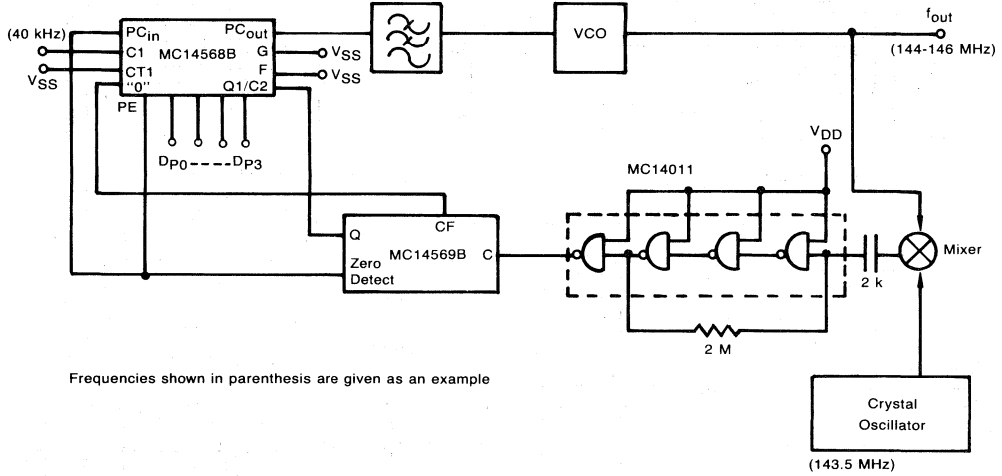


FIGURE 7 — FREQUENCY SYNTHESIZER WITH MC14568B and MC14569B USING A MIXER
(Channel Spacing 10 kHz)



Frequencies shown in parenthesis are given as an example



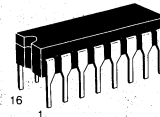
MOTOROLA

MC14572UB

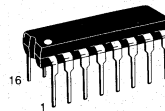
HEX GATE

The MC14572UB hex functional gate is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These complementary MOS logic gates find primary use where low power dissipation and/or high noise immunity is desired. The chip contains four inverters, one NOR gate and one NAND gate.

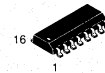
- Diode Protection on All Inputs
- Single Supply Operation
- Supply Voltage Range = 3.0 Vdc to 18.Vdc
- NOR Input Pin Adjacent to V_{SS} Pin to Simplify Use As An Inverter
- NAND Input Pin Adjacent to V_{DD} Pin to Simplify Use As An Inverter
- NOR Output Pin Adjacent to Inverter Input Pin For OR Application
- NAND Output Pin Adjacent to Inverter Input Pin For AND Application
- Capable of Driving Two Low-power TTL Loads or One Low-Power Schottky TTL Load over the Rated Temperature Range



L SUFFIX
CERAMIC
CASE 620



P SUFFIX
PLASTIC
CASE 648



D SUFFIX
SOIC
CASE 751B

ORDERING INFORMATION

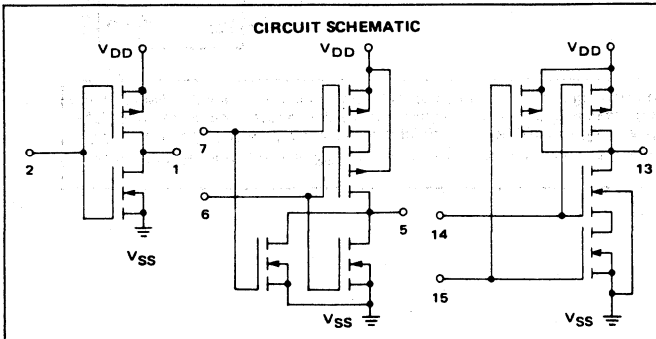
MC14XXXUBCP Plastic
MC14XXXUBCL Ceramic
MC14XXXUBD SOIC
T_A = -55° to 125°C for all packages.

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

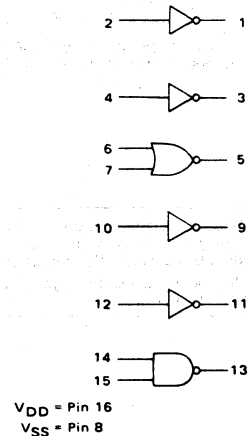
Symbol	Parameter	Value	Unit
V _{DD}	DC Supply Voltage	-0.5 to +18.0	V
V _{in} , V _{out}	Input or Output Voltage (DC or Transient)	-0.5 to V _{DD} + 0.5	V
I _{in} , I _{out}	Input or Output Current (DC or Transient), per Pin	± 10	mA
P _D	Power Dissipation, per Package†	500	mW
T _{stg}	Storage Temperature	-65 to +150	°C
T _L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P" and D/DW" Packages: -7.0 mW/°C From 65°C To 125°C
Ceramic "L" Packages: -12 mW/°C From 100°C To 125°C

CIRCUIT SCHEMATIC



LOGIC DIAGRAM



6

MC14572UB

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V _{DD} Vdc	-55°C		25°C			125°C		Unit
			Min	Max	Min	Typ #	Max	Min	Max	
Output Voltage V _{in} = V _{DD} or 0	V _{OL}	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
		10	—	0.05	—	0	0.05	—	0.05	
V _{in} = 0 or V _{DD}	V _{OH}	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc
		10	9.95	—	9.95	10	—	9.95	—	
Input Voltage (V _O = 4.5 or 0.5 Vdc) (V _O = 9.0 or 1.0 Vdc) (V _O = 13.5 or 1.5 Vdc)	V _{IL}	5.0	—	1.0	—	2.25	1.0	—	1.0	Vdc
		10	—	2.0	—	4.50	2.0	—	2.0	
(V _O = 0.5 or 4.5 Vdc) (V _O = 1.0 or 9.0 Vdc) (V _O = 1.5 or 13.5 Vdc)	V _{IH}	5.0	4.0	—	4.0	2.75	—	4.0	—	Vdc
		10	8.0	—	8.0	5.50	—	8.0	—	
Output Drive Current (V _{OH} = 2.5 Vdc) (V _{OH} = 4.6 Vdc) (V _{OH} = 9.5 Vdc) (V _{OH} = 13.5 Vdc)	Source I _{OH}	5.0	-1.2	—	-1.0	-1.7	—	-0.7	—	mA _{dc}
		5.0	-0.25	—	-0.2	-0.36	—	-0.14	—	
(V _{OL} = 0.4 Vdc) (V _{OL} = 0.5 Vdc) (V _{OL} = 1.5 Vdc)	Sink I _{OL}	5.0	0.64	—	0.51	0.88	—	0.36	—	mA _{dc}
		10	1.6	—	1.3	2.25	—	0.9	—	
		15	4.2	—	3.4	8.8	—	2.4	—	
Input Current	I _{in}	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	μA _{dc}
Input Capacitance (V _{in} = 0)	C _{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)	I _{DD}	5.0	—	0.25	—	0.0005	0.25	—	7.5	μA _{dc}
		10	—	0.5	—	0.0010	0.5	—	15	
		15	—	1.0	—	0.0015	1.0	—	30	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C _L = 50 pF on all outputs, all buffers switching)	I _T	5.0	I _T = (1.89 μA/kHz) f + I _{DD}							μA _{dc}
		10	I _T = (3.80 μA/kHz) f + I _{DD}							
		15	I _T = (5.68 μA/kHz) f + I _{DD}							

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

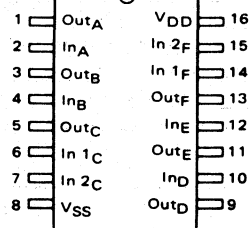
**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) V f k$$

where: I_T is in μA (per package), C_L in pF, V = (V_{DD} - V_{SS}) in volts, f in kHz is input frequency, and k = 0.006.

PIN ASSIGNMENT



This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range V_{SS} ≤ (V_{in} or V_{out}) ≤ V_{DD}. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

MC14572UB

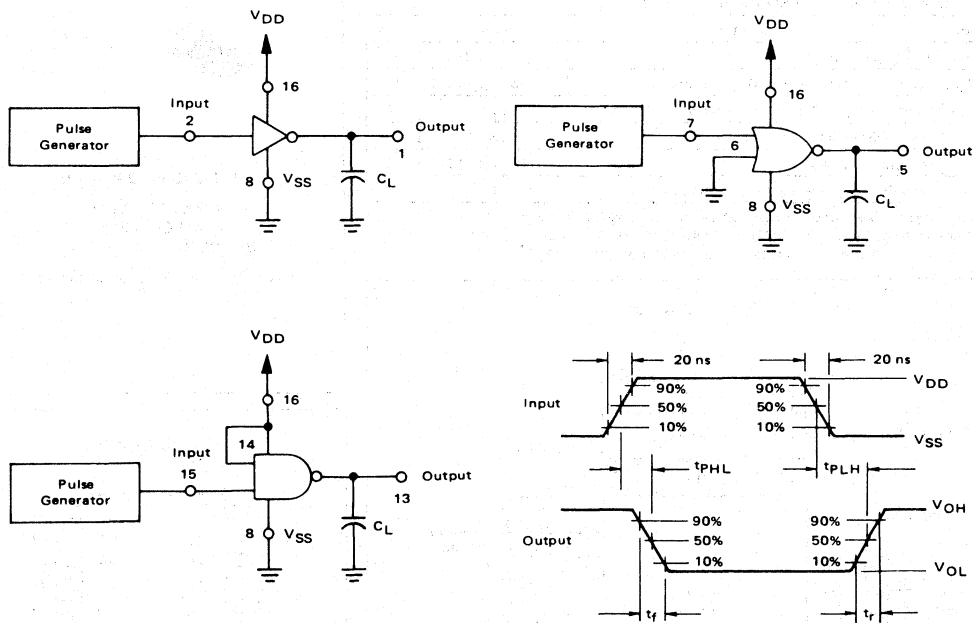
SWITCHING CHARACTERISTICS* ($C_L = 50 \text{ pF}$, $T_A = 25^\circ\text{C}$)

Characteristic	Symbol	V _{DD}	Min	Typ #	Max	Unit
Output Rise Time	t_{TLH}	5.0 10 15	— — —	180 90 65	360 180 130	ns
$t_{TLH} = (3.0 \text{ ns/pF}) C_L + 30 \text{ ns}$						
$t_{TLH} = (1.5 \text{ ns/pF}) C_L + 15 \text{ ns}$						
$t_{TLH} = (1.1 \text{ ns/pF}) C_L + 10 \text{ ns}$						
Output Fall Time	t_{THL}	5.0 10 15	— — —	100 50 40	200 100 80	ns
$t_{THL} = (1.5 \text{ ns/pF}) C_L + 25 \text{ ns}$						
$t_{THL} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$						
$t_{THL} = (0.55 \text{ ns/pF}) C_L + 9.5 \text{ ns}$						
Propagation Delay Time	t_{PLH} , t_{PHL}	5.0 10 15	— — —	90 50 40	180 100 80	ns
$t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 5 \text{ ns}$						
$t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 17 \text{ ns}$						
$t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 15 \text{ ns}$						

*The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

FIGURE 1 – SWITCHING TIME TEST CIRCUITS AND WAVEFORMS



MC14580B

4 x 4 MULTIPOINT REGISTER

The MC14580B is a 4 by 4 multipoint register useful in small scratch pad memories, arithmetic operations when coupled with an adder, and other data storage applications. It allows independent reading of any two words (or the same word at both outputs) while writing into any one of four words.

Address changing and data entry occur on the rising edge of the clock. When the write enable input is low, the contents of any word may be accessed but not altered.

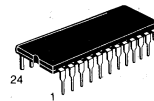
- No Restrictions on Clock Input Rise or Fall Times
- 3-State Outputs
- Single Phase Clocking
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or one Low-power Schottky TTL Load Over the Rated Temperature Range
- Pin Compatible with CD40108

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

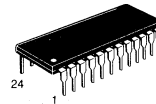
Symbol	Parameter	Value	Unit
V _{DD}	DC Supply Voltage	-0.5 to +18.0	V
V _{in, Vout}	Input or Output Voltage (DC or Transient)	-0.5 to V _{DD} + 0.5	V
I _{in, Iout}	Input or Output Current (DC or Transient), per Pin	± 10	mA
P _D	Power Dissipation, per Package†	500	mW
T _{stg}	Storage Temperature	-65 to +150	°C
T _L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.

†Temperature Derating: Plastic "P and D/DW" Packages: -7.0 mW/°C From 65°C To 125°C
Ceramic "L" Packages: -12 mW/°C From 100°C To 125°C



L SUFFIX
CERAMIC
CASE 623



P SUFFIX
PLASTIC
CASE 709



DW SUFFIX
SOIC
CASE 751E

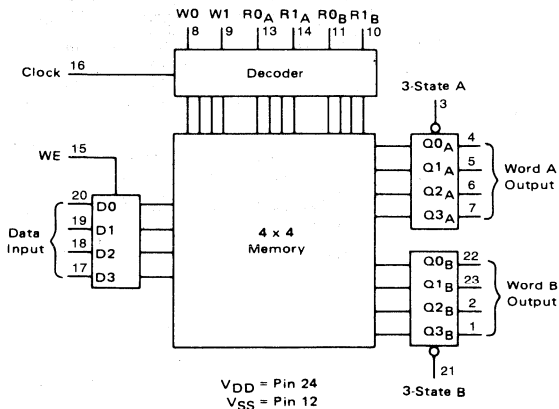
ORDERING INFORMATION

MC14XXXBCP Plastic
MC14XXXBCL Ceramic
MC14XXXBDW SOIC

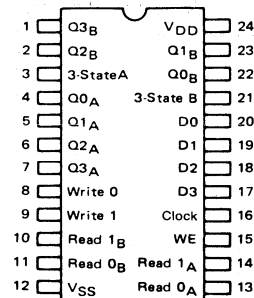
T_A = -55° to 125°C for all packages.

6

BLOCK DIAGRAM



PIN ASSIGNMENT



MC14580B

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	-55°C		25°C			125°C		Unit		
			Min	Max	Min	Typ #	Max	Min	Max			
Output Voltage $V_{in} = V_{DD}$ or 0	V_{OL}	5.0	—	0.05	—	0	0.05	—	0.05	Vdc		
		10	—	0.05	—	0	0.05	—	0.05			
		15	—	0.05	—	0	0.05	—	0.05			
	$V_{in} = 0$ or V_{DD}	V_{OH}	5.0	4.95	—	4.95	5.0	—	4.95		—	
			10	9.95	—	9.95	10	—	9.95		—	
			15	14.95	—	14.95	15	—	14.95		—	
Input Voltage ($V_O = 4.5$ or 0.5 Vdc) ($V_O = 9.0$ or 1.0 Vdc) ($V_O = 13.5$ or 1.5 Vdc)	V_{IL}	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc		
		10	—	3.0	—	4.50	3.0	—	3.0			
		15	—	4.0	—	6.75	4.0	—	4.0			
	V_{IH}	5.0	3.5	—	3.5	2.75	—	3.5	—		Vdc	
		10	7.0	—	7.0	5.50	—	7.0	—			
		15	11	—	11	8.25	—	11	—			
Output Drive Current ($V_{OH} = 2.5$ Vdc) ($V_{OH} = 4.6$ Vdc) ($V_{OH} = 9.5$ Vdc) ($V_{OH} = 13.5$ Vdc)	Source	I_{OH}	5.0	-3.0	—	-2.4	-4.2	—	-1.7	—		mAdc
			10	-0.64	—	-0.51	-0.88	—	-0.36	—		
			15	-4.2	—	-3.4	-8.8	—	-2.4	—		
	Sink	I_{OL}	5.0	0.64	—	0.51	0.88	—	0.36	—		
			10	1.6	—	1.3	2.25	—	0.9	—		
			15	4.2	—	3.4	8.8	—	2.4	—		
Input Current	I_{in}	15	—	± 0.1	—	± 0.00001	± 0.1	—	± 1.0	μ Adc		
Input Capacitance ($V_{in} = 0$)	C_{in}	—	—	—	—	5.0	7.5	—	—	pF		
Quiescent Current (Per Package)	I_{DD}	5.0	—	5.0	—	0.010	5.0	—	150	μ Adc		
		10	—	10	—	0.020	10	—	300			
		15	—	20	—	0.030	20	—	600			
Total Supply Current**† (Dynamic plus Quiescent, Per Package) ($C_L = 50$ pF on all outputs, all buffers switching)	I_T	5.0	$I_T = (1.18 \mu\text{A/kHz}) f + I_{DD}$ $I_T = (1.91 \mu\text{A/kHz}) f + I_{DD}$ $I_T = (2.67 \mu\text{A/kHz}) f + I_{DD}$							μ Adc		
		10										
		15										
Three-State Leakage Current	I_{TL}	15	—	± 0.1	—	± 0.00001	± 0.1	—	± 3.0	μ Adc		

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) V/k$$

where: I_T is in μA (per package), C_L in pF, $V = (V_{DD} - V_{SS})$ in volts, f in kHz is input frequency, and $k = 0.004$.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

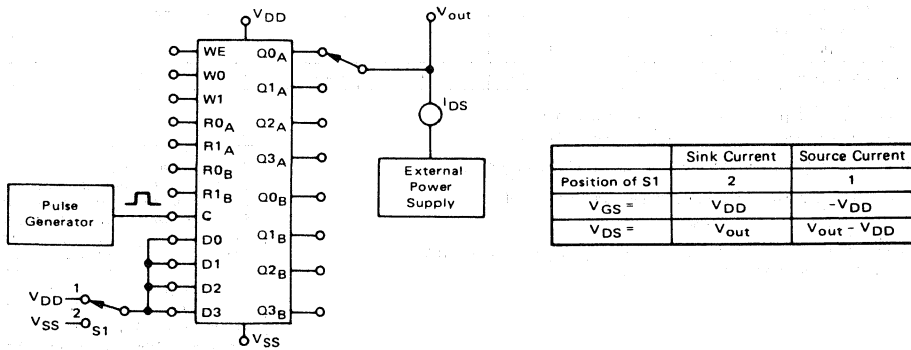
MC14580B

SWITCHING CHARACTERISTICS* ($C_L = 50$ pF, $T_A = 25^\circ\text{C}$)

Characteristic	Symbol	V _{DD}	Min	Typ #	Max	Unit
Output Rise and Fall Time $t_{TLH}, t_{THL} = (1.5 \text{ ns/pF}) C_L + 25 \text{ ns}$ $t_{TLH}, t_{THL} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$ $t_{TLH}, t_{THL} = (0.55 \text{ ns/pF}) C_L + 9.5 \text{ ns}$	t_{TLH}, t_{THL} (Figures 3 and 6)	5.0 10 15	— — —	100 50 40	200 100 80	ns
Propagation Delay Time Clock to Output	t_{PLH}, t_{PHL} (Figures 3 and 6)	5.0 10 15	— — —	650 250 170	1300 500 340	ns
Write Enable Setup Time (Enabling a Write or Read)	t_{su} (Figure 5)	5.0 10 15	800 300 200	400 150 100	— — —	ns
Write Enable Removal Time (Disabling a Write or Read)	t_{rem} (Figure 5)	5.0 10 15	0 0 0	-100 -50 -35	— — —	ns
Setup Time** Address, Data to Clock	t_{su} (Figure 3)	5.0 10 15	50 30 25	20 0 0	— — —	ns
Hold Time** Clock to Address, Data	t_h (Figure 3)	5.0 10 15	480 195 150	160 65 50	— — —	ns
3-State Enable/Disable Delay Time	t_{PHZ}, t_{PLZ} t_{PZH}, t_{PZL} (Figures 4 and 7)	5.0 10 15	— — —	130 60 45	260 120 90	ns
Clock Pulse Width	t_w (Figure 3)	5.0 10 15	820 330 220	410 165 110*	— — —	ns

**When loading repetitive highs, the output may glitch low momentarily after the rising edge of Clock. However, data integrity remains unaffected and data is valid after the propagation delays listed in the Switching Characteristics Table.

FIGURE 1 – OUTPUT DRIVE CURRENT TEST CIRCUIT



MC14580B

FIGURE 2 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORMS (3-State Inputs are High)

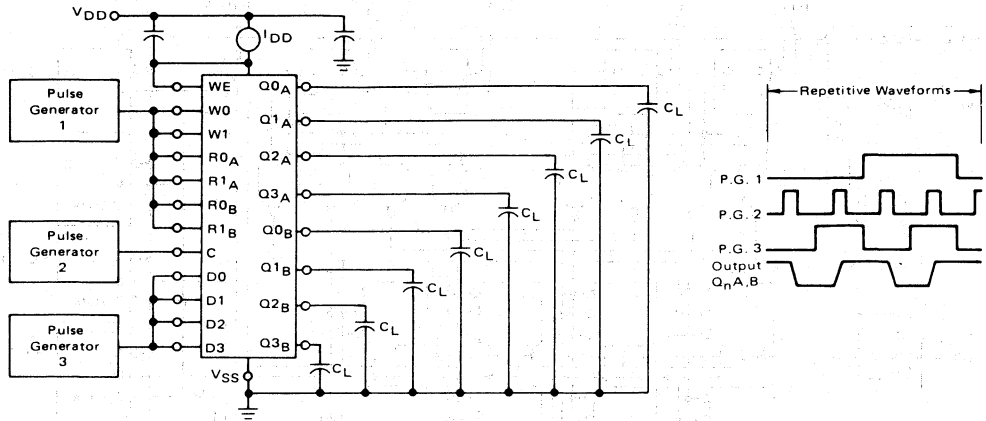


FIGURE 3

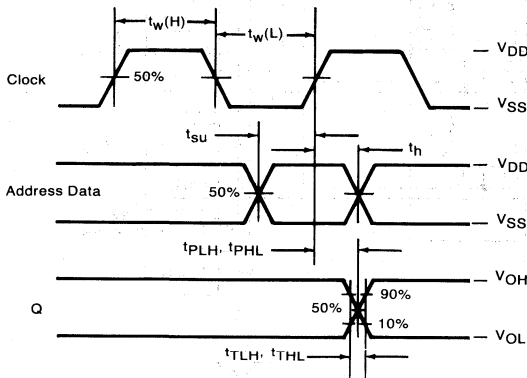


FIGURE 4

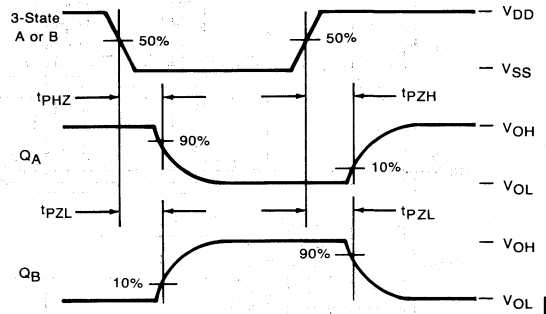


FIGURE 5

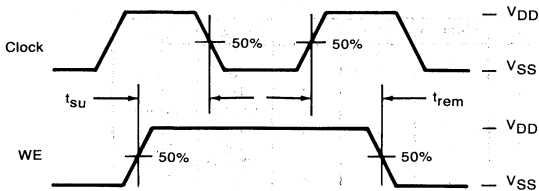


FIGURE 6 – TEST CIRCUIT

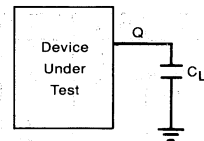
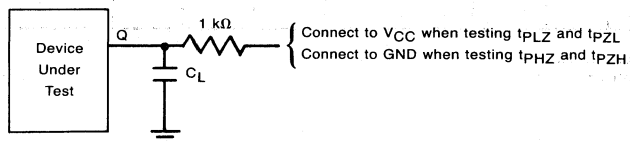
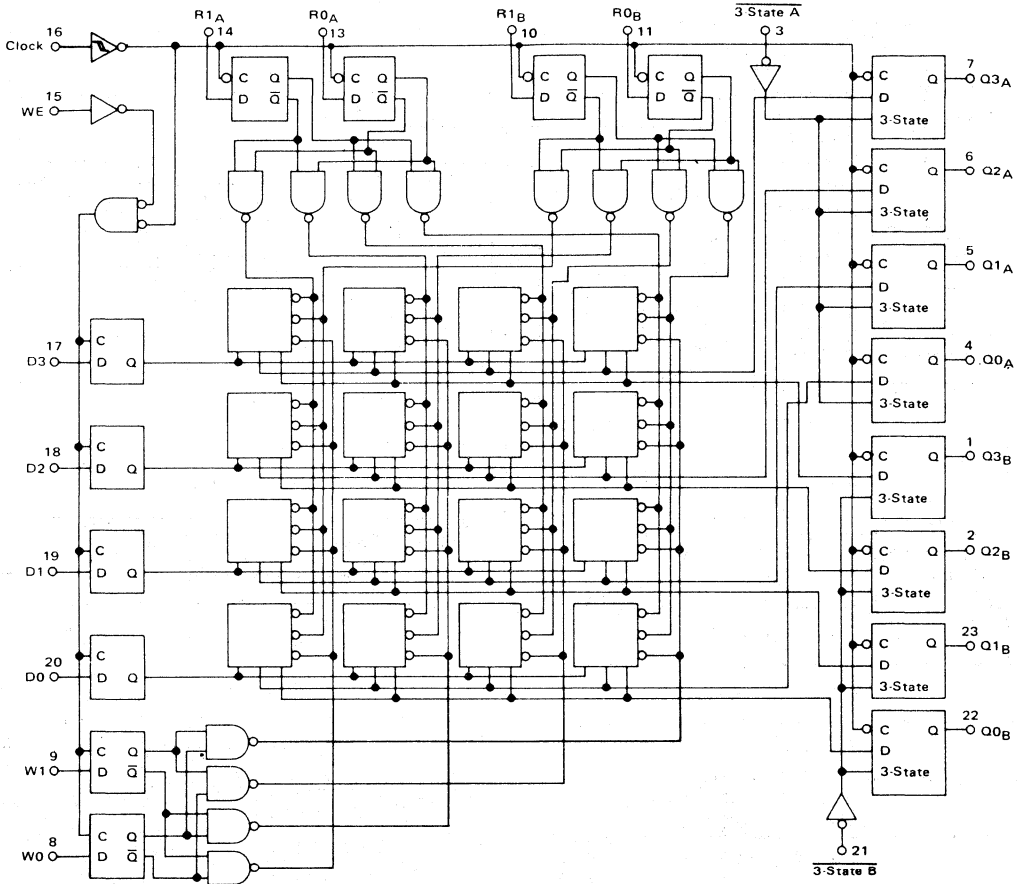


FIGURE 7 – TEST CIRCUIT



MC14580B

LOGIC DIAGRAM



6

TRUTH TABLE

Clock	WE	Write 1	Write 0	Read 1 _A	Read 0 _A	Read 1 _B	Read 0 _B	3-State A	3-State B	D _n	Q _{nA}	Q _{nB}
	1	0	1	0	1	0	1	1	1	1	1	1
	1	0	1	0	1	0	1	1	1	0	0	0
	X	X	X	X	X	X	X	1	1	X	No Change	No Change
X	X	X	X	X	X	X	X	0	0	X	Z	Z
0	X	X	X	X	X	X	X	1	1	X	No Change	No Change
1	X	X	X	X	X	X	X	1	1	X	No Change	No Change
	1	0	0	0	1	1	0	1	1	D _n to word 0	Change	Change
	0	0	0	0	1	1	0	1	1	Word 0 not altered	Contents of word 1 displayed	Contents of word 2 displayed

Z = High Impedance
X = Don't care



MOTOROLA

MC14581B

4-BIT ARITHMETIC LOGIC UNIT

The MC14581B is a CMOS 4-bit ALU capable of providing 16 functions of two Boolean variables and 16 binary arithmetic operations on two 14-bit words. The level of the mode control input determines whether the output function is logic or arithmetic. The desired logic function is selected by applying the appropriate binary word to the select inputs (S0 thru S3) with the mode control input high, while the desired arithmetic operation is selected by applying a low voltage to the mode control input, the required level to carry in, and the appropriate word to the select inputs. The word inputs and function outputs can be operated with either active high or active low data.

Carry propagate (\overline{P}) and carry generate (\overline{G}) outputs are provided to allow a full look-ahead carry scheme for fast simultaneous carry generation for the four bits in the package. Fast arithmetic operations on long words are obtainable by using the MC14582B as a second order look ahead block. An inverted ripple carry input (C_n) and a ripple carry output (C_{n+4}) are included for ripple through operation.

When the device is in the subtract mode (LHHL), comparison of two 4-bit words present at the \overline{A} and \overline{B} inputs is provided using the A = B output. It assumes a high-level state when indicating equality. Also, when the ALU is in the subtract mode the C_{n+4} output can be used to indicate relative magnitude as shown in this table:

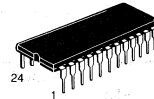
Data Level	C_n	C_{n+4}	Magnitude
Active High	H	H	$A \leq B$
	L	H	$A < B$
	L	L	$A > B$
Active Low	L	L	$A \leq B$
	H	H	$A < B$
	H	L	$A > B$

- Functional and Pinout Equivalent to 74181.
- Diode Protection on All Inputs
- All Outputs Buffered
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load over the Rated Temperature Range

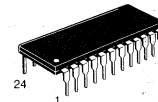
MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	-0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	-0.5 to $V_{DD} + 0.5$	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	± 10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

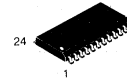
*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P and D/DW" Packages: -7.0 mW/°C From 65°C To 125°C
Ceramic "L" Packages: -12 mW/°C From 100°C To 125°C



L SUFFIX CERAMIC CASE 623



P SUFFIX PLASTIC CASE 709



DW SUFFIX SOIC CASE 751E

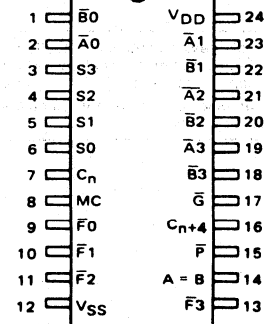
ORDERING INFORMATION

MC14XXXBCP Plastic
MC14XXXBCL Ceramic
MC14XXXBDW SOIC

$T_A = -55^\circ\text{C}$ to 125°C for all packages.

6

PIN ASSIGNMENT



MC14581B

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V _{DD} Vdc	-55°C		25°C			125°C		Unit
			Min	Max	Min	Typ #	Max	Min	Max	
Output Voltage V _{in} = V _{DD} or 0 V _{in} = 0 or V _{DD}	"0" Level V _{OL}	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
		10	—	0.05	—	0	0.05	—	0.05	
		15	—	0.05	—	0	0.05	—	0.05	
	"1" Level V _{OH}	5.0	4.95	—	4.95	5.0	—	4.95	—	
		10	9.95	—	9.95	10	—	9.95	—	
		15	14.95	—	14.95	15	—	14.95	—	
Input Voltage (V _O = 4.5 or 0.5 Vdc) (V _O = 9.0 or 1.0 Vdc) (V _O = 13.5 or 1.5 Vdc) (V _O = 0.5 or 4.5 Vdc) (V _O = 1.0 or 9.0 Vdc) (V _O = 1.5 or 13.5 Vdc)	"0" Level V _{IL}	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc
		10	—	3.0	—	4.50	3.0	—	3.0	
		15	—	4.0	—	6.75	4.0	—	4.0	
	"1" Level V _{IH}	5.0	3.5	—	3.5	2.75	—	3.5	—	
		10	7.0	—	7.0	5.50	—	7.0	—	
		15	11	—	11	8.25	—	11	—	
Output Drive Current (V _{OH} = 2.5 Vdc) (V _{OH} = 4.6 Vdc) (V _{OH} = 9.5 Vdc) (V _{OH} = 13.5 Vdc) (V _{OL} = 0.4 Vdc) (V _{OL} = 0.5 Vdc) (V _{OL} = 1.5 Vdc)	Source I _{OH}	5.0	-1.2	—	-1.0	-1.7	—	-0.7	—	mAdc
		5.0	-0.64	—	-0.51	-0.88	—	-0.36	—	
		10	-1.6	—	-1.3	-2.25	—	-0.9	—	
	Sink I _{OL}	5.0	0.64	—	0.51	0.88	—	0.36	—	
		10	1.6	—	1.3	2.25	—	0.9	—	
		15	4.2	—	3.4	8.8	—	2.4	—	
Input Current	I _{in}	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	μAdc
Input Capacitance (V _{in} = 0)	C _{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)	I _{DD}	5.0	—	5.0	—	0.005	5.0	—	150	μAdc
		10	—	10	—	0.010	10	—	300	
		15	—	20	—	0.015	20	—	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C _L = 50 pF on all outputs, all buffers switching)	I _T	5.0 10 15	I _T = (1.8 μA/kHz) f + I _{DD} I _T = (3.7 μA/kHz) f + I _{DD} I _T = (5.5 μA/kHz) f + I _{DD}						μAdc	

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) Vfk$$

where: I_T is in μA (per package), C_L in pF, V = (V_{DD} - V_{SS}) in volts, f in kHz is input frequency, and k = 0.008.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range V_{SS} ≤ (V_{in} or V_{out}) ≤ V_{DD}. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

MC14581B

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V _{DD}	Min	Typ #	Max	Unit
Output Rise and Fall Time	t_{TLH} , t_{THL}					ns
$t_{TLH}, t_{THL} = (1.5 \text{ ns/pF}) C_L + 25 \text{ ns}$	t_{TLH}	5.0	—	100	200	
$t_{TLH}, t_{THL} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$	t_{THL}	10	—	50	100	
$t_{TLH}, t_{THL} = (0.55 \text{ ns/pF}) C_L + 9.5 \text{ ns}$		15	—	40	80	
Propagation Delay Time	t_{PLH} , t_{PHL}					ns
Sum in to Sum Out						
$t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 620 \text{ ns}$	t_{PLH}	5.0	—	705	1410	
$t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 217 \text{ ns}$	t_{PHL}	10	—	250	500	
$t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 155 \text{ ns}$		15	—	180	360	
Sum in to Sum Out (Logic Mode)	t_{PLH} , t_{PHL}					ns
$t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 520 \text{ ns}$	t_{PLH}	5.0	—	605	1210	
$t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 182 \text{ ns}$	t_{PHL}	10	—	215	430	
$t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 155 \text{ ns}$		15	—	180	360	
Sum in to A = B	t_{PLH} , t_{PHL}					ns
$t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 870 \text{ ns}$	t_{PLH}	5.0	—	955	1910	
$t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 297 \text{ ns}$	t_{PHL}	10	—	330	660	
$t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 220 \text{ ns}$		15	—	245	490	
Sum In to P or G	t_{PLH} , t_{PHL}					ns
$t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 400 \text{ ns}$	t_{PLH}	5.0	—	485	970	
$t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 147 \text{ ns}$	t_{PHL}	10	—	180	360	
$t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 105 \text{ ns}$		15	—	130	260	
Sum In to C_{n+4}	t_{PLH}					ns
$t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 530 \text{ ns}$	t_{PLH}	5.0	—	615	1230	
$t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 187 \text{ ns}$	t_{PHL}	10	—	220	440	
$t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 135 \text{ ns}$		15	—	160	360	
Carry In to Sum Out	t_{PLH} , t_{PHL}					ns
$t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 295 \text{ ns}$	t_{PLH}	5.0	—	380	760	
$t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 112 \text{ ns}$	t_{PHL}	10	—	145	290	
$t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 80 \text{ ns}$		15	—	105	210	
Carry in to C_{n+4}	t_{PLH} , t_{PHL}					ns
$t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 220 \text{ ns}$	t_{PLH}	5.0	—	305	610	
$t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 87 \text{ ns}$	t_{PHL}	10	—	120	240	
$t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 60 \text{ ns}$		15	—	85	170	

*The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

AC TEST SETUP REFERENCE TABLE

TEST	AC PATHS		DC DATA INPUTS		MODE	FIG. 3 WAVEFORM
	INPUTS	OUTPUTS	TO V _{SS}	TO V _{DD}		
Sum _{in} to Sum _{out} Delay Time	\bar{A}_0	Any \bar{F}	Remaining \bar{A} 's C _n	All \bar{B} 's	Add	#1
Sum _{in} to \bar{P} Delay Time	\bar{A}_0	\bar{P}	Remaining \bar{A} 's C _n	All \bar{B} 's	Add	#1
Sum _{in} to \bar{G} Delay Time	\bar{B}_0	\bar{G}	All \bar{A} 's C _n	Remaining \bar{B} 's	Add	#1
Sum _{in} to C _{n+4} Delay Time	\bar{B}_0	C _{n+y}	All \bar{A} 's C _n	Remaining \bar{B} 's	Add	#2
C _n to Sum _{out} Delay Time	C _n	Any \bar{F}	All \bar{A} 's	All \bar{B} 's	Add	#1
C _n to C _{n+4} Delay Time	C _n	C _{n+4}	All \bar{A} 's	All \bar{B} 's	Add	#1
Sum _{in} to A = B Delay Time	\bar{A}_0	A = B	All \bar{B} 's Remaining \bar{A} 's	C _n	Sub	#2
Sum _{in} to Sum _{out} Delay Time (Logic Mode)	\bar{B}_0	Any \bar{F}	All A's	M	Exclusive OR	#2

MC14581B

FIGURE 1 – TYPICAL SOURCE CURRENT TEST CIRCUIT

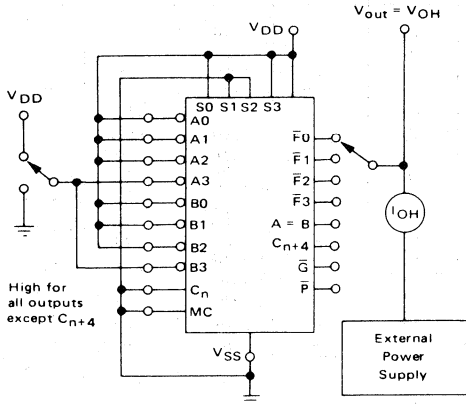


FIGURE 2 – TYPICAL SINK CURRENT TEST CIRCUIT

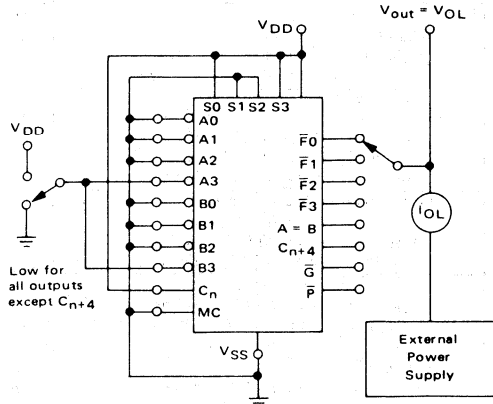


FIGURE 3 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

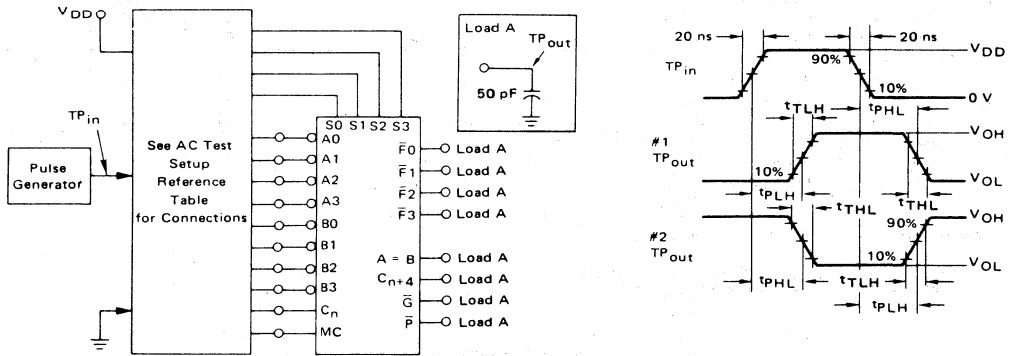
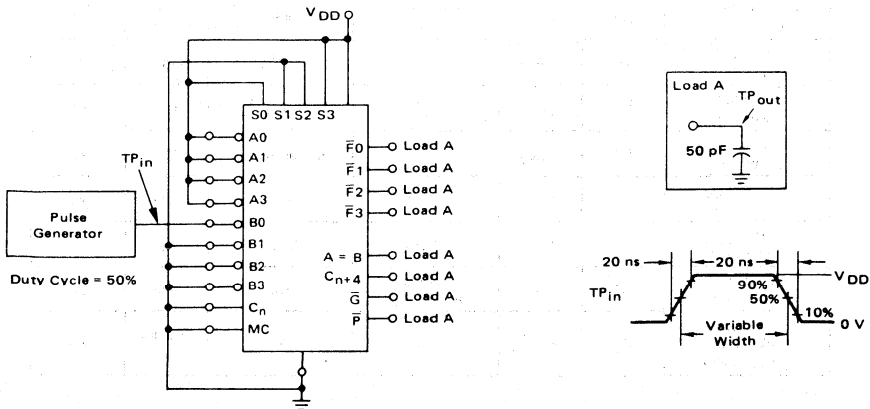
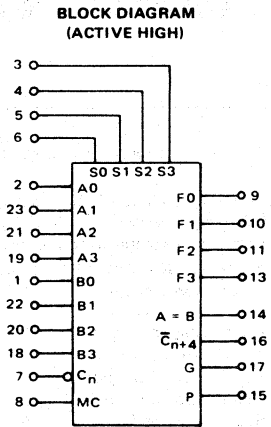
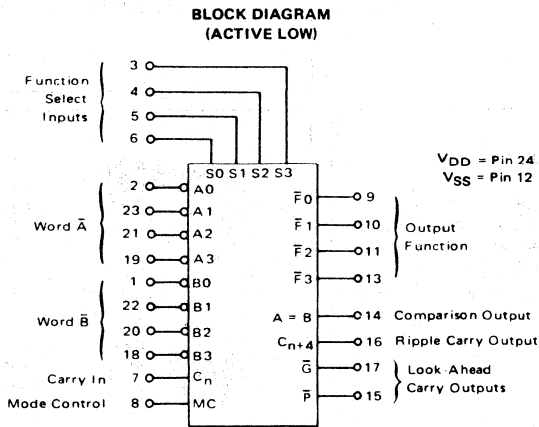


FIGURE 4 – DYNAMIC POWER DISSIPATION TEST CIRCUIT AND WAVEFORM



MC14581B



TRUTH TABLE

FUNCTION SELECT	INPUTS/OUTPUTS ACTIVE LOW				INPUTS/OUTPUTS ACTIVE HIGH			
	LOGIC FUNCTION (MC = H)				LOGIC FUNCTION (MC = H)			
	S3	S2	S1	S0	LOGIC FUNCTION (MC = L, C _n = L)	LOGIC FUNCTION (MC = H)	ARITHMETIC* FUNCTION (MC = L, C _n = H)	ARITHMETIC* FUNCTION (MC = L, C _n = H)
L	L	L	L	\bar{A}	A minus 1	\bar{A}	A	
L	L	L	H	$\bar{A}\bar{B}$	AB minus 1	$\bar{A} + \bar{B}$	A + B	
L	L	H	L	$\bar{A} + \bar{B}$	$\bar{A}\bar{B}$ minus 1	$\bar{A}\bar{B}$	A + \bar{B}	
L	L	H	H	Logic "1"	minus 1	Logic "0"	minus 1	
L	H	L	L	$\bar{A} + \bar{B}$	A plus (A + \bar{B})	$\bar{A}\bar{B}$	A plus $\bar{A}\bar{B}$	
L	H	L	H	\bar{B}	AB plus (A + \bar{B})	\bar{B}	(A + B) plus $\bar{A}\bar{B}$	
L	H	H	L	$A \oplus B$	A minus B minus 1	$A \oplus B$	A minus B minus 1	
L	H	H	H	$A + \bar{B}$	A + \bar{B}	$\bar{A}\bar{B}$	$\bar{A}\bar{B}$ minus 1	
H	L	L	L	$\bar{A}\bar{B}$	A plus (A + B)	$\bar{A} + \bar{B}$	A plus AB	
H	L	L	H	$A \oplus B$	A plus B	$A \oplus B$	A plus B	
H	L	H	L	B	$\bar{A}\bar{B}$ plus (A + B)	B	(A + \bar{B}) plus AB	
H	L	H	H	A + B	A + B	AB	AB minus 1	
H	H	L	L	Logic "0"	A plus A	Logic "1"	A plus A	
H	H	L	H	$\bar{A}\bar{B}$	AB plus A	$A + \bar{B}$	(A + B) plus A	
H	H	H	L	AB	$\bar{A}\bar{B}$ plus A	A + B	(A + \bar{B}) plus A	
H	H	H	H	A	A	A	A minus 1	

* Expressed as two's complements. For arithmetic function with C_n in the opposite state, the resulting function is as shown plus 1.



MOTOROLA

MC14582B

LOOK-AHEAD CARRY BLOCK

The MC14582B is a CMOS look-ahead carry generator capable of anticipating a carry across four binary adders or groups of adders. The device is cascadable to perform full look-ahead across n-bit adders. Carry, generate-carry, and propagate-carry functions are provided as enumerated in the pin designation table shown below.

- Expandable to any Number of Bits
- All Buffered Outputs
- Low Power Dissipation
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-Power Schottky TTL Load over the Rated Temperature Range

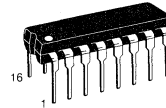
MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V _{DD}	DC Supply Voltage	-0.5 to +18.0	V
V _{in} , V _{out}	Input or Output Voltage (DC or Transient)	-0.5 to V _{DD} + 0.5	V
I _{in} , I _{out}	Input or Output Current (DC or Transient), per Pin	± 10	mA
P _D	Power Dissipation, per Package†	500	mW
T _{stg}	Storage Temperature	-65 to +150	°C
T _L	Lead Temperature (8-Second Soldering)	260	°C

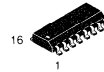
*Maximum Ratings are those values beyond which damage to the device may occur.
 †Temperature Derating: Plastic "P and D/DW" Packages: -7.0 mW/°C From 65°C To 125°C
 Ceramic "L" Packages: -12 mW/°C From 100°C To 125°C



L SUFFIX
 CERAMIC
 CASE 620



P SUFFIX
 PLASTIC
 CASE 648



D SUFFIX
 SOIC
 CASE 751B

ORDERING INFORMATION

MC14XXXBCP Plastic
 MC14XXXBCL Ceramic
 MC14XXXBD SOIC

T_A = -55° to 125°C for all packages.

6

LOGIC EQUATIONS

$$C_{n+x} = \overline{G_0} + (P_0 \bullet C_n)$$

$$C_{n+y} = \overline{G_1} + (P_1 \bullet \overline{G_0}) + (P_1 \bullet P_0 \bullet C_n)$$

$$C_{n+z} = \overline{G_2} + (P_2 \bullet \overline{G_1}) + (P_2 \bullet P_1 \bullet \overline{G_0}) + (P_2 \bullet P_1 \bullet P_0 \bullet C_n)$$

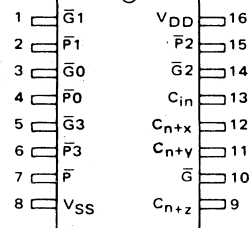
$$\overline{G} = \overline{G_3} + (P_3 \bullet \overline{G_2}) + (P_3 \bullet P_2 \bullet \overline{G_1}) + (P_3 \bullet P_2 \bullet P_1 \bullet \overline{G_0})$$

$$\overline{P} = \overline{P_3} \bullet \overline{P_2} \bullet \overline{P_1} \bullet \overline{P_0}$$

PIN DESIGNATIONS

DESIGNATION	PIN NO's	FUNCTION
$\overline{G_0}, \overline{G_1}, \overline{G_2}, \overline{G_3}$	3, 1, 14, 5	Active-Low Carry-Generate Inputs
$\overline{P_0}, \overline{P_1}, \overline{P_2}, \overline{P_3}$	4, 2, 15, 6	Active-Low Carry-Propagate Inputs
C _n	13	Carry Input
C _{n+x} , C _{n+y} , C _{n+z}	12, 11, 9	Carry Outputs
\overline{G}	10	Active-Low Group Carry-Generate Output
\overline{P}	7	Active-Low Group Carry-Propagate Output

PIN ASSIGNMENT



MC14582B

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V _{DD} Vdc	-55°C		25°C			125°C		Unit
			Min	Max	Min	Typ #	Max	Min	Max	
Output Voltage V _{in} = V _{DD} or 0	V _{OL}	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
		10	—	0.05	—	0	0.05	—	0.05	
V _{in} = 0 or V _{DD}	V _{OH}	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc
		10	9.95	—	9.95	10	—	9.95	—	
Input Voltage (V _O = 4.5 or 0.5 Vdc) (V _O = 9.0 or 1.0 Vdc) (V _O = 13.5 or 1.5 Vdc)	V _{IL}	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc
		10	—	3.0	—	4.50	3.0	—	3.0	
(V _O = 0.5 or 4.5 Vdc) (V _O = 1.0 or 9.0 Vdc) (V _O = 1.5 or 13.5 Vdc)	V _{IH}	5.0	3.5	—	3.5	2.75	—	3.5	—	Vdc
		10	7.0	—	7.0	5.50	—	7.0	—	
Output Drive Current (V _{OH} = 2.5 Vdc) (V _{OH} = 4.6 Vdc) (V _{OH} = 9.5 Vdc) (V _{OH} = 13.5 Vdc)	Source I _{OH}	5.0	-3.0	—	-2.4	-4.2	—	-1.7	—	mA _{dc}
		10	-0.64	—	-0.51	-0.88	—	-0.36	—	
(V _{OL} = 0.4 Vdc) (V _{OL} = 0.5 Vdc) (V _{OL} = 1.5 Vdc)	Sink I _{OL}	5.0	0.64	—	0.51	0.88	—	0.36	—	mA _{dc}
		10	1.6	—	1.3	2.25	—	0.9	—	
		15	4.2	—	3.4	8.8	—	2.4	—	
Input Current	I _{in}	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	μA _{dc}
Input Capacitance (V _{in} = 0)	C _{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)	I _{DD}	5.0	—	5.0	—	0.005	5.0	—	150	μA _{dc}
		10	—	10	—	0.010	10	—	300	
		15	—	20	—	0.015	20	—	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C _L = 50 pF on all outputs, all buffers switching)	I _T	5.0	I _T = (1.4 μA/kHz) f + I _{DD}							μA _{dc}
		10	I _T = (2.8 μA/kHz) f + I _{DD}							
		15	I _T = (4.3 μA/kHz) f + I _{DD}							

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) V/k$$

where: I_T is in μA (per package), C_L in pF, V = (V_{DD} - V_{SS}) in volts, f in kHz is input frequency, and k = 0.005.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range V_{SS} ≤ (V_{in} or V_{out}) ≤ V_{DD}. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

MC14582B

SWITCHING CHARACTERISTICS* ($C_L = 50 \text{ pF}$, $T_A = 25^\circ\text{C}$)

Characteristic	Symbol	V_{DD}	Min	Typ #	Max	Unit
Output Rise and Fall Time	t_{TLH} , t_{THL}	5.0	—	100	200	ns
t_{TLH} , $t_{THL} = (1.5 \text{ ns/pF}) C_L + 25 \text{ ns}$		10	—	50	100	
t_{TLH} , $t_{THL} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$		15	—	40	80	
Propagation Delay Time	t_{PLH} , t_{PHL}	5.0	—	345	690	ns
t_{PLH} , $t_{PHL} = (1.7 \text{ ns/pF}) C_L + 260 \text{ ns}$		10	—	140	280	
t_{PLH} , $t_{PHL} = (0.66 \text{ ns/pF}) C_L + 107 \text{ ns}$		15	—	110	220	

*The formulas given are for the typical characteristics only at 25°C .

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

FIGURE 1 – DYNAMIC POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

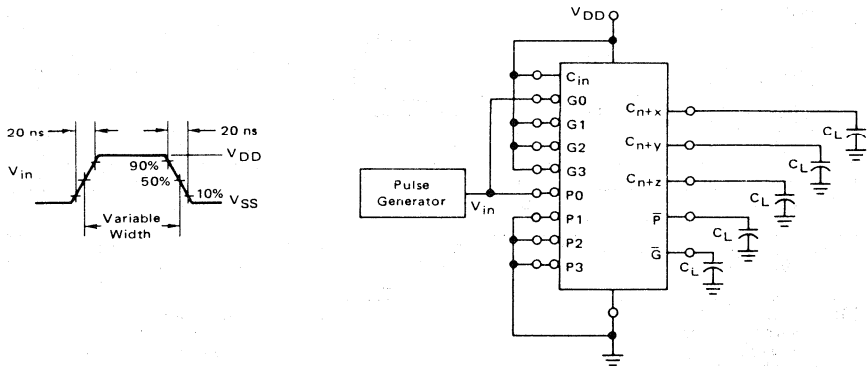


FIGURE 2 – SOURCE CURRENT TEST CIRCUIT

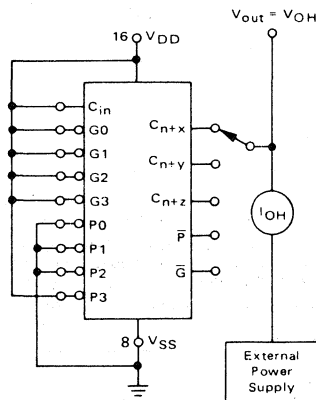
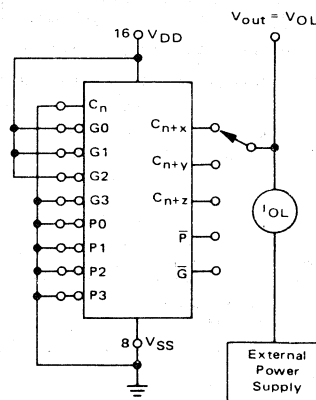
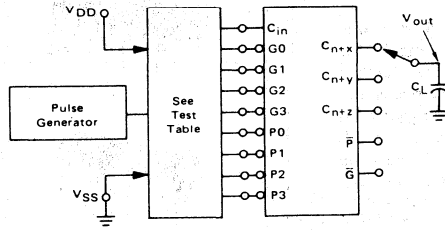


FIGURE 3 – SINK CURRENT TEST CIRCUIT



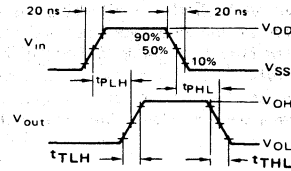
MC14582B

FIGURE 4 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

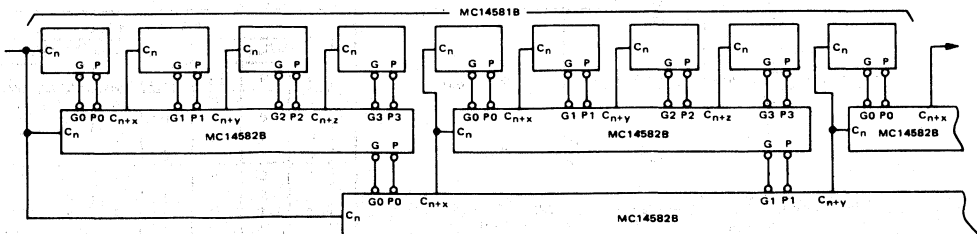
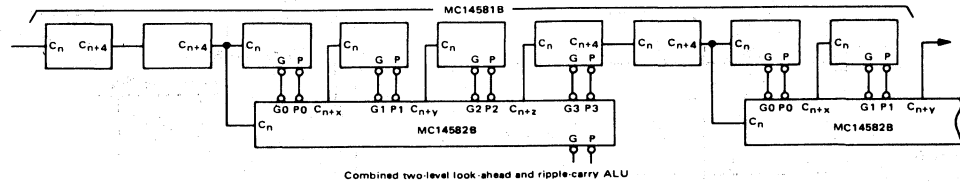
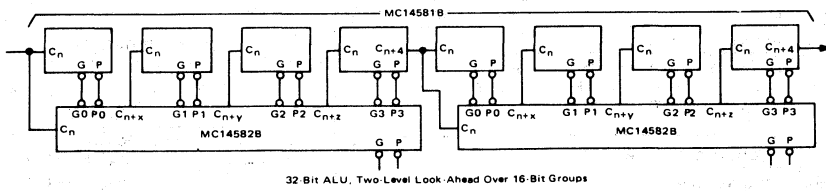
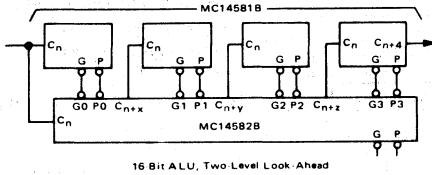
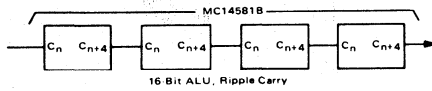


TEST TABLE

AC PATHS		DC DATA	
INPUT	OUTPUT	To VSS	To VDD
P0	P-bar	Remaining P's, Cn	G-bar's
G0	G-bar	P-bar's, Cn	Remaining G-bar's
Cn	Cn+x, Cn+y, Cn+z	P-bar's	G-bar's



TYPICAL APPLICATIONS



A and B inputs and F outputs are not shown (MC14581B).



MC14583B

DUAL SCHMITT TRIGGER

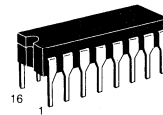
The MC14583B is a dual Schmitt trigger constructed with complementary P-channel and N-channel MOS devices on a monolithic silicon substrate. Each Schmitt trigger is functionally independent except for a common 3-state input and an internally-connected Exclusive OR output for use in line receiver applications. Trigger levels are adjustable through the positive, negative, and common terminals with the use of external resistors. Applications include the speed-up of a slow waveform edge in interface receivers, level detectors, etc.

- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Single Supply Operation
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range
- Resistor Adjustable Trigger Levels

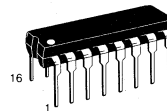
MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V _{DD}	DC Supply Voltage	-0.5 to +18.0	V
V _{in} , V _{out}	Input or Output Voltage (DC or Transient)	-0.5 to V _{DD} + 0.5	V
I _{in} , I _{out}	Input or Output Current (DC or Transient), per Pin	± 10	mA
P _D	Power Dissipation, per Package†	500	mW
T _{stg}	Storage Temperature	-65 to +150	°C
T _L	Lead Temperature (8-Second Soldering)	260	°C

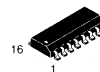
*Maximum Ratings are those values beyond which damage to the device may occur.
 †Temperature Derating: Plastic "P and D/DW" Packages: -7.0 mW/°C From 65°C To 125°C
 Ceramic "L" Packages: -12 mW/°C From 100°C To 125°C



L SUFFIX
CERAMIC
CASE 620



P SUFFIX
PLASTIC
CASE 648



D SUFFIX
SOIC
CASE 751B

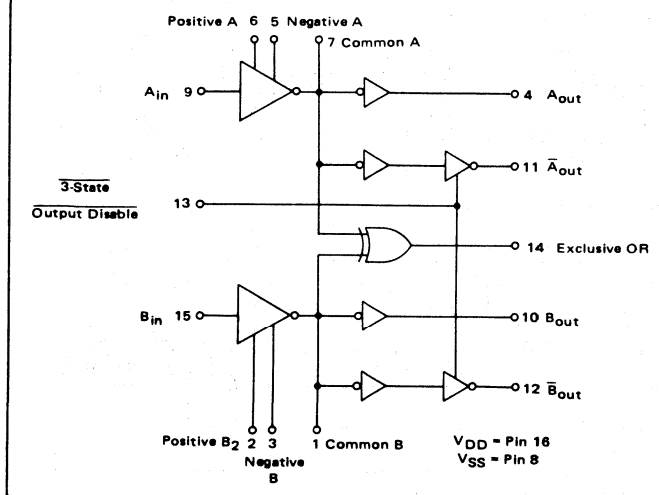
ORDERING INFORMATION

MC14XXXBCP Plastic
 MC14XXXBCL Ceramic
 MC14XXXBD SOIC

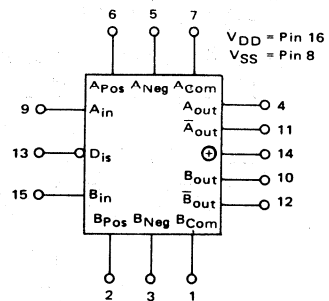
T_A = -55° to 125°C for all packages.

6

LOGIC DIAGRAM



BLOCK DIAGRAM



TRUTH TABLE

INPUTS			OUTPUTS				
A	B	D _{is}	A _{out}	A _{out}	B _{out}	B _{out}	⊕
0	0	0	0	Z	0	Z	0
0	0	1	0	1	0	1	0
0	1	0	0	Z	1	Z	1
0	1	1	0	1	1	0	1
1	0	0	1	Z	0	Z	1
1	0	1	1	0	0	1	1
1	1	0	1	Z	1	Z	0
1	1	1	1	0	1	0	0

Z = High impedance at output

MC14583B

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V _{DD} Vdc	-55°C		25°C			125°C		Unit
			Min	Max	Min	Typ #	Max	Min	Max	
Output Voltage V _{in} = V _{DD} or 0	V _{OL}	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
		10	—	0.05	—	0	0.05	—	0.05	
V _{in} = 0 or V _{DD}	V _{OH}	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc
		10	9.95	—	9.95	10	—	9.95	—	
Input Voltage A and B (V _O = 4.5 or 0.5 Vdc) (V _O = 9.0 or 1.0 Vdc) (V _O = 13.5 or 1.5 Vdc)	V _{IL}	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc
		10	—	3.0	—	4.50	3.0	—	3.0	
(V _O = 0.5 or 4.5 Vdc) (V _O = 1.0 or 9.0 Vdc) (V _O = 1.5 or 13.5 Vdc)	V _{IH}	5.0	3.5	—	3.5	2.75	—	3.5	—	Vdc
		10	7.0	—	7.0	5.50	—	7.0	—	
Output Drive Current (V _{OH} = 2.5 Vdc) (V _{OH} = 4.6 Vdc) (V _{OH} = 9.5 Vdc) (V _{OH} = 13.5 Vdc)	Source I _{OH}	5.0	-1.2	—	-1.0	-1.7	—	-0.7	—	mAdc
		10	-0.25	—	-0.2	-0.36	—	-0.14	—	
(V _{OL} = 0.4 Vdc) (V _{OL} = 0.5 Vdc) (V _{OL} = 1.5 Vdc)	Sink I _{OL}	5.0	0.64	—	0.51	0.88	—	0.36	—	mAdc
		10	1.6	—	1.3	2.25	—	0.9	—	
		15	4.2	—	3.4	8.8	—	2.4	—	
Input Current	I _{in}	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	μAdc
Input Capacitance (V _{in} = 0)	C _{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)	I _{DD}	5.0	—	0.25	—	0.0005	0.25	—	7.5	μAdc
		10	—	0.5	—	0.0010	0.5	—	15	
		15	—	1.0	—	0.0015	1.0	—	30	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C _L = 50 pF on all outputs, all buffers switching)	I _T	5.0	I _T = (1.33 μA/kHz) f + I _{DD}							μAdc
		10	I _T = (2.65 μA/kHz) f + I _{DD}							
		15	I _T = (3.98 μA/kHz) f + I _{DD}							
Three-State Leakage Current	I _{TL}	15	—	±0.1	—	±0.00001	±0.1	—	±3.0	μAdc

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

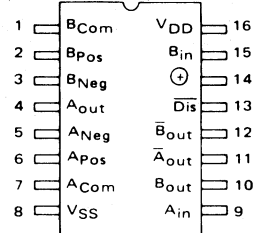
**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) Vfk$$

where: I_T is in μA (per package), C_L in pF, V = (V_{DD} - V_{SS}) in volts, f in kHz is input frequency, and k = 0.005.

PIN ASSIGNMENT



This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range V_{SS} ≤ (V_{in} or V_{out}) ≤ V_{DD}. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

MC14583B

SWITCHING CHARACTERISTICS* ($C_L = 50 \text{ pF}$, $T_A = 25^\circ\text{C}$)

Characteristic	Symbol	V _{DD}	Min	Typ #	Max	Unit
Output Rise Time $t_{TLH} = (3.0 \text{ ns/pF}) C_L + 30 \text{ ns}$ $t_{TLH} = (1.5 \text{ ns/pF}) C_L + 15 \text{ ns}$ $t_{TLH} = (1.1 \text{ ns/pF}) C_L + 10 \text{ ns}$	t_{TLH}	5.0 10 15	— — —	180 90 65	360 180 130	ns
Output Fall Time $t_{THL} = (1.5 \text{ ns/pF}) C_L + 25 \text{ ns}$ $t_{THL} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$ $t_{THL} = (0.55 \text{ ns/pF}) C_L + 9.5 \text{ ns}$	t_{THL}	5.0 10 15	— — —	100 50 40	200 100 80	ns
Propagation Delay Time A_{in}, B_{in} to A_{out}, B_{out} $t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 565 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 197 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 125 \text{ ns}$ A_{in}, B_{in} to A_{out}, B_{out} $t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 1015 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 347 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 235 \text{ ns}$ A_{in}, B_{in} to Exclusive OR $t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 665 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 257 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 145 \text{ ns}$	$t_{PLH},$ t_{PHL}	5.0 10 15	— — —	650 230 150	1300 460 300	ns
	$t_{PLH},$ t_{PHL}	5.0 10 15	— — —	1100 380 260	2200 760 520	ns
	$t_{PLH},$ t_{PHL}	5.0 10 15	— — —	750 280 170	1500 560 340	ns
3-State Enable, Disable Delay Time (see figure 5) $t_{on}, t_{off} = (1.7 \text{ ns/pF}) C_L + 140 \text{ ns}$ $t_{on}, t_{off} = (0.66 \text{ ns/pF}) C_L + 57 \text{ ns}$ $t_{on}, t_{off} = (0.5 \text{ ns/pF}) C_L + 30 \text{ ns}$	$t_{on},$ t_{off}	5.0 10 15	— — —	225 90 55	450 180 110	ns
Positive Threshold Voltage ($R_1, R_2 = 5.0 \text{ k}\Omega$)	V_{T+}	5.0 10 15	— — —	3.30 5.70 8.20	— — —	Vdc
Negative Threshold Voltage ($R_1, R_2 = 5.0 \text{ k}\Omega$)	V_{T-}	5.0 10 15	— — —	1.70 4.30 6.80	— — —	Vdc
Hysteresis Voltage ($R_1, R_2 = 5.0 \text{ k}\Omega$)	V_H	5.0 10 15	0.85 0.70 0.70	1.70 1.40 1.40	3.40 2.80 2.80	Vdc
Threshold Voltage Variation, A to B ($R_1, R_2 = 5.0 \text{ k}\Omega$)	ΔV_T	5.0 10 15	— — —	0.1 0.15 0.20	— — —	Vdc

*The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

MC14583B

FIGURE 1 – TYPICAL OUTPUT SOURCE AND SINK CHARACTERISTICS TEST CIRCUIT

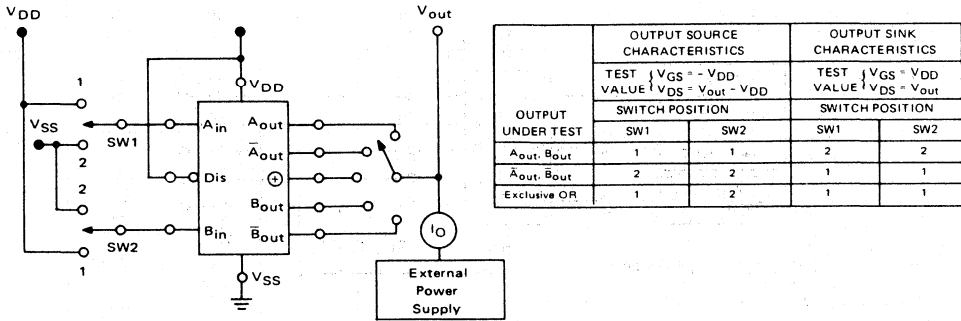


FIGURE 2 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORMS

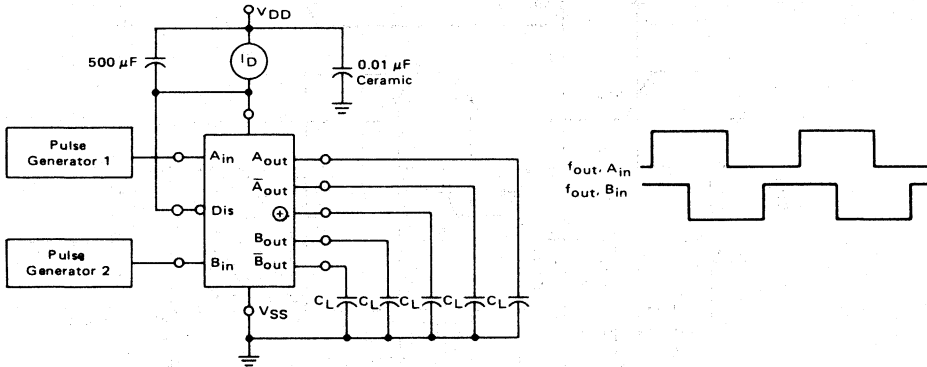
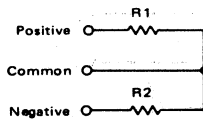
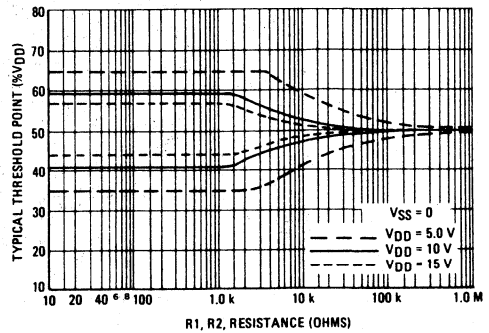
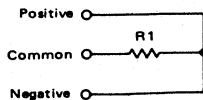


FIGURE 3 – TYPICAL THRESHOLD POINTS

A – Feedback scheme for independent threshold adjustment:

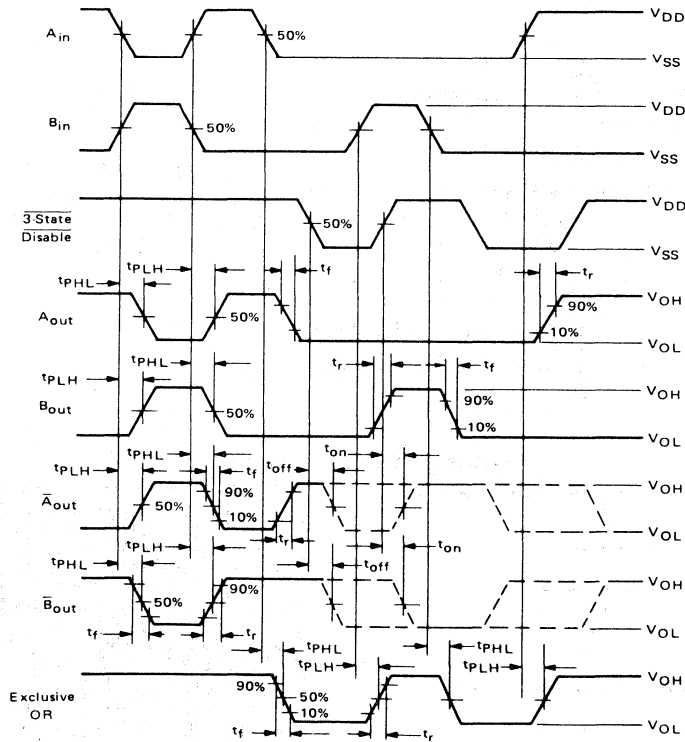
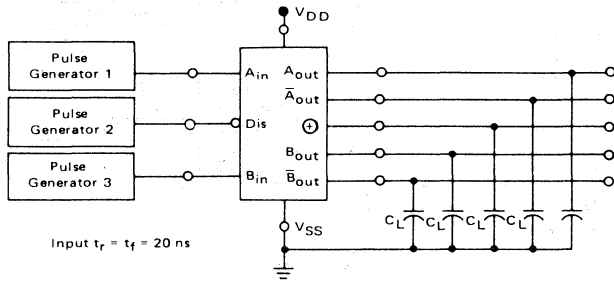


B – Feedback scheme for hysteresis adjustment:



MC14583B

FIGURE 4 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

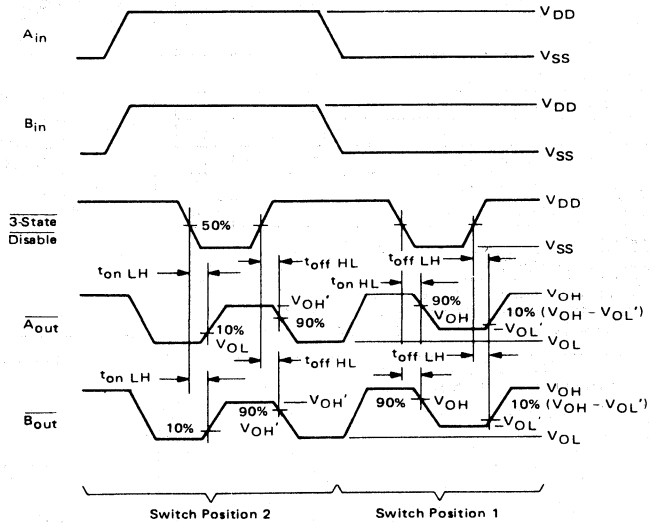
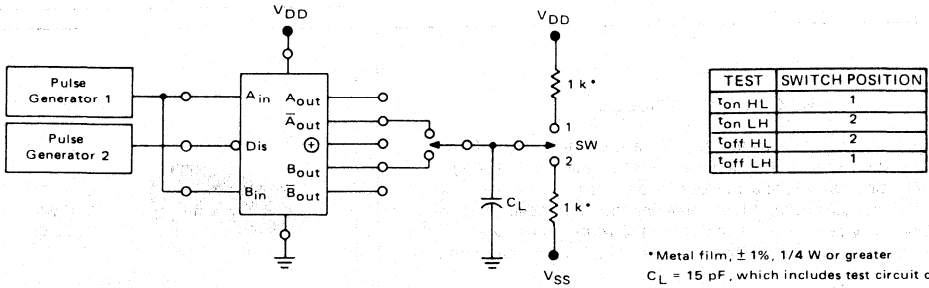


Note: Dashed lines indicate high output resistance.

6

MC14583B

FIGURE 5 – 3-STATE SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



V_{OL}' and V_{OH}' refer to the levels present as a result of the 1 k ohm load resistors.



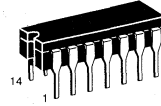
MOTOROLA

MC14584B

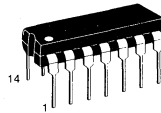
HEX SCHMITT TRIGGER

The MC14584B Hex Schmitt Trigger is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These devices find primary use where low power dissipation and/or high noise immunity is desired. The MC14584B may be used in place of the MC14069UB hex inverter for enhanced noise immunity to "square up" slowly changing waveforms.

- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load over the Rated Temperature Range
- Double Diode Protection on All Inputs
- Can Be Used to Replace MC14069UB
- For Greater Hysteresis, Use MC14106B which is Pin-for-Pin Replacement for CD40106B and MM74C14



L SUFFIX
CERAMIC
CASE 632



P SUFFIX
PLASTIC
CASE 646



D SUFFIX
SOIC
CASE 751A

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V _{DD}	DC Supply Voltage	-0.5 to +18.0	V
V _{in} , V _{out}	Input or Output Voltage (DC or Transient)	-0.5 to V _{DD} + 0.5	V
I _{in} , I _{out}	Input or Output Current (DC or Transient), per Pin	± 10	mA
P _D	Power Dissipation, per Package†	500	mW
T _{stg}	Storage Temperature	-65 to +150	°C
T _L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating, Plastic "P and D/DW" Packages: -7.0 mW/°C From 65°C To 125°C
Ceramic "L" Packages: -12 mW/°C From 100°C To 125°C

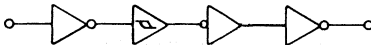
ORDERING INFORMATION

MC14XXBCP Plastic
MC14XXBCL Ceramic
MC14XXBD SOIC

T_A = -55° to 125°C for all packages.

6

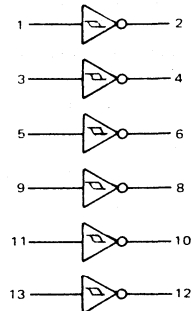
EQUIVALENT CIRCUIT SCHEMATIC (1/6 OF CIRCUIT SHOWN)



This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range V_{SS} ≤ (V_{in} or V_{out}) ≤ V_{DD}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

LOGIC DIAGRAM



V_{DD} = Pin 14
V_{SS} = Pin 7

MC14584B

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V _{DD} Vdc	-55°C		25°C			125°C		Unit
			Min	Max	Min	Typ #	Max	Min	Max	
Output Voltage "0" Level V _{in} = V _{DD}	V _{OL}	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
		10	—	0.05	—	0	0.05	—	0.05	
V _{in} = 0 "1" Level	V _{OH}	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc
		10	9.95	—	9.95	10	—	9.95	—	
Output Drive Current (V _{OH} = 2.5 Vdc) (V _{OH} = 4.6 Vdc) (V _{OH} = 9.5 Vdc) (V _{OH} = 13.5 Vdc)	Source I _{OH}	5.0	-3.0	—	-2.4	-4.2	—	-1.7	—	mAdc
		10	-0.64	—	-0.51	-0.88	—	-0.36	—	
(V _{OL} = 0.4 Vdc) (V _{OL} = 0.5 Vdc) (V _{OL} = 1.5 Vdc)	Sink I _{OL}	5.0	0.64	—	0.51	0.88	—	0.36	—	mAdc
		10	1.6	—	1.3	2.25	—	0.9	—	
15	4.2	—	3.4	8.8	—	2.4	—	—		
Input Current	I _{in}	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	μAdc
Input Capacitance (V _{in} = 0)	C _{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)	I _{DD}	5.0	—	0.25	—	0.0005	0.25	—	7.5	μAdc
		10	—	0.5	—	0.0010	0.5	—	15	
		15	—	1.0	—	0.0015	1.0	—	30	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C _L = 50 pF on all outputs, all buffers switching)	I _T	5.0	I _T = (1.8 μA/kHz) f + I _{DD}							μAdc
		10	I _T = (3.6 μA/kHz) f + I _{DD}							
		15	I _T = (5.4 μA/kHz) f + I _{DD}							
Hysteresis Voltage	V _{H‡}	5.0	0.27	1.0	0.25	0.6	1.0	0.21	1.0	Vdc
		10	0.36	1.3	0.3	0.7	1.2	0.25	1.2	
		15	0.77	1.7	0.6	1.1	1.5	0.50	1.4	
Threshold Voltage Positive-Going	V _{T+}	5.0	1.9	3.5	1.8	2.7	3.4	1.7	3.4	Vdc
		10	3.4	7.0	3.3	5.3	6.9	3.2	6.9	
		15	5.2	10.6	5.2	8.0	10.5	5.2	10.5	
Negative-Going	V _{T-}	5.0	1.6	3.3	1.6	2.1	3.2	1.5	3.2	Vdc
		10	3.0	6.7	3.0	4.6	6.7	3.0	6.7	
		15	4.5	9.7	4.6	6.9	9.8	4.7	9.9	

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) Vfk$$

where: I_T is in μA (per package), C_L in pF, V = (V_{DD} - V_{SS}) in volts, f in kHz is input frequency, and k = 0.001.

‡V_H = V_{T+} - V_{T-} (But maximum variation of V_H is specified as less than V_{T+} max - V_{T-} min).

MC14584B

SWITCHING CHARACTERISTICS (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V _{DD} Vdc	Min	Typ #	Max	Unit
Output Rise Time	t _{TLH}	5.0	—	100	200	ns
		10	—	50	100	
		15	—	40	80	
Output Fall Time	t _{THL}	5.0	—	100	200	ns
		10	—	50	100	
		15	—	40	80	
Propagation Delay Time	t _{PLH} , t _{PHL}	5.0	—	125	250	ns
		10	—	50	100	
		15	—	40	80	

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

FIGURE 1 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

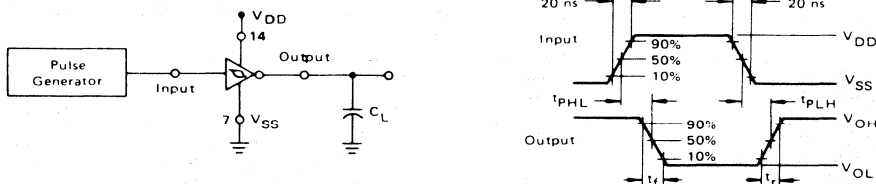


FIGURE 2 – TYPICAL SCHMITT TRIGGER APPLICATIONS

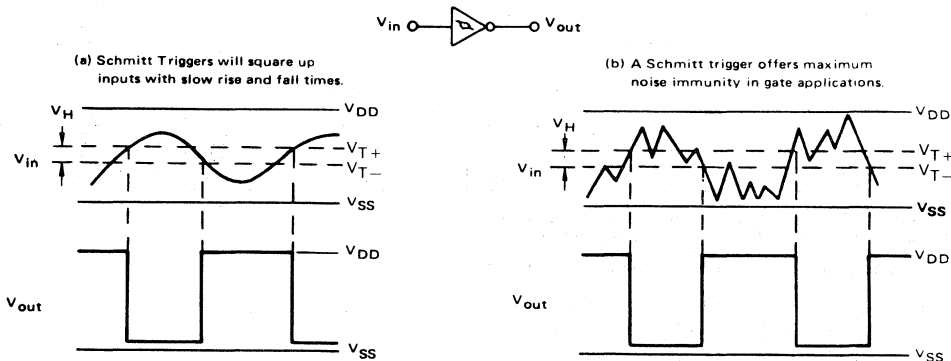
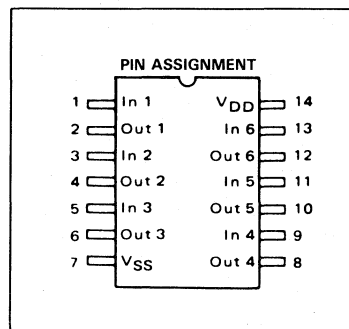
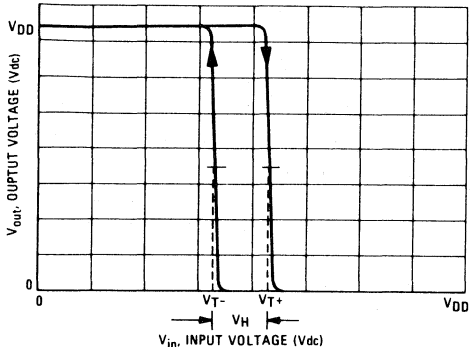


FIGURE 3 – TYPICAL TRANSFER CHARACTERISTICS





MOTOROLA

MC14585B

4-BIT MAGNITUDE COMPARATOR

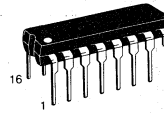
The MC14585B 4-Bit Magnitude Comparator is constructed with complementary MOS (CMOS) enhancement mode devices. The circuit has eight comparing inputs (A3, B3, A2, B2, A1, B1, A0, B0), three cascading inputs (A<B, A=B, and A>B), and three outputs (A<B, A=B, and A>B). This device compares two 4-bit words (A and B) and determines whether they are "less than", "equal to", or "greater than" by a high level on the appropriate output. For words greater than 4-bits, units can be cascaded by connecting outputs (A>B), (A<B), and (A=B) to the corresponding inputs of the next significant comparator. Inputs (A<B), (A=B), and (A>B) on the least significant (first) comparator are connected to a low, a high, and a low, respectively.

Applications include logic in CPU's, correction and/or detection of instrumentation conditions, comparator in testers, converters, and controls.

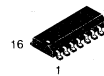
- Diode Protection on All Inputs
- Expandable
- Applicable to Binary or 8421-BCD Code
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load over the Rated Temperature Range
- Can be Cascaded - See Fig. 3



L SUFFIX
CERAMIC
CASE 620



P SUFFIX
PLASTIC
CASE 648



D SUFFIX
SOIC
CASE 751B

ORDERING INFORMATION

MC14XXXBCP Plastic
MC14XXXBCL Ceramic
MC14XXXBD SOIC

T_A = -55° to 125°C for all packages.

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V _{DD}	DC Supply Voltage	-0.5 to +18.0	V
V _{in} , V _{out}	Input or Output Voltage (DC or Transient)	-0.5 to V _{DD} +0.5	V
I _{in} , I _{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
P _D	Power Dissipation, per Package†	500	mW
T _{stg}	Storage Temperature	-65 to +150	°C
T _L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.

†Temperature Derating: Plastic "P and D/DW" Packages: -7.0 mW/°C From 65°C to 125°C

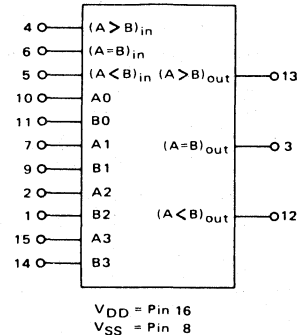
Ceramic "L" Packages: -12 mW/°C From 100°C to 125°C

TRUTH TABLE

COMPARING INPUTS				CASCADING			OUTPUTS		
A3, B3	A2, B2	A1, B1	A0, B0	A<B	A=B	A>B	A<B	A=B	A>B
A3>B3	x	x	x	x	x	x	0	0	1
A3=B3	A2>B2	x	x	x	x	x	0	0	1
A3=B3	A2=B2	A1>B1	x	x	x	x	0	0	1
A3=B3	A2=B2	A1=B1	A0>B0	x	x	x	0	0	1
A3=B3	A2=B2	A1=B1	A0=B0	0	0	x	0	0	1
A3=B3	A2=B2	A1=B1	A0=B0	0	1	x	0	1	0
A3=B3	A2=B2	A1=B1	A0=B0	1	0	x	1	0	0
A3=B3	A2=B2	A1=B1	A0=B0	1	1	x	1	1	0
A3=B3	A2=B2	A1=B1	A0<B0	x	x	x	1	0	0
A3=B3	A2=B2	A1<B1	x	x	x	x	1	0	0
A3=B3	A2<B2	x	x	x	x	x	1	0	0
A3<B3	x	x	x	x	x	x	1	0	0

x = Don't Care

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

MC14585B

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V _{DD} Vdc	-55°C		25°C			125°C		Unit	
			Min	Max	Min	Typ #	Max	Min	Max		
Output Voltage V _{in} = V _{DD} or 0	V _{OL}	5.0	—	0.05	—	0	0.05	—	0.05	Vdc	
		10	—	0.05	—	0	0.05	—	0.05		
		15	—	0.05	—	0	0.05	—	0.05		
V _{in} = 0 or V _{DD}	V _{OH}	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc	
		10	9.95	—	9.95	10	—	9.95	—		
		15	14.95	—	14.95	15	—	14.95	—		
Input Voltage (V _O = 4.5 or 0.5 Vdc) (V _O = 9.0 or 1.0 Vdc) (V _O = 13.5 or 1.5 Vdc)	V _{IL}	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc	
		10	—	3.0	—	4.50	3.0	—	3.0		
		15	—	4.0	—	6.75	4.0	—	4.0		
	V _{IH}	5.0	3.5	—	3.5	2.75	—	3.5	—	Vdc	
		10	7.0	—	7.0	5.50	—	7.0	—		
		15	11	—	11	8.25	—	11	—		
Output Drive Current (V _{OH} = 2.5 Vdc) (V _{OH} = 4.6 Vdc) (V _{OH} = 9.5 Vdc) (V _{OH} = 13.5 Vdc)	Source	I _{OH}	5.0	-3.0	—	-2.4	-4.2	—	-1.7	—	mA _{dc}
			10	-0.64	—	-0.51	-0.88	—	-0.36	—	
			15	-1.6	—	-1.3	-2.25	—	-0.9	—	
	Sink	I _{OL}	5.0	0.64	—	0.51	0.88	—	0.36	—	mA _{dc}
			10	1.6	—	1.3	2.25	—	0.9	—	
			15	4.2	—	3.4	8.8	—	2.4	—	
Input Current	I _{in}	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	μA _{dc}	
Input Capacitance (V _{in} = 0)	C _{in}	—	—	—	—	5.0	7.5	—	—	pF	
Quiescent Current (Per Package)	I _{DD}	5.0	—	5.0	—	0.005	5.0	—	150	μA _{dc}	
		10	—	10	—	0.010	10	—	300		
		15	—	20	—	0.015	20	—	600		
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C _L = 50 pF on all outputs, all buffers switching)	I _T	5.0	I _T = (0.6 μA/kHz) f + I _{DD}							μA _{dc}	
		10	I _T = (1.2 μA/kHz) f + I _{DD}								
		15	I _T = (1.8 μA/kHz) f + I _{DD}								

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

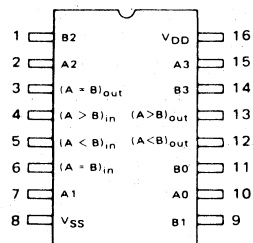
**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) V/fk$$

where: I_T is in μA (per package), C_L in pF, V = (V_{DD} - V_{SS}) in volts, f in kHz is input frequency, and k = 0.001.

PIN ASSIGNMENT



MC14585B

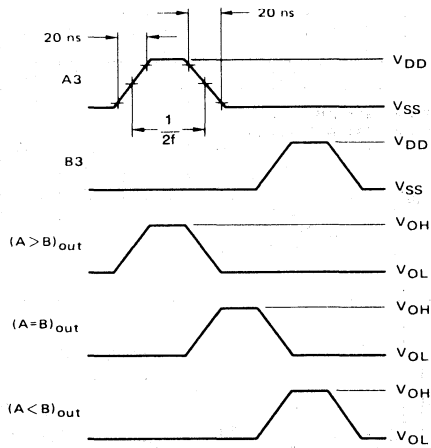
SWITCHING CHARACTERISTICS* ($C_L = 50 \text{ pF}$, $T_A = 25^\circ\text{C}$)

Characteristic	Symbol	V_{DD}	Min	Typ #	Max	Unit
Output Rise and Fall Time						ns
t_{TLH} , $t_{THL} = (1.5 \text{ ns/pF}) C_L + 25 \text{ ns}$	t_{TLH} , t_{THL}	5.0	—	100	200	
t_{TLH} , $t_{THL} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$		10	—	50	100	
t_{TLH} , $t_{THL} = (0.55 \text{ ns/pF}) C_L + 9.5 \text{ ns}$		15	—	40	80	
Turn-On, Turn-Off Delay Time						ns
t_{PLH} , $t_{PHL} = (1.7 \text{ ns/pF}) C_L + 345 \text{ ns}$	t_{PLH} , t_{PHL}	5.0	—	430	860	
t_{PLH} , $t_{PHL} = (0.66 \text{ ns/pF}) C_L + 147 \text{ ns}$		10	—	180	360	
t_{PLH} , $t_{PHL} = (0.5 \text{ ns/pF}) C_L + 105 \text{ ns}$		15	—	130	260	

*The formulas given are for the typical characteristics only at 25°C.

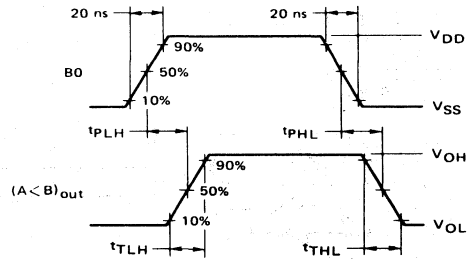
#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

FIGURE 1 – DYNAMIC POWER DISSIPATION SIGNAL WAVEFORMS



Inputs (A > B) and (A = B) high, and inputs B2, A2, B1, A1, B0, A0 and (A < B) low.
f in respect to a system clock.

FIGURE 2 – DYNAMIC SIGNAL WAVEFORMS

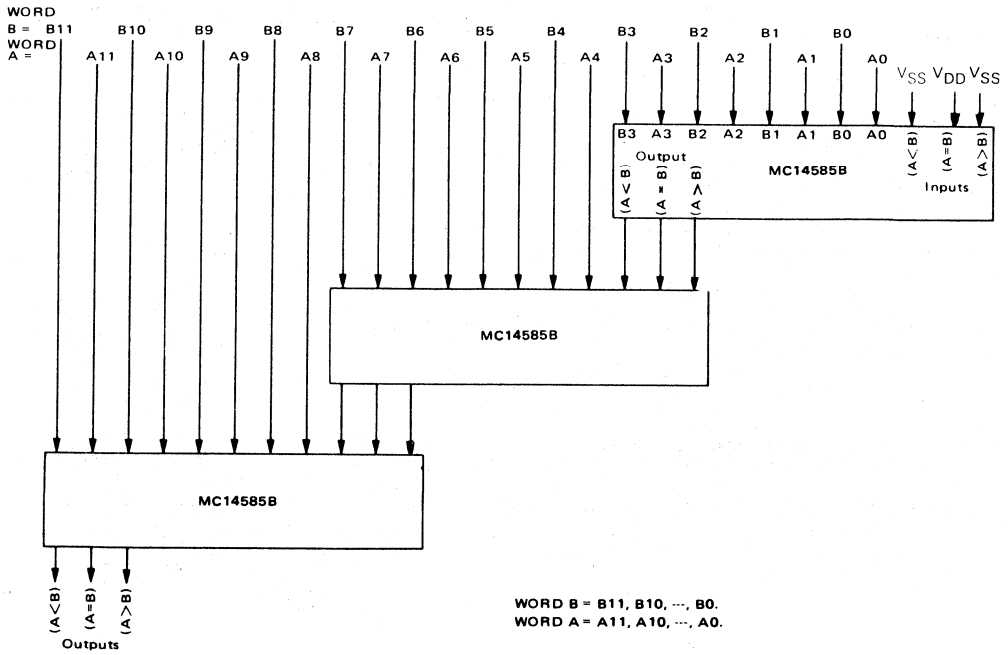


Inputs (A > B) and (A = B) high, and inputs B3, A3, B2, A2, B1, A1, A0, and (A < B) low.

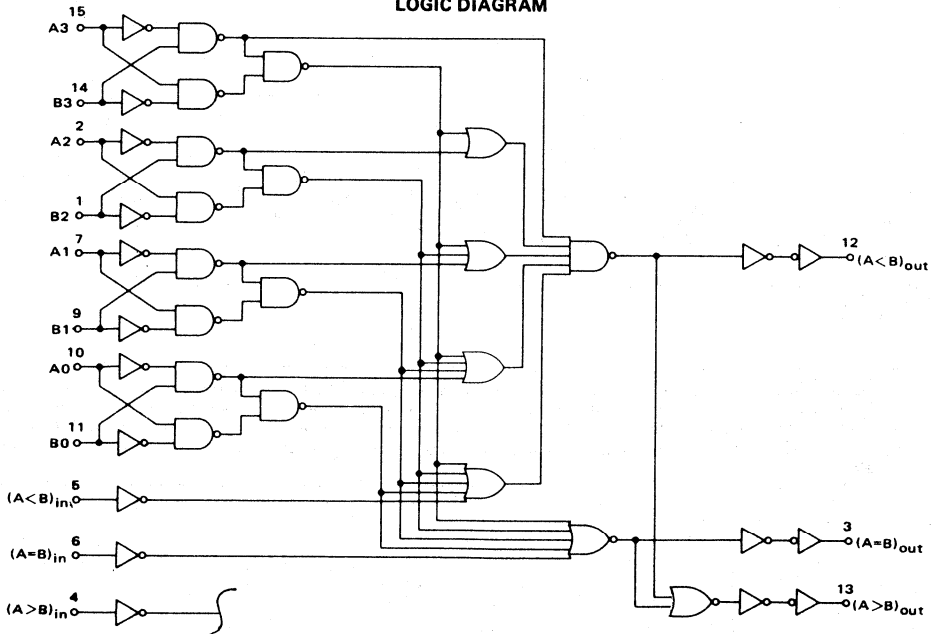
This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

MC14585B

FIGURE 3 – CASCADING COMPARATORS



LOGIC DIAGRAM



6



MOTOROLA

MC14599
See Page 6-174

MC14597B
MC14598B

8-BIT BUS-COMPATIBLE LATCHES

The MC14597B and MC14598B are 8-bit latches, one addressed with an internal counter and the other addressed with an external binary address. The 8 latch-outputs are high drive, three-state and bus line compatible. The drive capability allows direct applications with MPU systems such as the Motorola 6800 family.

With MC14597B, a 3-bit address counter (clocked on the falling edge of Increment) selects the appropriate latch. The latches of the MC14598B are accessed via the Address pins, A0, A1, and A2. A Full Flag is provided on the MC14597B to indicate the position of the Address counter.

All 8 outputs from the latches are available in parallel when Enable is in the low state. Data is entered into a selected latch from the Data pin when the Strobe is high. Master reset is available on both parts.

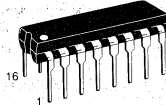
- Serial Data Input
- Three-State Bus Compatible Parallel Outputs
- Three-State Control Pin (Enable) TTL Compatible Input
- Open Drain Full Flag (Multiple Latch Wire-O Ring)
- Master Reset
- Level Shifting Inputs on All Except Enable
- Diode Protection – All Inputs
- Supply Voltage Range – 3.0 Vdc to 18 Vdc
- Capable of Driving TTL Over Rated Temperature Range

With Fanout as Follows:

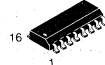
- 1 TTL Load
- 4 LSTTL Loads



L SUFFIX
CERAMIC
CASE 620



P SUFFIX
PLASTIC
CASE 648

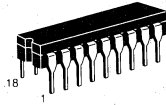


D SUFFIX
SOIC
CASE 751B

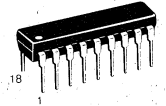
ORDERING INFORMATION

- MC14597BCP Plastic
- MC14597BCL Ceramic
- MC14597BDW SOIC

T_A = -55°C to +125°C for all packages.



L SUFFIX
CERAMIC PACKAGE
CASE 726



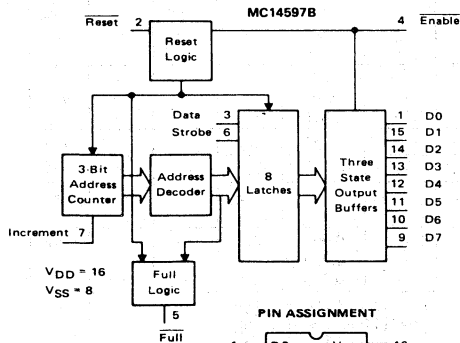
P SUFFIX
PLASTIC PACKAGE
CASE 707

ORDERING INFORMATION

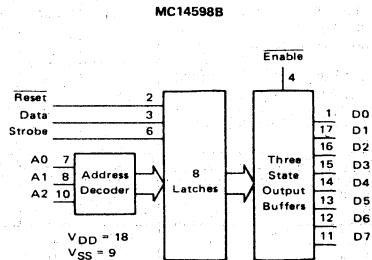
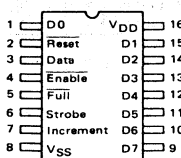
- MC14598BCP Plastic
- MC14598BCL Ceramic

T_A = -55°C to +125°C for all packages.

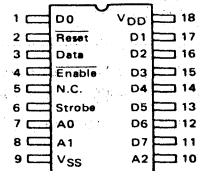
BLOCK DIAGRAMS



PIN ASSIGNMENT



PIN ASSIGNMENT



OUTPUT TRUTH TABLE

Enable	Outputs
1	High Impedance
0	D _n

D_n = State of nth latch
NC = No Connection

6

MC14597B•MC14598B

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V _{DD}	DC Supply Voltage	-0.5 to +18.0	V
V _{in}	Input Voltage, Enable (DC or Transient)	-0.5 to V _{DD} + 0.5	V
V _{in}	Input Voltage, All other Inputs (DC or Transient)	-0.5 to V _{DD} + 12	V
V _{out}	Output Voltage (DC or Transient)	-0.5 to V _{DD} + 0.5	V
I _{in} , I _{out}	Input or Output Current (DC or Transient), per Pin	± 10	mA
P _D	Power Dissipation, per Package†	500	mW
T _{stg}	Storage Temperature	-65 to +150	°C
T _L	Lead Temperature (8-Second Soldering)	260	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range V_{SS} ≤ (V_{in} or V_{out}) ≤ V_{DD}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

*Maximum Ratings are those values beyond which damage to the device may occur.

†Temperature Derating: Plastic "P and D/DW" Packages: -7.0 mW/°C From 65°C To 125°C
Ceramic "L" Packages: -12 mW/°C From 100°C To 125°C

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V _{DD} Vdc	-55°C		25°C			125°C		Unit
			Min	Max	Min	Typ #	Max	Min	Max	
Output Voltage V _{in} = V _{DD} or 0 V _{in} = 0 or V _{DD}	"0" Level V _{OL}	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
		10	—	0.05	—	0	0.05	—	0.05	
		15	—	0.05	—	0	0.05	—	0.05	
	"1" Level V _{OH}	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc
		10	9.95	—	9.95	10	—	9.95	—	
		15	14.95	—	14.95	15	—	14.95	—	
Input Voltage** — Enable (V _O = 4.5 or 0.5 Vdc) (V _O = 9.0 or 1.0 Vdc) (V _O = 13.5 or 1.5 Vdc) (V _O = 0.5 or 4.5 Vdc) (V _O = 1.0 or 9.0 Vdc) (V _O = 1.5 or 13.5 Vdc)	"0" Level V _{IL}	5.0	—	0.8	—	1.1	0.8	—	0.8	Vdc
		10	—	1.6	—	2.2	1.6	—	1.6	
		15	—	2.4	—	3.4	2.4	—	2.4	
	"1" Level V _{IH}	5.0	2.0	—	2.0	1.9	—	2.0	—	Vdc
		10	6.0	—	6.0	3.1	—	6.0	—	
		15	10	—	10	4.3	—	10	—	
Input Voltage Other Inputs (V _O = 4.5 or 0.5 Vdc) (V _O = 9.0 or 1.0 Vdc) (V _O = 13.5 or 1.5 Vdc) (V _O = 0.5 or 4.5 Vdc) (V _O = 1.0 or 9.0 Vdc) (V _O = 1.5 or 13.5 Vdc)	"0" Level V _{IL}	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc
		10	—	3.0	—	4.50	3.0	—	3.0	
		15	—	4.0	—	6.75	4.0	—	4.0	
	"1" Level V _{IH}	5.0	3.5	—	3.5	2.75	—	3.5	—	Vdc
		10	7.0	—	7.0	5.50	—	7.0	—	
		15	11	—	11	8.25	—	11	—	
Output Drive Current (Full — Sink Only) (V _{OH} = 4.6 Vdc) (V _{OH} = 9.5 Vdc) (V _{OH} = 13.5 Vdc) (V _{OL} = 0.4 Vdc) (V _{OL} = 0.5 Vdc) (V _{OL} = 1.5 Vdc)	Source I _{OH}	5.0	-1.0	—	-1.0	-2.0	—	-1.0	—	mAdc
		10	—	—	—	-6.0	—	—	—	
		15	—	—	—	-12	—	—	—	
	Sink I _{OL}	5.0	1.6	—	1.6	3.2	—	1.6	—	mAdc
		10	—	—	—	6.0	—	—	—	
		15	—	—	—	12	—	—	—	
Input Current	I _{in}	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	μAdc
Three-State Leakage Current	I _{TL}	15	—	±0.1	—	±0.00001	±0.1	—	±3.0	μAdc
Input Capacitance (V _{in} = 0)	C _{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)	I _{DD}	5.0	—	5.0	—	0.005	5.0	—	150	μAdc
		10	—	10	—	0.010	10	—	300	
		15	—	20	—	0.015	20	—	600	
**Total Supply Current at an External Load Capacitance of 130 pF	I _T	5.0	I _T = (2.0 μA/kHz) f + I _{DD} I _T = (4.0 μA/kHz) f + I _{DD} I _T = (6.0 μA/kHz) f + I _{DD}					10	μAdc	

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C.

MC14597B•MC14598B

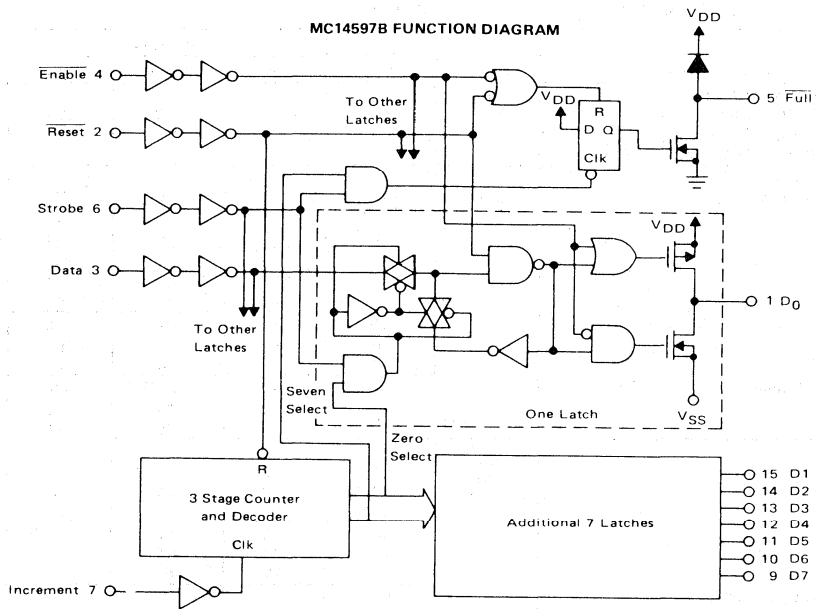
SWITCHING CHARACTERISTICS* ($T_A = 25^\circ\text{C}$, $C_L = 130\text{ pF} + 1\text{ TTL Load}$)

Characteristic	Symbol	V _{DD} Vdc	All Types			Unit
			Min	Typ #	Max	
Output Rise and Fall Time $t_{TLH}, t_{THL} = (0.5\text{ ns/pF})C_L + 35\text{ ns}$ $t_{TLH}, t_{THL} = (0.2\text{ ns/pF})C_L + 25\text{ ns}$ $t_{TLH}, t_{THL} = (0.16\text{ ns/pF})C_L + 20\text{ ns}$	$t_{TLH},$ t_{THL}	5.0 10 15	— — —	100 50 40	200 100 80	ns
Propagation Delay Time Enable to Output	$t_{PLH},$ t_{PHL}	5.0 10 15	— — —	160 125 100	320 250 200	ns
Strobe to Output		5.0 10 15	— — —	200 100 80	400 200 160	
Strobe to Full (MC14597B only)		5.0 10 15	— — —	200 100 80	400 200 160	
Reset to Output		5.0 10 15	— — —	175 90 70	350 180 140	
Pulse Width Enable	$t_{WH},$ t_{WL}	5.0 10 15	320 240 160	160 120 80	— — —	ns
Strobe		5.0 10 15	200 100 80	100 50 40	— — —	
Increment (MC14597B only)		5.0 10 15	200 100 80	100 50 40	— — —	
Reset		5.0 10 15	300 160 100	150 80 50	— — —	
Setup Time Data	t_{su}	5.0 10 15	100 50 35	50 25 20	— — —	ns
Address (MC14598B only)		5.0 10 15	200 100 70	100 50 35	— — —	
Increment (MC14597B only)		5.0 10 15	400 200 170	200 100 85	— — —	
Hold Time Data	t_h	5.0 10 15	100 50 35	50 25 20	— — —	ns
Address (MC14598B only)		5.0 10 15	100 50 35	50 25 20	— — —	
Reset Removal Time	t_{rem}	5.0 10 15	20 20 20	-25 -15 -10	— — —	ns

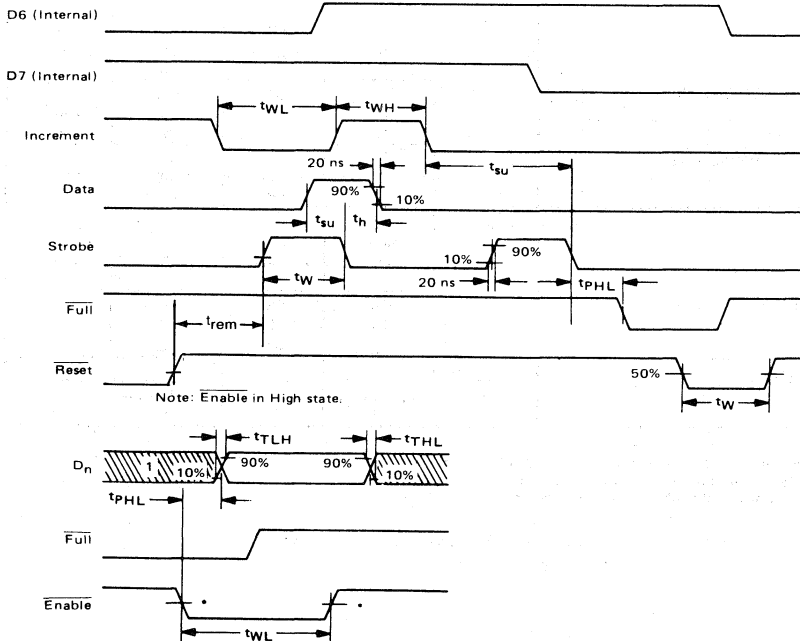
*The formulas given are for the typical characteristics only at 25°C.
#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

6

MC14597B•MC14598B



MC14597B TIMING DIAGRAMS

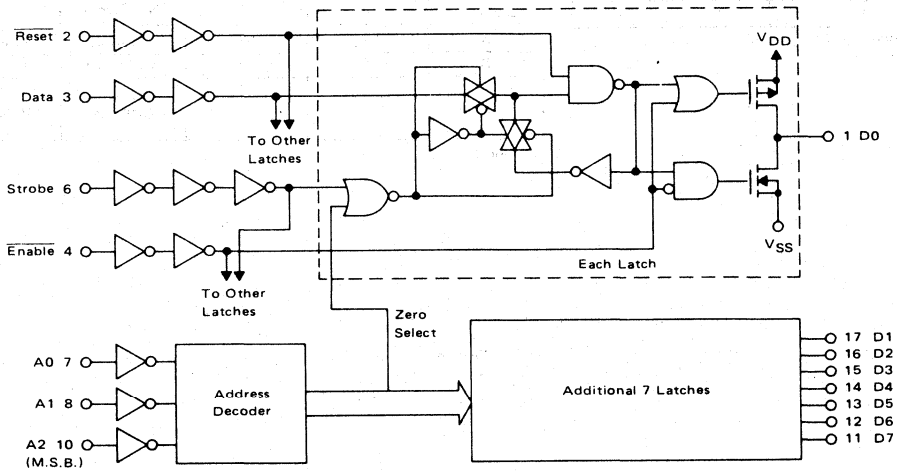


* 1.4 V with $V_{DD} = 5.0$ V

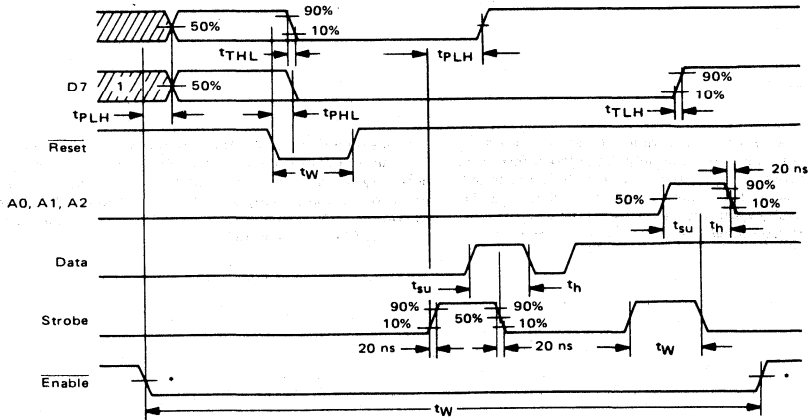
- NOTES: 1. High-impedance output state (another device controls bus).
2. Reset in High state.

MC14597B•MC14598B

MC14598B FUNCTION DIAGRAM



MC14598B TIMING DIAGRAM



* 1.4 V with $V_{DD} = 5.0$ V.

- NOTES 1. High-impedance output state (another device controls bus).
2. Output Load as for MC14597B.

MC14597B•MC14598B



LATCH TRUTH TABLE

Strobe	Reset	Addressed Latch	Other Latches
0	1	*	*
1	1	Data	*
X	0	0	0

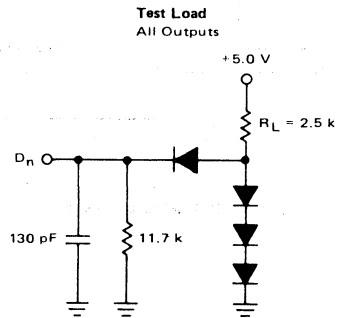
* = No change in state of latch

X = Don't care

TRUTH TABLE FOR MC14597B

Increment	Enable	Reset	Address Counter	Full
	X	1	Count Up	—
	X	1	No Change	—
X	1	0	Reset to Zero	Set to One
X	0	1	No Change	Set to One
X	1	1	If at ADDRESS 7	To Zero on Falling Edge of STROBE

X = Don't care



6

Circuit diagrams external to or containing Motorola products are included as a means of illustration only. Complete information sufficient for construction purposes may not be fully illustrated. Although the information herein has been carefully checked and is believed to be reliable, Motorola assumes no responsibility for inaccuracies. Information herein does not convey to the purchaser

any license under the patent rights of Motorola or others.

The information contained herein is for guidance only, with no warranty of any type, expressed or implied. Motorola reserves the right to make any changes to the information and the product(s) to which the information applies and to discontinue manufacture of the product(s) at any time.



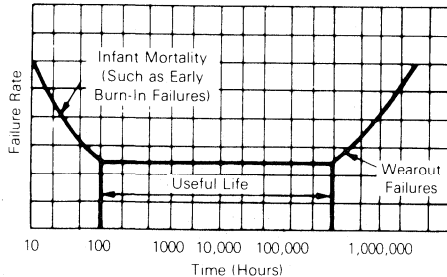
RELIABILITY

Paramount in the mind of every semiconductor user is the question of device performance versus time. After the applicability of a particular device has been established, its effectiveness depends on the length of troublefree service it can offer. The reliability of a device is exactly that — an expression of how well it will serve the customer. The following discussion will attempt to present an overview of Motorola's reliability efforts.

BASIC CONCEPTS

It is essential to begin with an explanation of the various parameters of Reliability. These are probably summarized best in the Bathtub Curve (Figure 1). The reliability performance of a device is characterized by three phases: infant mortality, useful life, and wearout. When a device is produced, there is often a small distribution of failure mechanisms which will exhibit themselves under relatively moderate stress levels and therefore appear early. This period of early failures, termed infant mortality is reduced significantly through proper manufacturing controls and screening techniques. The most effective period is that in which only occasional random failure mechanisms appear. The useful life typically spans a long period of time with a very low failure rate. The final period is that in which the devices literally wear out due to continuous phenomena which existed at the time of manufacture. Using strictly controlled design techniques and selectivity in applications, this period is shifted well beyond the lifetime required by the user.

FIGURE 1



7

Both the infant mortality and random failure rate regions can be described through the same types of calculations. During this time the probability of having no failures to a specific point in time can be expressed by the equation:

$$P_0 = e^{-\lambda t}$$

where λ is the failure rate and t is time. Since λ is changing rapidly during infant mortality, the expression does not become useful until the random period, where λ is relatively constant. In this equation λ is failures per unit of time. It is usually expressed in percent failures per thousand hours. Other forms include FIT (Failures in Time = $(\% \times 10^3 \text{ hrs}) \times 10^{-4} = 10^{-9}$ failures per hour) and MTTF (Mean Time To Failure) or MTBF (Mean Time Between Failures), both being equal to $1/\lambda$ and having units of hours.

Since reliability evaluations usually involve only samples of an entire population of devices, the concepts of the Central Limit Theorem apply and λ is calculated using χ^2 distribution through the equation:

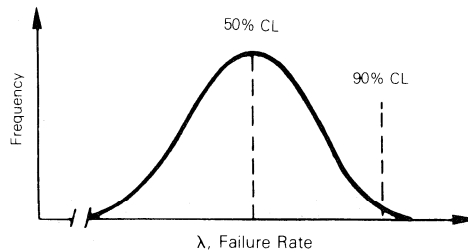
$$\lambda \leq \frac{\chi^2(x, 2r + 2)}{2nt}$$

$$\text{where } x = \frac{100 - CL}{100}$$

- CL = Confidence Limit in percent
- r = Number of rejects
- n = Number of devices
- t = Duration of test

The confidence limit is the degree of conservatism desired in the calculation. The Central Limit Theorem states that the values of any sample of units out of a large population will produce a normal distribution. A 50% confidence limit is termed the best estimate and is the mean of this distribution. A 90% confidence limit is a very conservative value and results in a higher λ which represents the point at which 90% of the area of the distribution is to the left of that value (Figure 2). The term $(2r + 2)$ is called the degrees of freedom and is an expression of the number of rejects in a form suitable to χ^2 tables.

FIGURE 2



The number of rejects is a critical factor since the definition of rejects often differs between manufacturers. While Motorola uses data sheet limits to determine failures, sometimes rejects are counted only if they are catastrophic. Due to the increasing chance of a test not being representative of the entire population, as sample size and test time are decreased, the χ^2 calculation produces surprisingly high values of λ for short test durations even though the true long term failure rate may be quite low. For this reason relatively large amounts of data must be gathered to demonstrate the real long term failure rate.

Since this would require years of testing on thousands of devices, methods of accelerated testing have been developed.

Years of semiconductor device testing has shown that temperature will accelerate failures and that this behavior fits the form of the Arrhenius equation:

$$R(t) = R_0(t)e^{-\Theta/kT}$$

where $R(t)$ = Reaction rate as a function of time and temperature

- R_0 = A constant
- t = Time
- Θ = Activation energy in electron volts
- k = Boltzman's constant
- T = Temperature in degrees Kelvin

To provide time-temperature equivalents this equation is applied to failure rate calculations in the form:

$$t = t_0 e^{\Theta/kT}$$

where t = time

$$t_0 = A \text{ constant}$$

The Arrhenius equation essentially states that reaction rate increases exponentially with temperature. This produces a straight line when plotted in log-linear paper with a slope expressed by Θ . Θ may be physically interpreted as the energy threshold of a particular reaction or failure mechanism. The activation energy exhibited by semiconductors varies from about 0.3 eV. Although the relationships do not prohibit devices from having poor failure rates and high activation energies, good performance usually does not imply a high Θ . Studies by Bell Telephone Laboratories have indicated that an overall Θ for semiconductors is 1.0 eV. This value has been accepted by the Rome Air Development Command for time-temperature acceleration in powered burn-in. Data taken by Motorola on Integrated Circuits have verified this number and it is therefore applied as our standard time-temperature regression for extrapolation of high temperature failure rates to temperatures at which the devices will be used (Figure 3). For Discrete products, 0.7 eV is generally applied.

To accomplish this, the time in device hours (t_1) and temperature (T_1) of the test are plotted as point P1. A vertical line is drawn at the temperature of interest (T_2) and a line with a 1.0 eV slope is drawn through point P1.

Its intersection with the vertical line defines point P2, and determines the number of equivalent device hours (t_2). This number may then be used with the x^2 formula to determine the failure rate at the temperature of interest. Assuming T_1 of 125°C at t_1 of 10,000 hours, a t_2 of 7.8 million hours results at a T_2 of 50°C. If one reject results in the 10,000 device hours of testing at 125°C, the failure rate at that temperature will be 0.1%/1,000 hours using a 60% confidence level. One reject at the equivalent 7.8 million device hours at 50°C will result in a 0.0008%/1,000 hour failure rate, as illustrated in Figure 4.

Three parameters determine the failure rate quoted by the manufacturer: the failure rate at the test temperature, the activation energy employed, and the difference between the test temperature and the temperature of the quoted λ . A term often used in this manipulation is the "acceleration factor" which is simply the equivalent device hours at the lower temperature divided by the actual test device hours.

Every device will eventually fail, but with the present techniques in Semiconductor design and applications, the wearout phase is extended far beyond the lifetime required. During wearout, as in infant mortality, the failure rate is changing rapidly and therefore loses its value. The parameter used to describe performance in this area is "Median Life" and is the point at which 50% of the devices have failed. There are currently only few significant wearout mechanisms: electromigration of circuit metallization, electrolytic corrosion in plastic devices and metal fatigue for Power devices.

FIGURE 3
NORMALIZED TIME-TEMPERATURE
REGRESSIONS FOR VARIOUS ACTIVATION
ENERGY VALUES

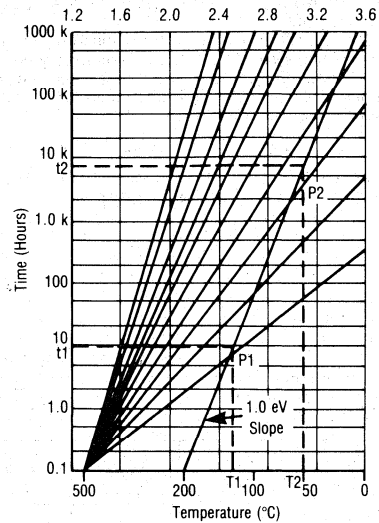
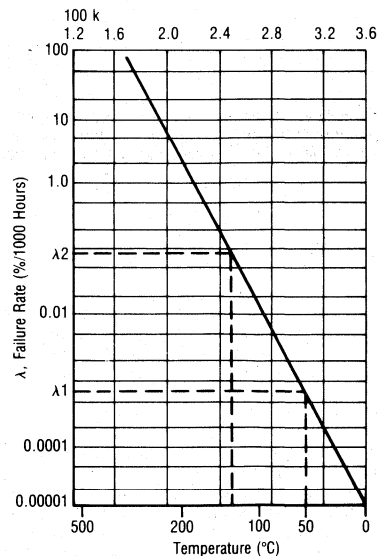


FIGURE 4
FAILURE RATE



For increased flexibility in working with a broad range of device hours, the time-temperature regression lines have been normalized to 500°C and the time scale omitted, permitting the user to define the scale based on his own requirements.

THERMAL MANAGEMENT

Circuit performance and long-term circuit reliability are affected by die temperature. Normally, both are improved by keeping the IC junction temperatures low.

Electrical power dissipated in any integrated circuit is a source of heat. This heat source increases the temperature of the die relative to some reference point, normally the ambient temperature of 25°C in still air. The temperature increase, then, depends on the amount of power dissipated in the circuit and on the net thermal resistance between the heat source and the reference point.

The temperature at the junction is a function of the packaging and mounting system's ability to remove heat generated in the circuit — from the junction region to the ambient environment. The basic formula for converting power dissipation to estimated junction temperature is:

$$T_J = T_A + P_D(\bar{\theta}_{JC} + \bar{\theta}_{CA}) \quad (1)$$

or

$$T_J = T_A + P_D(\bar{\theta}_{JA}) \quad (2)$$

where

T_J = maximum junction temperature

T_A = maximum ambient temperature

P_D = calculated maximum power dissipation including effects of external loads (see Power Dissipation in section III).

$\bar{\theta}_{JC}$ = average thermal resistance, junction to case

$\bar{\theta}_{CA}$ = average thermal resistance, case to ambient

$\bar{\theta}_{JA}$ = average thermal resistance, junction to ambient

This Motorola recommended formula has been approved by RADC or DESC for calculating a "practical" maximum operating junction temperature for MIL-M-38510 (JAN) devices.

Only two terms on the right side of equation (1) can be varied by the user — the ambient temperature, and the device case-to-ambient thermal resistance, $\bar{\theta}_{CA}$. (To some extent the device power dissipation can also be controlled, but under recommended use the V_{CC} supply and loading dictate a fixed power dissipation.) Both system air flow and the package mounting technique affect the $\bar{\theta}_{CA}$ thermal resistance term. $\bar{\theta}_{JC}$ is essentially independent of air flow and external mounting method, but is sensitive to package material, die bonding method, and die area.

FIGURE 5 — THERMAL RESISTANCE VALUES FOR STANDARD I/C PACKAGES

Thermal Resistance in Still Air								
Package Description								
No. Leads	Body Style	Body Material	Body W x L	Die Bonds	Die Area (Sq. Mills)	Flag Area (Sq. Mills)	$\bar{\theta}_{JC}$ (°C/Watt)	
							Avg.	Max.
14	DIL	Epoxy	1/4" x 3/4"	Epoxy	4096	6,400	38	61
16	DIL	Epoxy	1/4" x 3/4"	Epoxy	4096	12,100	34	54

NOTES:

1. All plastic packages use copper lead frames.
2. Body style DIL is "Dual-In-Line."
3. Standard Mounting Method: Dual-In-Line Socket or P/C board with no contact between bottom of package and socket or P/C board.

For applications where the case is held at essentially a fixed temperature by mounting on a large or temperature-controlled heat sink, the estimated junction temperature is calculated by:

$$T_J = T_C + P_D(\bar{\theta}_{JC}) \quad (3)$$

where T_C = maximum case temperature and the other parameters are as previously defined.

The maximum and average $\bar{\theta}_{JC}$ resistance values for standard IC packages are given in Figure 5.

AIR FLOW

The majority of users employ some form of air-flow cooling. As air passes over each device on a printed circuit board, it absorbs heat from each package. This heat gradient from the first package to the last package is a function of the air flow rate and individual package dissipations. Figure 7 provides gradient data at power levels of 200 mW, 250 mW, 300 mW, and 400 mW with an air flow rate of 500 lfm. These figures show the proportionate increase in the junction temperature of each dual in-line package as the air passes over each device. For higher rates of air flow the change in junction temperature from package to package down the airstream will be lower due to greater cooling.

FIGURE 7 — THERMAL GRADIENT OF JUNCTION TEMPERATURE (16-PIN DUAL-IN-LINE PACKAGE)

Power Dissipation (mW)	Junction Temperature Gradient (°C/Package)
200	0.4
250	0.5
300	0.63
400	0.88

Devices mounted on 0.062" PC board with Z axis spacing of 0.5". Air flow is 500 lfm along the Z axis.

OPTIMIZING THE LONG TERM RELIABILITY OF PLASTIC PACKAGES

Today's plastic integrated circuit packages are as reliable as ceramic packages under most environmental conditions. However when the ultimate in system reliability is required, thermal management must be considered as a prime system design goal.

Modern plastic package assembly technology utilizes gold wire bonded to aluminum bonding pads throughout the electronics industry. When exposed to high temperatures for protracted periods of time an intermetallic compound can form in the bond area resulting in high impedance contacts and degradation of device performance. Since the formation of intermetallic compounds is directly related to device junction temperature, it is incumbent on the designer to determine that the device junction temperatures are consistent with system reliability goals.

Predicting Bond Failure Time:

Based on the results of almost ten (10) years of +125°C operating life testing, a special arrhenius equation has been developed to show the relationship between junction temperature and reliability.

$$\text{Eq. (1) } T = (6.376 \times 10^9) e^{\left[\frac{11554.267}{273.15 + T_J} \right]}$$

Where: T = Time in hours to 0.1% bond failure (1 failure per 1,000 bonds).

T_J = Device junction temperature, °C.

And:

$$\text{Eq. (2) } T_J = T_A + PD\theta_{JA} = T_A + \Delta T_J$$

Where: T_J = Device junction temperature, °C.

T_A = Ambient temperature, °C.

PD = Device power dissipation in watts.

θ_{JA} = Device thermal resistance, junction to air, °C/Watt.

ΔT_J = Increase in junction temperature due to on-chip power dissipation.

Table 1 shows the relationship between junction temperature, and continuous operating time to 0.1% bond failure, (1 failure per 1,000 bonds).

TABLE 1 — DEVICE JUNCTION TEMPERATURE versus TIME TO 0.1% BOND FAILURES.

Junction Temperature °C	Time, Hours	Time, Years
80	1,032,200	117.8
90	419,300	47.9
100	178,700	20.4
110	79,600	9.4
120	37,000	4.2
130	17,800	2.0
140	8,900	1.0

Table 1 is graphically illustrated in Figure 8 which shows that the reliability for plastic and ceramic devices are the same until elevated junction temperatures induces intermetallic failures in plastic devices. Early and mid-life failure rates of plastic devices are not effected by this intermetallic mechanism.

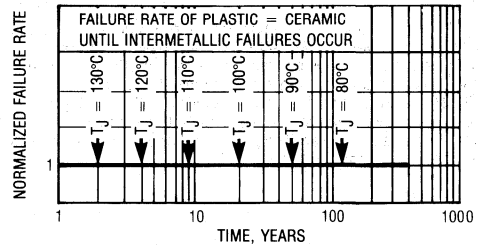


FIGURE 8 — FAILURE RATE versus TIME JUNCTION TEMPERATURE

Procedure

After the desired system failure rate has been established for failure mechanisms other than intermetallics, each device in the system should be evaluated for maximum junction temperature. Knowing the maximum junction temperature, refer to Table 1 or Equation 1 to determine the continuous operating time required to 0.1% bond failures due to intermetallic formation. At this time, system reliability departs from the desired value as indicated in Figure 8.

Air flow is one method of thermal management which should be considered for system longevity. Other commonly used methods include heat sinks for higher powered devices, refrigerated air flow and lower density board stuffing. Since θ_{CA} is entirely dependent on the application, it is the responsibility of the designer to determine its value. This can be achieved by various techniques including simulation, modeling, actual measurement, etc.

The material presented here emphasizes the need to consider thermal management as an integral part of system design and also the tools to determine if the management methods being considered are adequate to produce the desired system reliability.

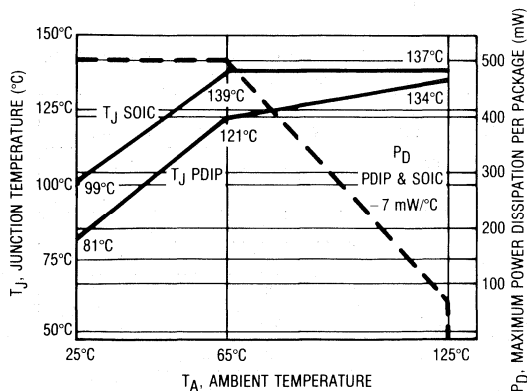


FIGURE 9 — JUNCTION TEMPERATURE FOR WORST CASE CMOS LOGIC DEVICE

This graph illustrates junction temperature for the worst case CMOS Logic device (MC14007UB) — smallest die area operating at maximum power dissipation limit in still air. The solid line indicates the junction temperature, T_J, in a Dual-In-Line (PDIP) package and in a Small Outline IC (SOIC) package versus ambient temperature, T_A. The dotted line indicates maximum allowable power dissipation derated over the ambient temperature range, 25°C to 125°C.

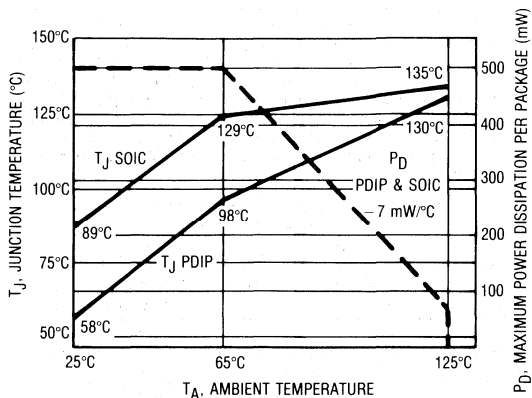


FIGURE 10 — JUNCTION TEMPERATURE FOR TYPICAL CMOS LOGIC DEVICE

This graph illustrates junction temperature for a CMOS Logic device (MC14053B) — average die area operating at maximum power dissipation limit in still air. The solid line indicates the junction temperature, T_J, in a Dual-In-Line (PDIP) package and in a Small Outline IC (SOIC) package versus ambient temperature, T_A. The dotted line indicates maximum allowable power dissipation derated over the ambient temperature range, 25°C to 125°C.

EQUIVALENT GATE COUNT

The equivalent gate count for a logic circuit is the number of gates that would be required to implement the circuit using only NAND gates. The equivalent gate count is a measure of the complexity of a logic circuit. The equivalent gate count is calculated by counting the number of gates in the circuit and then multiplying the number of gates by the number of inputs to each gate. The equivalent gate count is a measure of the complexity of a logic circuit.

Gate Type	Number of Inputs	Equivalent Gate Count
NAND	2	1
NAND	3	1.5
NAND	4	2
NAND	5	2.5
NAND	6	3
NAND	7	3.5
NAND	8	4
NAND	9	4.5
NAND	10	5
NAND	11	5.5
NAND	12	6
NAND	13	6.5
NAND	14	7
NAND	15	7.5
NAND	16	8
NAND	17	8.5
NAND	18	9
NAND	19	9.5
NAND	20	10
NAND	21	10.5
NAND	22	11
NAND	23	11.5
NAND	24	12
NAND	25	12.5
NAND	26	13
NAND	27	13.5
NAND	28	14
NAND	29	14.5
NAND	30	15
NAND	31	15.5
NAND	32	16
NAND	33	16.5
NAND	34	17
NAND	35	17.5
NAND	36	18
NAND	37	18.5
NAND	38	19
NAND	39	19.5
NAND	40	20
NAND	41	20.5
NAND	42	21
NAND	43	21.5
NAND	44	22
NAND	45	22.5
NAND	46	23
NAND	47	23.5
NAND	48	24
NAND	49	24.5
NAND	50	25
NAND	51	25.5
NAND	52	26
NAND	53	26.5
NAND	54	27
NAND	55	27.5
NAND	56	28
NAND	57	28.5
NAND	58	29
NAND	59	29.5
NAND	60	30
NAND	61	30.5
NAND	62	31
NAND	63	31.5
NAND	64	32
NAND	65	32.5
NAND	66	33
NAND	67	33.5
NAND	68	34
NAND	69	34.5
NAND	70	35
NAND	71	35.5
NAND	72	36
NAND	73	36.5
NAND	74	37
NAND	75	37.5
NAND	76	38
NAND	77	38.5
NAND	78	39
NAND	79	39.5
NAND	80	40
NAND	81	40.5
NAND	82	41
NAND	83	41.5
NAND	84	42
NAND	85	42.5
NAND	86	43
NAND	87	43.5
NAND	88	44
NAND	89	44.5
NAND	90	45
NAND	91	45.5
NAND	92	46
NAND	93	46.5
NAND	94	47
NAND	95	47.5
NAND	96	48
NAND	97	48.5
NAND	98	49
NAND	99	49.5
NAND	100	50
NAND	101	50.5
NAND	102	51
NAND	103	51.5
NAND	104	52
NAND	105	52.5
NAND	106	53
NAND	107	53.5
NAND	108	54
NAND	109	54.5
NAND	110	55
NAND	111	55.5
NAND	112	56
NAND	113	56.5
NAND	114	57
NAND	115	57.5
NAND	116	58
NAND	117	58.5
NAND	118	59
NAND	119	59.5
NAND	120	60
NAND	121	60.5
NAND	122	61
NAND	123	61.5
NAND	124	62
NAND	125	62.5
NAND	126	63
NAND	127	63.5
NAND	128	64
NAND	129	64.5
NAND	130	65
NAND	131	65.5
NAND	132	66
NAND	133	66.5
NAND	134	67
NAND	135	67.5
NAND	136	68
NAND	137	68.5
NAND	138	69
NAND	139	69.5
NAND	140	70
NAND	141	70.5
NAND	142	71
NAND	143	71.5
NAND	144	72
NAND	145	72.5
NAND	146	73
NAND	147	73.5
NAND	148	74
NAND	149	74.5
NAND	150	75
NAND	151	75.5
NAND	152	76
NAND	153	76.5
NAND	154	77
NAND	155	77.5
NAND	156	78
NAND	157	78.5
NAND	158	79
NAND	159	79.5
NAND	160	80
NAND	161	80.5
NAND	162	81
NAND	163	81.5
NAND	164	82
NAND	165	82.5
NAND	166	83
NAND	167	83.5
NAND	168	84
NAND	169	84.5
NAND	170	85
NAND	171	85.5
NAND	172	86
NAND	173	86.5
NAND	174	87
NAND	175	87.5
NAND	176	88
NAND	177	88.5
NAND	178	89
NAND	179	89.5
NAND	180	90
NAND	181	90.5
NAND	182	91
NAND	183	91.5
NAND	184	92
NAND	185	92.5
NAND	186	93
NAND	187	93.5
NAND	188	94
NAND	189	94.5
NAND	190	95
NAND	191	95.5
NAND	192	96
NAND	193	96.5
NAND	194	97
NAND	195	97.5
NAND	196	98
NAND	197	98.5
NAND	198	99
NAND	199	99.5
NAND	200	100
NAND	201	100.5
NAND	202	101
NAND	203	101.5
NAND	204	102
NAND	205	102.5
NAND	206	103
NAND	207	103.5
NAND	208	104
NAND	209	104.5
NAND	210	105
NAND	211	105.5
NAND	212	106
NAND	213	106.5
NAND	214	107
NAND	215	107.5
NAND	216	108
NAND	217	108.5
NAND	218	109
NAND	219	109.5
NAND	220	110
NAND	221	110.5
NAND	222	111
NAND	223	111.5
NAND	224	112
NAND	225	112.5
NAND	226	113
NAND	227	113.5
NAND	228	114
NAND	229	114.5
NAND	230	115
NAND	231	115.5
NAND	232	116
NAND	233	116.5
NAND	234	117
NAND	235	117.5
NAND	236	118
NAND	237	118.5
NAND	238	119
NAND	239	119.5
NAND	240	120
NAND	241	120.5
NAND	242	121
NAND	243	121.5
NAND	244	122
NAND	245	122.5
NAND	246	123
NAND	247	123.5
NAND	248	124
NAND	249	124.5
NAND	250	125
NAND	251	125.5
NAND	252	126
NAND	253	126.5
NAND	254	127
NAND	255	127.5
NAND	256	128
NAND	257	128.5
NAND	258	129
NAND	259	129.5
NAND	260	130
NAND	261	130.5
NAND	262	131
NAND	263	131.5
NAND	264	132
NAND	265	132.5
NAND	266	133
NAND	267	133.5
NAND	268	134
NAND	269	134.5
NAND	270	135
NAND	271	135.5
NAND	272	136
NAND	273	136.5
NAND	274	137
NAND	275	137.5
NAND	276	138
NAND	277	138.5
NAND	278	139
NAND	279	139.5
NAND	280	140
NAND	281	140.5
NAND	282	141
NAND	283	141.5
NAND	284	142
NAND	285	142.5
NAND	286	143
NAND	287	143.5
NAND	288	144
NAND	289	144.5
NAND	290	145
NAND	291	145.5
NAND	292	146
NAND	293	146.5
NAND	294	147
NAND	295	147.5
NAND	296	148
NAND	297	148.5
NAND	298	149
NAND	299	149.5
NAND	300	150
NAND	301	150.5
NAND	302	151
NAND	303	151.5
NAND	304	152
NAND	305	152.5
NAND	306	153
NAND	307	153.5
NAND	308	154
NAND	309	154.5
NAND	310	155
NAND	311	155.5
NAND	312	156
NAND	313	156.5
NAND	314	157
NAND	315	157.5
NAND	316	158
NAND	317	158.5
NAND	318	159
NAND	319	159.5
NAND	320	160
NAND	321	160.5
NAND	322	161
NAND	323	161.5
NAND	324	162
NAND	325	162.5
NAND	326	163
NAND	327	163.5
NAND	328	164
NAND	329	164.5
NAND	330	165
NAND	331	165.5
NAND	332	166
NAND	333	166.5
NAND	334	167
NAND	335	167.5
NAND	336	168
NAND	337	168.5
NAND	338	169
NAND	339	169.5
NAND	340	170
NAND	341	170.5
NAND	342	171
NAND	343	171.5
NAND	344	172
NAND	345	172.5
NAND	346	173
NAND	347	173.5
NAND	348	174
NAND	349	174.5
NAND	350	175
NAND	351	175.5
NAND	352	176
NAND	353	176.5
NAND	354	177
NAND	355	177.5
NAND	356	178
NAND	357	178.5
NAND	358	179
NAND	359	179.5
NAND	360	180
NAND	361	180.5
NAND	362	181
NAND	363	181.5
NAND	364	182
NAND	365	182.5
NAND	366	183
NAND	367	183.5
NAND	368	184
NAND	369	184.5
NAND	370	185
NAND	371	185.5
NAND	372	186
NAND	373	186.5
NAND	374	187
NAND	375	187.5
NAND	376	188
NAND	377	188.5
NAND	378	189
NAND	379	189.5
NAND	380	190
NAND	381	190.5
NAND	382	191
NAND	383	191.5
NAND	384	192
NAND	385	192.5
NAND	386	193
NAND	387	193.5
NAND	388	194
NAND	389	194.5
NAND	390	195
NAND	391	195.5
NAND	392	196
NAND	393	196.5
NAND	394	197
NAND	395	197.5
NAND	396	198
NAND	397	198.5
NAND	398	199
NAND	399	199.5
NAND	400	200

Equivalent Gate Count

EQUIVALENT GATE COUNT

The following is a list of equivalent gate counts for some of Motorola's CMOS devices. In general for CMOS, the number of equivalent gates is equal to the total number of transistors on chip divided by four. This list includes only those devices with equivalent gate counts known at the time of this printing.

DEVICE	EQUIVALENT GATE COUNT	DEVICE	EQUIVALENT GATE COUNT
MC14000UB	3.5	MC14094B	79
MC14001B	8	MC14099B	70
MC14001UB	4	MC14161B	72.5
MC14002B	7	MC14163B	72.5
MC14002UB	4	MC14174B	43.5
MC14006B	61.5	MC14175B	39.5
MC14007UB	1.5	MC14194B	40.5
MC14008B	40	MC14490	136.5
MC14011B	8	MC14500B	192
MC14011UB	4	MC14503B	17
MC14012B	7	MC14504B	37.5
MC14012UB	4	MC14508B	42
MC14013B	16	MC14510B	74
MC14014B	74	MC14511B	54
MC14015B	53	MC14512B	17.25
MC14016B	8	MC14514B	59
MC14017B	62.5	MC14515B	67
MC14018B	38.25	MC14516B	61
MC14020B	84	MC14517B	119
MC14021B	74	MC14518B	43.5
MC14023B	9	MC14519B	11.5
MC14023UB	4.5	MC14520B	43.5
MC14024B	59	MC14522B	86
MC14025B	9	MC14526B	86
MC14025UB	4.5	MC14527B	46
MC14028B	26	MC14528B	24
MC14029B	65.5	MC14530B	22
MC14034B	145	MC14531B	44
MC14035B	38.5	MC14532B	38.5
MC14040B	73	MC14534B	206
MC14042B	17.5	MC14536B	103
MC14046B	35	MC14538B	38
MC14049UB	3	MC14539B	20
MC14049B	9	MC14541B	93
MC14050B	6	MC14543B	52
MC14051B	48.5	MC14549B	122
MC14052B	38.5	MC14551B	35
MC14053B	38	MC14553B	147.5
MC14060B	73.5	MC14555B	21
MC14066B	13	MC14556B	25
MC14067B	65	MC14557B	232.5
MC14068B	8	MC14559B	122
MC14069UB	3	MC14562B	206
MC14071B	10	MC14568B	137.25
MC14072B	8	MC14569B	156
MC14073B	10.5	MC14572UB	4
MC14075B	10.5	MC14573	7
MC14076B	32.5	MC14574	9
MC14078B	7.5	MC14575	11
MC14081B	10	MC14583B	14
MC14082B	8	MC14584B	18
MC14093B	18		

PACKAGING INFORMATION

1. General Information
2. Dimensions
3. Weight
4. Material
5. Surface Mounts

6. Environmental Conditions
7. Storage
8. Handling

9. Shipping
10. Receiving

11. Inspection
12. Testing

13. Packaging Information
14. Including Surface Mounts

15. Additional Information
16. Contact Us

17. Revision History
18. Drawings

19. Notes
20. Appendix

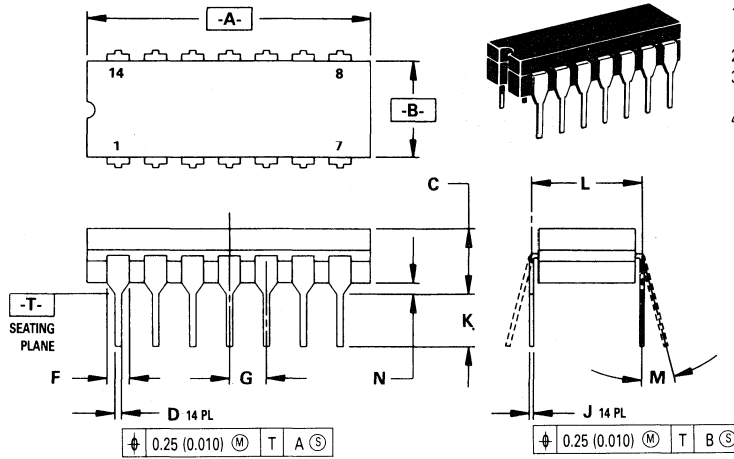
Packaging Information Including Surface Mounts

PACKAGE DIMENSIONS

The standard package availability for each device is indicated on the front page of the individual data sheets. Dimensions for the packages are given in this chapter. Surface mount packages may be special ordered by specifying the following suffixes: "D" (narrow SOIC), "DW" (wide SOIC), or "FN" (PLCC). For example, to order a quad NOR gate, use MC14001BD.

14-PIN PACKAGE

CERAMIC PACKAGE CASE 632-08

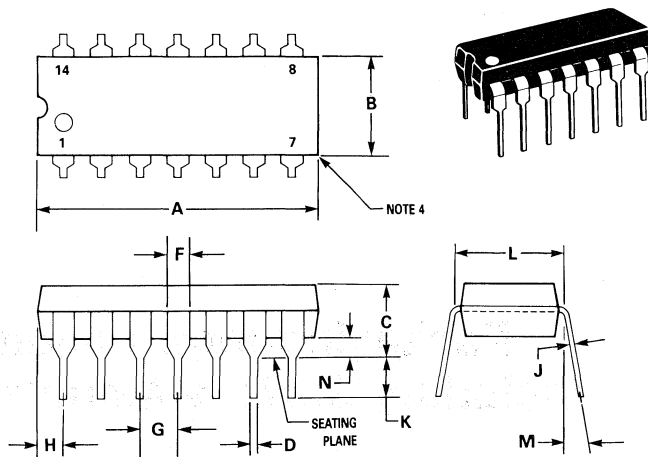


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIM F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	19.05	19.94	0.750	0.785
B	6.23	7.11	0.245	0.280
C	3.94	5.08	0.155	0.200
D	0.39	0.50	0.015	0.020
F	1.40	1.65	0.055	0.065
G	2.54 BSC		0.100 BSC	
J	0.21	0.38	0.008	0.015
K	3.18	4.31	0.125	0.170
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.01	0.020	0.040

PLASTIC PACKAGE CASE 646-06



NOTES:

1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.
4. ROUNDED CORNERS OPTIONAL.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	18.16	19.56	0.715	0.770
B	6.10	6.60	0.240	0.260
C	3.69	4.69	0.145	0.185
D	0.38	0.53	0.015	0.021
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	1.32	2.41	0.052	0.095
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	0°	10°	0°	10°
N	0.39	1.01	0.015	0.039

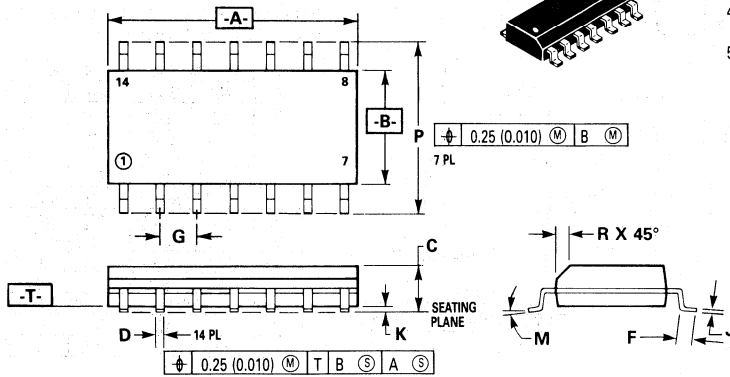
PACKAGE DIMENSIONS (Continued)

14-PIN PACKAGE

SOIC PACKAGE CASE 751A-02 D SUFFIX

NOTES:

1. DIMENSIONS A AND B ARE DATUMS AND T IS A DATUM SURFACE.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
3. CONTROLLING DIMENSION: MILLIMETER.
4. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
5. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.

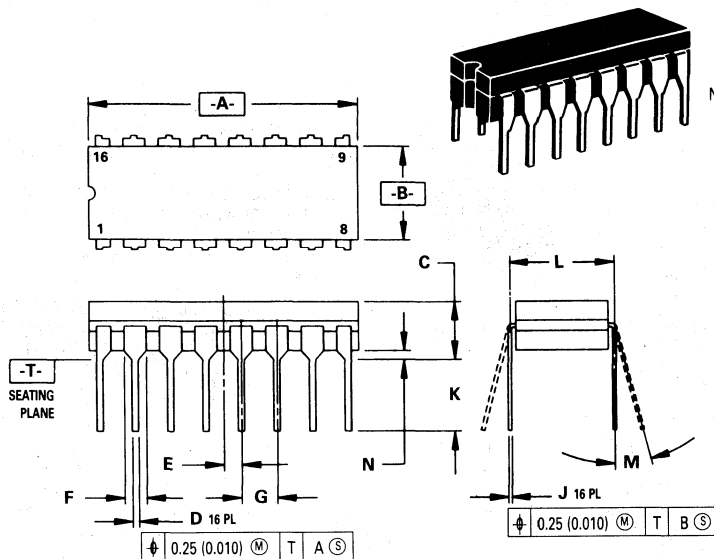


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

PACKAGE DIMENSIONS (Continued)

16-PIN PACKAGE

CERAMIC PACKAGE CASE 620-09

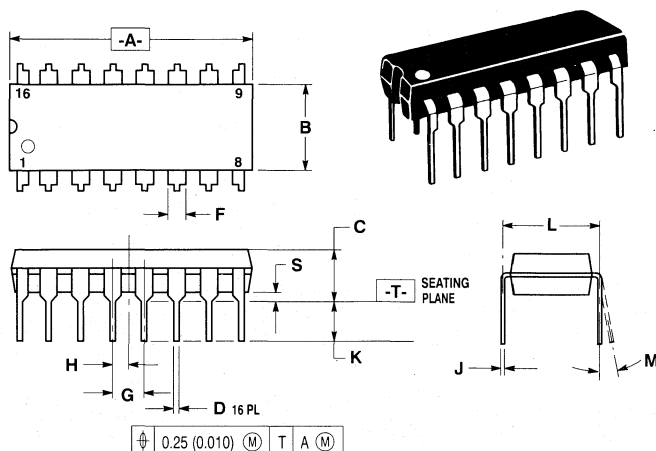


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIM F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	19.05	19.55	0.750	0.770
B	6.10	7.36	0.240	0.290
C	—	4.19	—	0.165
D	0.39	0.53	0.015	0.021
E	1.27 BSC	—	0.050 BSC	—
F	1.40	1.77	0.055	0.070
G	2.54 BSC	—	0.100 BSC	—
J	0.23	0.27	0.009	0.011
K	—	5.08	—	0.200
L	7.62 BSC	—	0.300 BSC	—
M	0°	15°	0°	15°
N	0.39	0.88	0.015	0.035

PLASTIC PACKAGE CASE 648-08



NOTES:

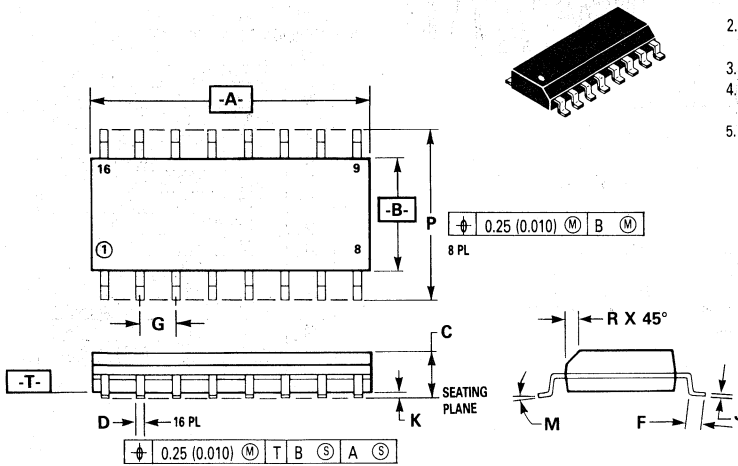
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	18.80	19.55	0.740	0.770
B	6.35	6.85	0.250	0.270
C	3.69	4.44	0.145	0.175
D	0.39	0.53	0.015	0.021
F	1.02	1.77	0.040	0.070
G	2.54 BSC	—	0.100 BSC	—
H	1.27 BSC	—	0.050 BSC	—
J	0.21	0.38	0.008	0.015
K	2.80	3.30	0.110	0.130
L	7.50	7.74	0.295	0.305
M	0°	10°	0°	10°
S	0.51	1.01	0.020	0.040

PACKAGE DIMENSIONS (Continued)

16-PIN PACKAGE

SOIC PACKAGE CASE 751B-03 D SUFFIX

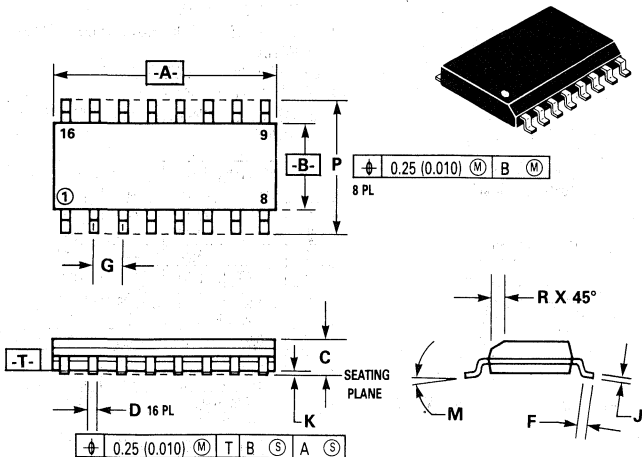


NOTES:

1. DIMENSIONS A AND B ARE DATUMS AND T IS A DATUM SURFACE.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
3. CONTROLLING DIMENSION: MILLIMETER.
4. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
5. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

SOIC PACKAGE CASE 751G-01 DW SUFFIX



NOTES:

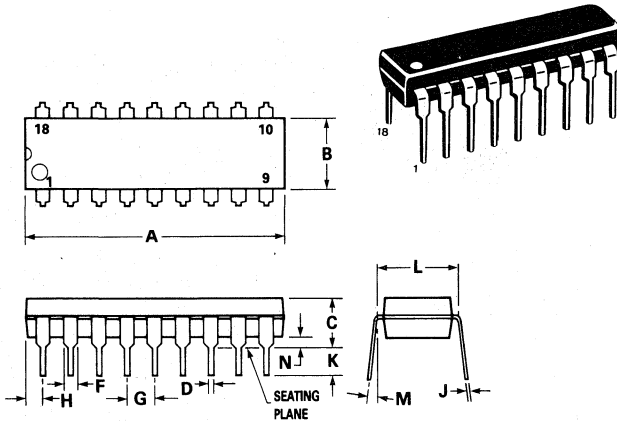
1. DIMENSIONS A AND B ARE DATUMS AND T IS A DATUM SURFACE.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
3. CONTROLLING DIMENSION: MILLIMETER.
4. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
5. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	10.15	10.45	0.400	0.411
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
J	0.25	0.32	0.010	0.012
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	10.05	10.55	0.395	0.415
	0.25	0.75	0.010	0.029

PACKAGE DIMENSIONS (Continued)

18-PIN PACKAGE

PLASTIC PACKAGE CASE 707-02

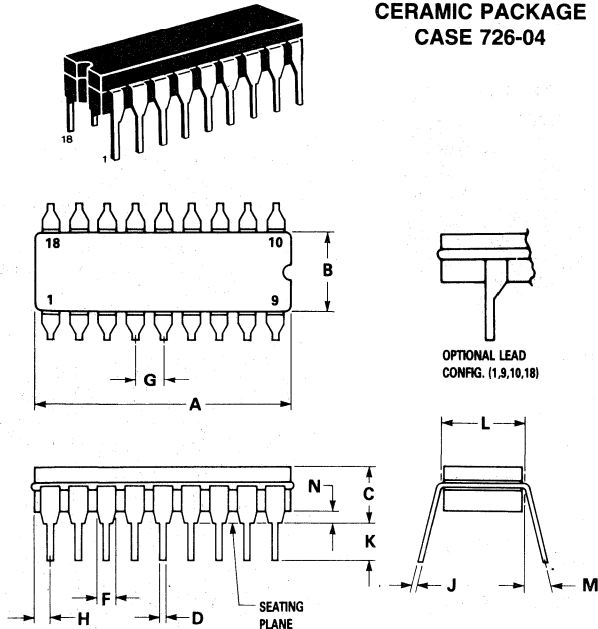


NOTES:

1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25mm(0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	22.22	23.24	0.875	0.915
B	6.10	6.60	0.240	0.260
C	3.56	4.57	0.140	0.180
D	0.36	0.56	0.014	0.022
F	1.27	1.78	0.050	0.070
G	2.54 BSC		0.100 BSC	
H	1.02	1.52	0.040	0.060
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

CERAMIC PACKAGE CASE 726-04



NOTES:

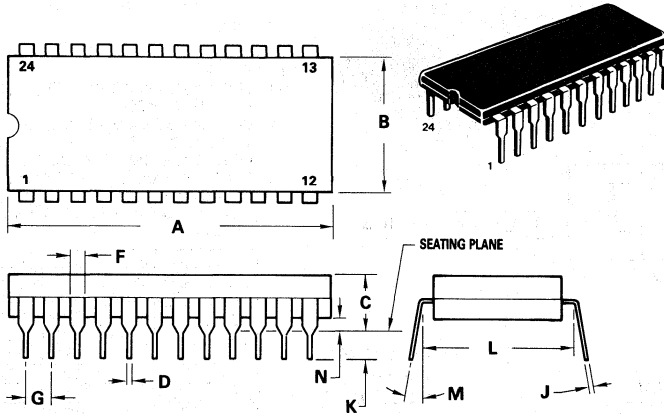
1. LEADS, TRUE POSITIONED WITHIN 0.25 mm (0.010) DIA. AT SEATING PLANE, AT MAXIMUM MATERIAL CONDITION.
2. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIM "A" & "B" INCLUDES MENISCUS.
4. "F" DIMENSION IS FOR FULL LEADS. "HALF" LEADS ARE OPTIONAL AT LEAD POSITIONS 1, 9, 10, AND 18.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	22.35	23.11	0.880	0.910
B	6.10	7.49	0.240	0.295
C	—	5.08	—	0.200
D	0.38	0.53	0.015	0.021
F	1.40	1.78	0.055	0.070
G	2.54 BSC		0.100 BSC	
H	0.51	1.14	0.020	0.045
J	0.20	0.30	0.008	0.012
K	3.18	4.32	0.125	0.170
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

PACKAGE DIMENSIONS (Continued)

24-PIN PACKAGE

CERAMIC PACKAGE CASE 623-05

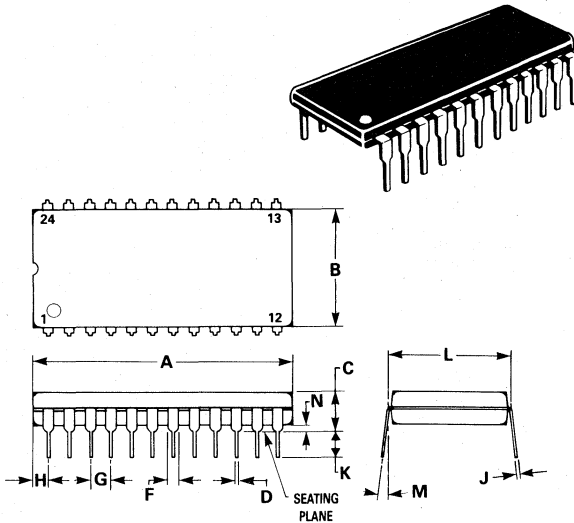


NOTES:

- DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
- LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION. (WHEN FORMED PARALLEL).

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	31.24	32.77	1.230	1.290
B	12.70	15.49	0.500	0.610
C	4.06	5.59	0.160	0.220
D	0.41	0.51	0.016	0.020
F	1.27	1.52	0.050	0.060
G	2.54 BSC		0.100 BSC	
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.27	0.020	0.050

PLASTIC PACKAGE CASE 709-02



NOTES:

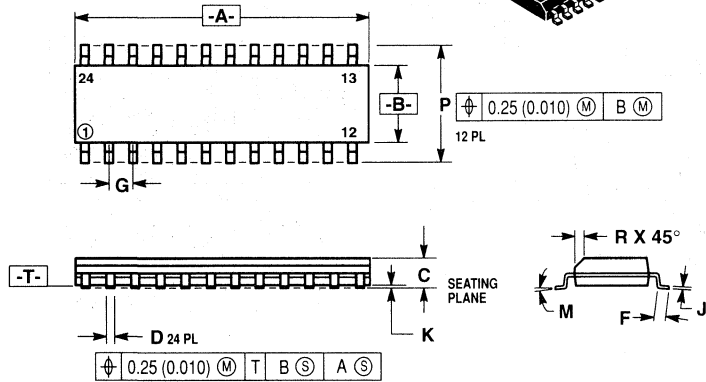
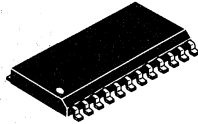
- POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25 mm (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
- DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
- DIMENSION B DOES NOT INCLUDE MOLD FLASH.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	31.37	32.13	1.235	1.265
B	13.72	14.22	0.540	0.560
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.03	0.065	0.080
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

PACKAGE DIMENSIONS (Continued)

24-PIN PACKAGE

DW SUFFIX
SOIC
CASE 751E-03



NOTES:

1. DIMENSIONS A AND B ARE DATUMS AND T IS A DATUM SURFACE.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
3. CONTROLLING DIMENSION: MILLIMETER.
4. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
5. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	15.25	15.54	0.601	0.612
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.41	0.90	0.016	0.035
G	1.27 BSC		0.050 BSC	
J	0.229	0.317	0.0090	0.0125
K	0.127	0.292	0.0050	0.0115
M	0°	8°	0°	8°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

1 Master Index

2 Product Selection Guide

3 The “Better” Program

4 B and UB Series Family Data

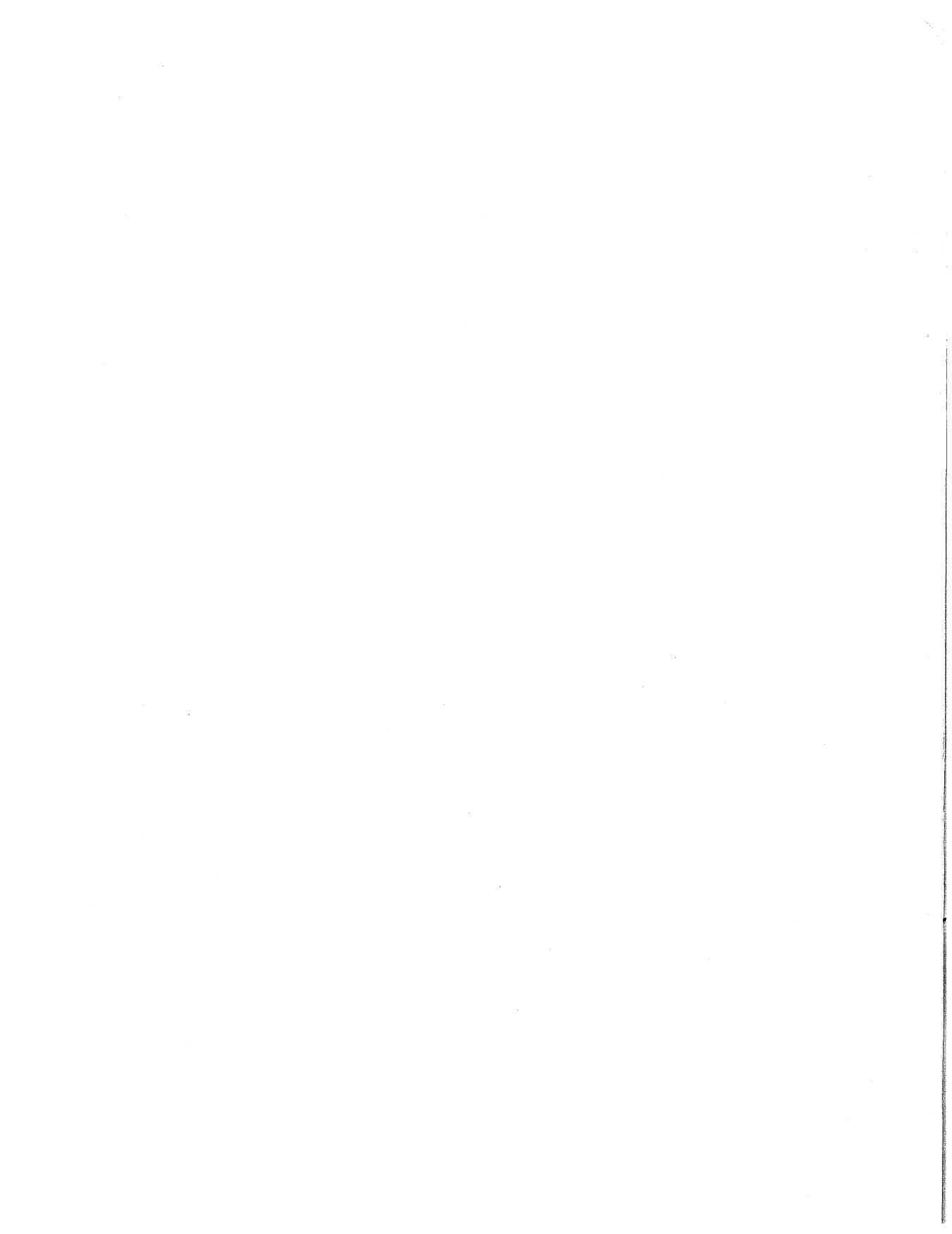
5 CMOS Handling and Design Guidelines

6 Data Sheets

7 CMOS Reliability

8 Equivalent Gate Count

**9 Packaging Information
Including Surface Mounts**





Literature Distribution Centers:

USA: Motorola Literature Distribution; P.O. Box 20912; Phoenix, Arizona 85036

EUROPE: Motorola Ltd.; European Literature Center; 88 Tanners Drive, Blakelands, Milton Keynes MK14 5BP, England

JAPAN: Nippon Motorola Ltd.; 4-32-1, Nishi-Gotanda, Shinagawa-ku, Tokyo 141 Japan

ASIA-PACIFIC: Motorola Semiconductors H.K. Ltd.; Silicon Harbour Center, No. 2 Dai King Street, Tai Po Industrial Estate, Tai Po, N.T., Hong Kong.